

Power Management Products Data Book

Volume 1

Literature Number: SLVD003



Printed on Recycled Paper

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Von Hoffmann Graphics
Owensville, Missouri

INTRODUCTION

The Texas Instruments 1999 Power Management Products Data Book Set showcases TI's broad portfolio of analog components for power supply designs. Featured in this set are most of the components previously found in the 1996 Power Supply Circuits Data Book, the new and exciting power management products introduced since then, and other components useful for power supply designs.

The set consists of three product area specific volumes:

- Power Management Products, Volume 1:
 - Linear voltage regulators
 - Shunt regulators
 - Voltage references
 - Precision virtual grounds
- Power Management Products, Volume 2:
 - Processor power supply controllers (DSP and CPU)
 - Switching power supply controllers and DC/DC charge pump converters
 - MOSFET drivers
 - Supervisory circuits
- Power Management Products, Volume 3:
 - Power distribution switches
 - LED drivers
 - Voltage Rail splitters
 - Special Functions

More than a collection of data sheets, this data book set is a tool for locating the best power management components for a successful design effort. It is structured to help you quickly find the devices best suited to your application. The set contains:

- An alphanumeric index at the beginning of each book to make finding known part numbers simple.
- Product selection guides with a condensed view of parametric information organized to help you choose the devices that most closely fit your needs.
- Key specifications and features presented for easy comparison.
- A section on mechanical specifications for all packages used with Texas Instruments power management devices.

While this data book offers design and specification data only for power management products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or from the TI web site at:

<http://www.ti.com/sc>

We believe you will find the 1999 Power Management Data Book set to be a valuable addition to your collection of technical literature.

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1 General Information (Vol. 1)

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FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS

Device	VO (typ) (V)	IO (max) (mA)	Vdo (typ) (V)	Vdo (max) (V)	Iq (typ) (mA)	Tolerance (%)	VIN (max) (V)	Shutdown	SVS	Description	Page No.
TPS76912	1.224	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77012	1.224	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS76515	1.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76615	1.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76715	1.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76815	1.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76915	1.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77015	1.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS77515	1.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-373
TPS77615	1.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-373
TPS77715	1.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-391
TPS77815	1.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-391
TPS76316	1.6	150	0.36	0.6	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS76318	1.8	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS73HD318	1.8	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2-185
TPS76518	1.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76618	1.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76718	1.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS767D318	1.8	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2-311
TPS76818	1.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76918	1.8	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77018	1.8	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS77518	1.8	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-373
TPS77718	1.8	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-391
TPS77618	1.8	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-373
TPS77818	1.8	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-391
TPS76325	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS71025	2.5	500	0.33	0.5	0.29	2	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-59
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TPS7325	2.5	500	0.27	0.6	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-145
TPS73HD325	2.5	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2-185
TPS76425	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-247
TPS76525	2.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261

LINEAR VOLTAGE REGULATORS SELECTION GUIDE

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V _O (typ) (V)	I _O (max) (mA)	V _{do} (typ) (V)	V _{do} (max) (V)	I _q (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SYS	Description	Page No.
TPS76625	2.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76725	2.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS767D325	2.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2-311
TPS76825	2.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76925	2.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77025	2.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS77525	2.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-373
TPS77625	2.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-373
TPS77725	2.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-391
TPS77825	2.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-391
TPS76327	2.7	150	0.36	0.6	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS76427	2.7	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-247
TPS76527	2.7	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76627	2.7	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76727	2.7	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76827	2.7	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76927	2.7	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77027	2.7	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS76928	2.784	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77028	2.784	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS7228	2.8	250			0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2-113
TPS76328	2.8	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS76428	2.8	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-247
TPS76528	2.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76628	2.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76728	2.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76828	2.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS7230	3	250	0.39	0.9	0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2-113
TPS7330	3	500	0.052	0.075	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-145
TPS76030	3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-211
TPS76130	3	100	0.17	0.28	2.6	3.6	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-221
TPS76330	3	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS76430	3	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-247

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V _O (typ) (V)	I _O (max) (mA)	V _{DO} (typ) (V)	V _{DO} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76530	3	150	0.16	0.28	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76630	3	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76730	3	1000	0.45	0.675	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76830	3	1000	0.45	0.675	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS77030	3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS76930	3.09	100	0.115	0.23	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS76032	3.2	50	0.12	0.18	0.85	3.1	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-211
TPS76132	3.2	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-221
TPS7133QPWP	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-3
TPS7133	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-29
TPS71H33	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-75
TPS7233	3.3	250	0.14	0.18	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2-113
TPS7333	3.3	500	0.044	0.06	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-145
TPS76033	3.3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-211
TPS76133	3.3	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-221
TPS76633	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-291
TPS76433	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-247
TPS76533	3.3	150	0.14	0.24	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76633	3.3	250	0.23	0.4	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76733	3.3	1000	0.35	0.575	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76833	3.3	1000	0.35	0.575	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76933	3.3	100	0.098	0.2	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77033	3.3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TPS77533	3.3	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-373
TPS77633	3.3	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-373
TPS77733	3.3	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2-391
TPS77833	3.3	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2-391
TLV2217-33	3.3	500	0.4	0.5	19	1	12	No	No	LDO	2-461
TPS76038	3.8	50	0.12	0.18	0.85	2.6	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-211
TPS76138	3.8	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-221
TPS76338	3.8	150	0.36	0.6	0.085	3.5	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS7148	4.95	500	0.03	0.037	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-29
TPS71H48	4.95	500	0.03	0.047	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-75

LINEAR VOLTAGE REGULATORS SELECTION GUIDE

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V _O (typ) (V)	I _O (max) (mA)	V _{DO} (typ) (V)	V _{DO} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS7248	4.85	250	0.09	0.1	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2-113
TPS7348	4.85	500	0.028	0.037	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-145
TPS7150	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-29
TPS71H50	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2-75
TPS7250	5	250	0.76	0.85	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2-113
TPS7350	5	500	0.027	0.035	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-145
TPS76050	5	50	0.12	0.18	0.85	2	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-211
TPS76150	5	100	0.17	0.28	2.6	2.8	16	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-221
TPS76350	5	150	0.18	0.3	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-231
TPS76550	5	150	0.085	0.15	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-261
TPS76650	5	250	0.14	0.25	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2-277
TPS76750	5	1000	0.23	0.38	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2-293
TPS76850	5	1000	0.23	0.38	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2-329
TPS76950	5	100	0.071	0.17	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-345
TPS77050	5	50	0.035	0.085	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT-23	2-359
TL750L05	5	150	0.2	0.6	10	4	26	No	No	Fixed, LDO, Positive Output	2-421
TL750M05	5	750	0.5	0.6	60	2	26	No	No	Fixed, LDO, Positive Output	2-429
TL751L05	5	150	0.2	0.6	10	4	26	Yes	No	Fixed, LDO, Positive Output	2-421
TL751M05	5	750	0.5	0.6	60	2	26	Yes	No	Fixed, LDO, Positive Output	2-429
TL750L08	8	150	0.2	0.7	10	4	26	No	No	Fixed, LDO, Positive Output	2-421
TL750M08	8	750	0.5	0.7	60	2	26	No	No	Fixed, LDO, Positive Output	2-429
TL751L08	8	150	0.2	0.7	10	4	26	Yes	No	Fixed, LDO, Positive Output	2-421
TL751M08	8	750	0.5	0.7	60	2	26	Yes	No	Fixed, LDO, Positive Output	2-429
TL750L10	10	150	0.2	0.8	10	4	26	No	No	Fixed, LDO, Positive Output	2-421
TL750M10	10	750	0.5	0.8	60	2	26	No	No	Fixed, LDO, Positive Output	2-429
TL751L10	10	150	0.2	0.8	10	4	26	Yes	No	Fixed, LDO, Positive Output	2-421
TL751M10	10	750	0.5	0.8	60	2	26	Yes	No	Fixed, LDO, Positive Output	2-429
TL750L12	12	150	0.2	0.9	10	4	26	No	No	Fixed, LDO, Positive Output	2-421
TL750M12	12	750	0.5	0.9	60	2	26	No	No	Fixed, LDO, Positive Output	2-429
TL751L12	12	150	0.2	0.9	10	4	26	Yes	No	Fixed, LDO, Positive Output	2-421
TL751M12	12	750	0.5	0.9	60	2	26	Yes	No	Fixed, LDO, Positive Output	2-429

ADJUSTABLE OUTPUT-VOLTAGE REGULATORS

Device	V _O Adjustable (nom) (V)	I _O (max) (mA)	V _{do} (typ) (V)	V _{do} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76501	1.2 – 5.5	150	0.16	0.33	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2-261
TPS76601	1.2 – 5.5	250	0.23	0.54	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2-277
TPS76701	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Adjustable, LDO, Positive Output	2-293
TPS767D301	1.2 – 5.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2-311
TPS76801	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	No	Adjustable, LDO, Positive Output	2-329
TPS76901	1.2 – 5.5	100	0.071	0.245	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT-23	2-345
TPS77001	1.2 – 5.5	50	0.035	0.125	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT-23	2-359
TPS77501	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2-373
TPS77601	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2-373
TPS77701	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2-391
TPS77801	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2-391
TPS76301	1.5 – 6.5	150	0.6	0.6	0.085	3	10	Yes	No	Adjustable, LDO, Positive Output, SOT-23	2-231
TPS7101	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2-29
TPS71H01	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2-75
TPS7201	1.2 – 9.75	250	0.16	0.27	0.155	3	10	Yes	No	Adjustable, LDO	2-113
TPS7301	1.2 – 9.75	500	0.052	0.085	0.34	3	10	Yes	Yes	Adjustable, LDO	2-145
TPS73HD301	1.2 – 9.75	750	0.353	0.6	1.1	3	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2-185
TL317	1.2 – 32	100	2.5	3	1.5	4	35	No	No	Adjustable	2-415
μA723	2 – 37	150		3	2.3	1	40	No	No	Adjustable	2-467
TL783	1.25 – 125	700	10	15	15	6	125	No	No	Adjustable	2-449
LM237	-1.2 – -37	1500			2.2			No	No	3-Terminal Adjustable Regulator	2-409
LM337	-1.2 – -37	1500			2.2			No	NO	3-Terminal Adjustable Regulator	2-409

LINEAR VOLTAGE REGULATORS SELECTION GUIDE

FIXED POSITIVE-OUTPUT VOLTAGE REGULATORS

Device	V _O (typ) (V)	I _O (max) (mA)	V _{do} (typ) (V)	V _{do} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (min) (V)	Shutdown	SVS	Description	Page No.
μA78L02A	2	100	1.7	3	3.6	5	20	No	No	Fixed, Positive Output	2-493
TL-SCSI285	2.85	500		0.7	26	1	5.5	No		Fixed Reg. for SCSI Active Termination	2-527
TL2217-285	2.85	500		1	26	1.5	5.5	No		Fixed Reg. for SCSI Active Termination	2-533
μA7805	5	1500	2	3	4.2	4	25	No	No	Fixed, Positive Output	2-479
μA78L05	5	100	2	3	3.8	10	20	No	No	Fixed, Positive Output	2-493
μA78L05A	5	100	1.7	3	3.8	5	20	No	No	Fixed, Positive Output	2-493
μA78M05	5	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2-505
TL780-05	5	1500	2	3	5	1	25	No	No	Fixed, Positive Output	2-441
μA7806	6	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2-479
μA78L06	6	100	1.7	3	3.9	10	20	No	No	Fixed, Positive Output	2-493
μA78L06A	6	100	1.7	3	3.9	5	20	No	No	Fixed, Positive Output	2-493
μA78M06	6	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2-505
μA7808	8	1500	2.5	3	4.3	4	25	No	No	Fixed, Positive Output	2-479
μA7885	8	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2-479
μA78L08	8	100	1.7	3	4	10	23	No	No	Fixed, Positive Output	2-493
μA78L08A	8	100	1.7	3	4	5	23	No	No	Fixed, Positive Output	2-493
μA78M08	8	500	2.5	3	4.6	4	25	No	No	Fixed, Positive Output	2-505
μA78L09	9	100	1.7	3	4.1	10	24	No	No	Fixed, Positive Output	2-493
μA78L09A	9	100	1.7	3	4.1	5	24	No	No	Fixed, Positive Output	2-493
μA78M09	9	500	2.5	3	4.6	4	26	No	No	Fixed, Positive Output	2-505
μA7810	10	1500	2.5	3	4.3	4	28	No	No	Fixed, Positive Output	2-479
μA78L10	10	100	1.7	3	4.2	10	25	No	No	Fixed, Positive Output	2-493
μA78L10A	10	100	1.7	3	4.2	5	25	No	No	Fixed, Positive Output	2-493
μA78M10	10	500	2.5	3	4.6	4	28	No	No	Fixed, Positive Output	2-505
TL780-12	12	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2-441
μA7812	12	1500	2.5	3	4.3	4	30	No	No	Fixed, Positive Output	2-479
μA78L12	12	100	1.7	3	4.3	10	27	No	No	Fixed, Positive Output	2-493
μA78L12A	12	100	1.7	3	4.3	5	27	No	No	Fixed, Positive Output	2-493
μA78M12	12	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2-505
TL780-15	15	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2-441
μA7815	15	1500	2.5	3	4.4	4	30	No	No	Fixed, Positive Output	2-479
μA78L15	15	100	1.7	3	4.6	10	30	No	No	Fixed, Positive Output	2-493
μA78L15A	15	100	1.7	3	4.6	5	30	No	No	Fixed, Positive Output	2-493

FIXED POSITIVE-OUTPUT VOLTAGE REGULATORS (continued)

Device	V _O (typ) (V)	I _O (max) (mA)	V _{do} (typ) (V)	V _{do} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SVS	Description	Page No.
μA78M15	15	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2-505
μA7818	18	1500	3	3	4.5	4	33	No	No	Fixed, Positive Output	2-479
μA78M20	20	500	3	3	4.9	4	35	No	No	Fixed, Positive Output	2-505
μA7824	24	1500	3	3	4.6	4	38	No	No	Fixed, Positive Output	2-479
μA78M24	24	500	3	3	5	4	38	No	No	Fixed, Positive Output	2-505

FIXED NEGATIVE-OUTPUT VOLTAGE REGULATORS

Device	V _O (typ) (V)	I _O (max) (mA)	V _{do} (typ) (V)	V _{do} (max) (V)	I _q (typ) (mA)	Tolerance (%)	V _{IN} (max) (V)	Shutdown	SVS	Description	Page No.
μA79M05	-5	500	2	3	1	4	-25	No	No	Fixed, Negative Output	2-517
μA79M06	-6	500	2	3	1	4	-25	No	No	Fixed, Negative Output	2-517
μA79M08	-8	500	2.5	3	1	4	-25	No	No	Fixed, Negative Output	2-517
μA79M12	-12	500	2.5	3	1.5	4	-30	No	No	Fixed, Negative Output	2-517
μA79M15	-15	500	2.5	3	1.5	4	-30	No	No	Fixed, Negative Output	2-517
μA79M20	-20	500	3	3	1.5	4	-35	No	No	Fixed, Negative Output	2-517
μA79M24	-24	500	3	3	1.5	4	-38	No	No	Fixed, Negative Output	2-517



SHUNT REGULATOR and PRECISION VIRTUAL GROUND SELECTION GUIDE

SHUNT REGULATORS

Device	V _{ref} (V)	I _Z (min) (μ A)	I _Z (max) (mA)	V _O (min) (V)	V _O (max) (V)	Tolerance (%)	V _I (max) (V)	Temp Coeff (typ) (ppm/ $^{\circ}$ C)	Description	Page No.
TLV431A	1.24	100	15	V _{ref}	6	1	6	46	Adjustable Shunt	3-45
TL1431	2.5	1000	100	V _{ref}	36	0.4	36	30	Adjustable Shunt	3-27
TL431	2.5	1000	100	V _{ref}	36	2	36	30	Adjustable Shunt	3-9
TL431A	2.5	1000	100	V _{ref}	36	1	36	30	Adjustable Shunt	3-9
TLV431	2.5	1000	100	V _{ref}	36	2	36	30	Adjustable Shunt	3-45
TL430	2.75	2000	100	V _{ref}	30	9	30	120	Adjustable Shunt	3-3

PRECISION VIRTUAL GROUNDS

Device	I _O (typ) (mA)	Output Regulation (typ) (μ A)	V _O (min) (V)	V _O (max) (V)	V _I (max) (V)	Temp Coeff (typ) (ppm/ $^{\circ}$ C)	Description	Page No.
TLE2425	20	-45 - 15	2.48	2.52	40	20	Precision Virtual Ground	4-3

PROCESSOR POWER SUPPLY CONTROLLERS

Device	Drop Comp	OCP	Output Drive Current (A)	Outputs	OVP	Power Good	Soft Start	UVLO	V _{IN} (V)	V _O (typ) (V)	V _{ref} (tol) (±%)	Description	Page No.
TPS5102	No	Yes	1.5	2	No	No	Yes	Yes	4.5 - 25	1.2 - V _{CC}	1.5	Notebook	7-3
TPS5103	No	Yes	1.5	1	No	No	Yes	Yes	4.5 - 25	1.2 - V _{CC}	1.5	Multipurpose	7-33
TPS5210	Yes	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1	Pentium class	7-123
TPS5211	Yes	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1.5	Pentium class	7-89
TPS5602	No	Yes	1	2	No	No	Yes	Yes	4.5 - 25	1.2 - V _{CC}	2	DSP	7-149
TPS56100	No	Yes	2	1	Yes	Yes	Yes	Yes	5	0.9 - V _{CC}	1.5	DSP	7-171
TPS5615	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.5	1	DSP	7-99
TPS5618	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.8	1	DSP	7-99
TPS5625	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	2.8	1	DSP	7-99
TPS5633	No	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	3.3	1	DSP	7-99

SWITCHING POWER SUPPLY CONTROLLER and DC/DC CHARGE PUMP CONVERTER SELECTION GUIDE

SWITCHING POWER SUPPLY CONTROLLERS

Device	SHDN	Pulse -by- Pulse Isense	Vin Range (VDC)	Output Type	Output Current (mA)	Freq (max) (kHz)	Operating/ Standby Current (mA)	Reference Voltage (V)	Vref Tol (%)	Duty Cycle (max) (%)	UVLO	Description	Page No.
SG2524	Yes	No	8-40	Single Switch	100	500	NA/8	5	4	90	No	Voltage-Mode PWM	8-97
SG3524	Yes	No	8-40	Single Switch	100	500	NA/8	5	8	90	No	Voltage-Mode PWM	8-97
TL494	No	No	7-40	Single Switch	200	300	7.5/6	5	5	90	No	Voltage-Mode PWM	8-111
TL497A	Yes	No	4.5-12	Single Switch	500	50	11/6	1.2	5		No	Fixed On-Time Voltage-Mode	8-121
TL499A	No	No	1.1-35	Single Switch	500	40	1.8/NA	1.26	5		No	Fixed On-Time Voltage-Mode	8-129
TL594	No	No	7-40	Single Switch	200	300	12.4/9	5	1	90	Yes	Voltage-Mode PWM	8-137
TL598	No	No	7-40	Totem Pole	-250	300	15/NA	5	1	90	Yes	Voltage-Mode PWM	8-149
UC2842	No	Yes	30	Totem Pole	-200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8-159
UC2843	No	Yes	30	Totem Pole	-200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8-159
UC2844	No	Yes	30	Totem Pole	-200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8-159
UC2845	No	Yes	30	Totem Pole	-200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8-159
UC3842	No	Yes	30	Totem Pole	-200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8-159
UC3843	No	Yes	30	Totem Pole	-200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8-159
UC3844	No	Yes	30	Totem Pole	-200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8-159
UC3845	No	Yes	30	Totem Pole	-200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8-159
TL5001	No	No	3.6-40	Single Switch	20	400	1.1/1	1	5	100	Yes	Voltage-Mode PWM	8-79
TL5001A	No	No	3.6-40	Single Switch	20	400	1.1/1	1	3	100	Yes	Voltage-Mode PWM	8-79
LT1054	No	No	3.6-15	Totem Pole	±100	2000	3.5/3.1	1.25	2.5	100	Yes	Dual Channel- Mode PWM	8-171

LOW-NOISE CHARGE PUMP DC/DC CONVERTERS

Device	SHDN	VO (typ) (V)	Tolerance (%)	V _{IN} Range (VDC)	Output Current (mA)	Freq (max) (kHz)	Quiescent Current (μ A)	Shutdown Current (μ A)	UVLO	Description	Page No.
TPS60100	Yes	3.3	± 4	1.8-3.6	200	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8-3
TPS60101	Yes	3.3	± 4	1.8-3.6	100	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8-23
TPS60110	Yes	5	± 4	2.7-5.4	300	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8-43
TPS60111	Yes	5	± 4	2.7-5.4	150	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8-61

MOSFET DRIVERS SELECTION GUIDE

MOSFET DRIVERS

Device	I _{CC} (μ A)	Internal Regulator	Output Current (max) (A)	Rise/Fall Time (max) (ns)	Supply Voltage(s) (V)	Description	Page No.
TPS2811	5	Yes (8 - 40 V)	2	20	4-14	Dual Channel	9-3
TPS2812	5	Yes (8 - 40 V)	2	20	4-14	Dual Channel	9-3
TPS2813	5	Yes (8 - 40 V)	2	20	4-14	Dual Channel	9-3
TPS2814	5	No	2	20	4-14	Dual Channel	9-3
TPS2815	5	No	2	20	4-14	Dual Channel	9-3
TPS2816	150	Yes (8 - 40 V)	2	25	4-14	Active Pullup, Internal Regulator, Single Channel	9-31
TPS2817	150	Yes (8 - 40 V)	2	25	4-14	Active Pullup, Internal Regulator, Single Channel	9-31
TPS2818	25	Yes (8 - 40 V)	2	25	4-14	Single Channel	9-31
TPS2819	25	Yes (8 - 40 V)	2	25	4-14	Single Channel	9-31
TPS2828	25	No	2	25	4-14	Single Channel	9-31
TPS2829	25	No	2	25	4-14	Single Channel	9-31
TPS2830	1	No	2	50 / 85	4.5-15	Fast Synchronous-Buck With Deadtime Control	9-49
TPS2831	1	No	2	50 / 85	4.5-15	Fast Synchronous-Buck With Deadtime Control	9-49
TPS2832	1	No	2	50 / 85	4.5-15	Fast Synchronous-Buck With Deadtime Control	9-61
TPS2833	1	No	2	50 / 85	4.5-15	Fast Synchronous-Buck With Deadtime Control	9-61

SUPERVISORY CIRCUITS

Device	V _{CC} (nom) (V)	V _t (V)	Tolerance (%)	I _{CC} (max) (mA)	V _{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3123J12	1.2	1.08	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10-21
TPS3124J12	1.2	1.08	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10-21
TPS3125J12	1.2	1.08	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10-21
TPS3123G15	1.5	1.4	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10-21
TPS3124G15	1.5	1.4	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10-21
TPS3125G15	1.5	1.4	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10-21
TPS3123J18	1.8	1.62	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10-21
TPS3124J18	1.8	1.62	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10-21
TPS3125J18	1.8	1.62	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10-21
TPS3305-18	1.8	1.68	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10-33
TPS3307-18	1.8	1.68	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10-43
TLC7725	2.5	2.25	3	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10-9
TPS3707-25	2.5	2.25	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10-53
TPS3801J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-63
TPS3305-25	2.5	2.25	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10-33
TPS3809J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-3
TPS3820-25	2.5	2.25	1.8	0.025		No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3823-25	2.5	2.25	1.8	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3824-25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3825-25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3828-25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3307-25	2.5	2.25	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10-43
TLC7703	3	2.63	2.7	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10-9
TPS3125L30	3	2.64	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10-21
TPS3705-30	3	2.63	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10-53
TPS3707-30	3	2.63	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10-53
TPS3801L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-63
TPS3809L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-3
TPS3820-30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3823-30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3824-30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71

SUPERVISORY CIRCUITS SELECTION GUIDE

SUPERVISORY CIRCUITS (continued)

Device	V _{CC} (nom) (V)	V _t (V)	Tolerance (%)	I _{CC} (max) (mA)	V _{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3825-30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3828-30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TL7733	3.3	2.93	2.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10-9
TPS3705-33	3.3	2.93	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10-53
TPS3707-33	3.3	2.93	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10-53
TPS3801K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-63
TPS3809K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-3
TPS3820-33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3823-33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3824-33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3825-33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3828-33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TL7705A	5	4.55	2	3	3.6	No	Yes	1	No	Programmable Delay	10-91
TL7705B	5	4.55	2	3	1	No	Yes	1	No	Programmable Delay	10-113
TL7757	5	4.55	3	2.5	1	No	No	1	No	No Delay	10-123
TL7759	5	4.55	3	2	1	No	Yes	1	No	No Delay	10-133
TL7770-5	5	4.55	1.5	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10-9
TPS3705-50	5	4.55	2	0.05	2	No	No	2	No	Programmable Delay	10-139
TPS3707-50	5	4.55	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10-53
TPS3801I50	5	4.55	2	0.012	2	No	Yes	1	No	Fixed Delay, Micropower	10-53
TPS3305-33	5	4.55	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10-63
TPS3809I50	5	4.55	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10-33
TPS3820-50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-3
TPS3823-50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3824-50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3825-50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3828-50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10-71
TPS3307-33	5	4.55	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10-43
TL7709A	9	7.6	2	3	3.6	No	Yes	1	No	Programmable Delay	10-91

SUPERVISORY CIRCUITS (continued)

Device	V _{CC} (nom) (V)	V _I (V)	Tolerance (%)	I _{CC} (max) (mA)	V _{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TL7712A	12	10.8	2	3	3.6	No	Yes	1	No	Programmable Delay	10-91
TL7770-12	12	10.9	1	5	1	Yes	Yes	2	No	Programmable Delay	10-139
TL7715A	15	13.5	2	3	3.6	No	Yes	1	No	Programmable Delay	10-91
TPS5510			3	1	4	Yes	Yes	3	No	Fixed Delay	10-79
TPS5511			3	1	4	Yes	Yes	3	No	Fixed Delay	10-85
TL7700	adj			0.016		No	Yes	1	No	Micropower, Programmable Delay	10-101
TL7702A	pgm	pgm	2	3	3.6	No	Yes	1	No	Programmable Delay	10-91
TL7702B	pgm	pgm	2	3	1	No	Yes	1	No	Programmable Delay	10-113
TLC7701	adj	1.1	5.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10-9

POWER DISTRIBUTION SWITCHES SELECTION GUIDE

GENERAL PURPOSE DISTRIBUTION SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (m Ω)	I_O (max) (A)	Current Limit (typ) (A)	V_{IN} Range (typ) (V)	Over Current Reporting	Over Temp Protection	Enable	Description	Page No.
TPS2010	1	75	0.2	0.4	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-25
TPS2010A	1	30	0.2	0.3	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-53
TPS2011	1	75	0.6	1.2	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-25
TPS2011A	1	30	0.6	0.9	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-53
TPS2012	1	75	1	2	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-25
TPS2012A	1	30	1	1.5	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-53
TPS2013	1	75	1.5	2.6	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-25
TPS2013A	1	30	1.5	2.2	2.7 - 5.5	No	Yes	Neg	Current-Limited	13-53

VAUX SWITCHES

Device	Number of Inputs	$r_{DS(on)}$ (typ) (m Ω)	$r_{DS(on)}$ (typ) (Ω)	IN1 Output Current (mA)	IN2 Output Current (mA)	IN1 Supply Current (typ) (μ A)	IN2 Supply Current (typ) (μ A)	IN1, IN2 Input Voltage Range (V)	Enable	Page No.
TPS2100	2	250	1.3	500	10	10	0.75	2.7 - 4.0	Neg	13-311
TPS2101	2	250	1.3	500	10	10	0.75	2.7 - 4.0	Pos	13-311

PCMCIA/CARDBUS DISTRIBUTION SWITCHES

Device	12-V Supply Required	3V/5V $r_{DS(on)}$ (typ) (m Ω)	Control Inputs	Current and Temperature Protection	VPP Good and OC Reporting	Description	Page No.
TPS2205	No	110/140	8 Line Parallel	Yes	N/Y	Dual Channel	13-325
TPS2206	No	110/140	3 Line Serial w/Reset	Yes	N/Y	Dual Channel	13-349
TPS2211	No	50	4 Line Parallel	Yes	N/Y	Single Channel	13-375
TPS2212	No	160	4 Line Parallel	Yes	N/Y	Single Channel	13-395
TPS2214	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13-413
TPS2216	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13-437

USB SWITCHES

Device	Number of FETs	r _{DS(on)} (typ) (mΩ)	I _O (max) (A)	Current Limit (typ) (A)	V _{IN} Range (typ) (V)	Over Current Reporting	Over Temp Reporting	Enable	Description	Page No.
TPS2014	1	95	0.6	1.2	4.0–5.5	Yes	No	Neg	Current-Limited, UL Listed, USB	13-73
TPS2015	1	95	1	2	4.0–5.5	Yes	No	Neg	Current-Limited, USB	13-73
TPS2020	1		0.2	0.3	2.7–5.5	Yes	Yes	Neg	Current-Limited, USB	13-93
TPS2021	1		0.6	0.9	2.7–5.5	Yes	Yes	Neg	Current-Limited, USB	13-93
TPS2022	1		1	1.5	2.7–5.5	Yes	Yes	Neg	Current-Limited, USB	13-93
TPS2023	1		1.5	2.2	2.7–5.5	Yes	Yes	Neg	Current-Limited, USB	13-93
TPS2024	1		2	3	2.7–5.5	Yes	Yes	Neg	Current-Limited, USB	13-93
TPS2030	1	30	0.2	0.3	2.7–5.5	Yes	Yes	Pos	Current-Limited, USB	13-115
TPS2031	1	30	0.6	0.9	2.7–5.5	Yes	Yes	Pos	Current-Limited, USB	13-115
TPS2032	1	30	1	1.5	2.7–5.5	Yes	Yes	Pos	Current-Limited, USB	13-115
TPS2033	1	30	1.5	2.2	2.7–5.5	Yes	Yes	Pos	Current-Limited, USB	13-115
TPS2034	1	30	2	3	2.7–5.5	Yes	Yes	Pos	Current-Limited, USB	13-115
TPS2041	1	80	0.5	0.9	2.7–5.5	Yes	Yes	Neg	Current-Limited, Nemko Recognized	13-137
TPS2042	2	80	0.5	0.9	2.7–5.5	Each	Yes	Neg	Current-Limited, Nemko Recognized	13-157
TPS2043	3	80	0.5	0.9	2.7–5.5	Each	Yes	Neg	Current-Limited, Nemko Recognized	13-179
TPS2044	4	80	0.5	0.9	2.7–5.5	Each	Yes	Neg	Current-Limited, Nemko Recognized	13-203
TPS2045	1	80	0.25	0.44	2.7–5.5	Yes	Yes	Neg	Current-Limited, Nemko Recognized	13-227
TPS2046	2	80	0.25	0.44	2.7–5.5	Yes	Yes	Neg	Current-Limited, Nemko Recognized	13-247
TPS2047	3	80	0.25	0.44	2.7–5.5	Yes	Yes	Neg	Current-Limited, Nemko Recognized	13-267
TPS2048	4	80	0.25	0.44	2.7–5.5	Yes	Yes	Neg	Current-Limited, Nemko Recognized	13-289
TPS2051	1	80	0.5	0.9	2.7–5.5	Yes	Yes	Pos	Current-Limited, Nemko Recognized	13-137
TPS2052	2	80	0.5	0.9	2.7–5.5	Each	Yes	Pos	Current-Limited, Nemko Recognized	13-157
TPS2053	3	80	0.5	0.9	2.7–5.5	Each	Yes	Pos	Current-Limited, Nemko Recognized	13-179
TPS2054	4	80	0.5	0.9	2.7–5.5	Each	Yes	Pos	Current-Limited, Nemko Recognized	13-203
TPS2055	1	80	0.25	0.44	2.7–5.5	Yes	Yes	Pos	Current-Limited, Nemko Recognized	13-227
TPS2056	2	80	0.25	0.44	2.7–5.5	Yes	Yes	Pos	Current-Limited, Nemko Recognized	13-247
TPS2057	3	80	0.25	0.44	2.7–5.5	Yes	Yes	Pos	Current-Limited, Nemko Recognized	13-267
TPS2058	4	80	0.25	0.44	2.7–5.5	Yes	Yes	Pos	Current-Limited, Nemko Recognized	13-289



POWER DISTRIBUTION SWITCHES SELECTION GUIDE

PMOS DISTRIBUTION SWITCHES

Device	Number of FETs	rDS(on) (typ) (mΩ)	VDS (max) (V)	IDD (max) (A)	ESD Circuitry	Description	Page No.
TPS1100	1	180	15	1.6	Yes	High-Side PMOS	13-3
TPS1101	1	90	15	2.3	Yes	High-Side PMOS	13-13
TPS1120	2	180	15	1.17	Yes	High-Side PMOS	13-23

LED DRIVERS

Device	V _{ref} (V)	I _Z (min) (μ A)	I _Z (max) (mA)	V _O (min) (V)	V _O (max) (V)	Tolerance (%)	V _I (max) (V)	Temp Coeff (typ) (ppm/ $^{\circ}$ C)	Description	Page No.
TLC5904	2.5	1000	100	V _{ref}	36	0.4	36	30	LED Driver	14-3

VOLTAGE RAIL SPLITTERS

Device	I _{CC} (μ A)	V _{CC} (V)	I _O (mA)	V _O (min) (V)	V _O (max) (V)	Temp Coeff (typ) (ppm/ $^{\circ}$ C)	Description	Page No.
TLE2426	280	4 - 40	20	1.98	20.2	25	Rail Splitter Precision Virtual Ground	15-3

SPECIAL FUNCTIONS

Device	V _{ref} (V)	I _Z (min) (μ A)	I _Z (max) (μ A)	V _O (min) (V)	Input Clamp Current (mA)	Settling Time (μ s)	Description	Page No.
TL7726	4.5		60		25	30	Hex Clamping Circuit	16-3
TL2218-285		-20.5		2.5			Excalibur Current-Mode SCSI Terminator	16-7



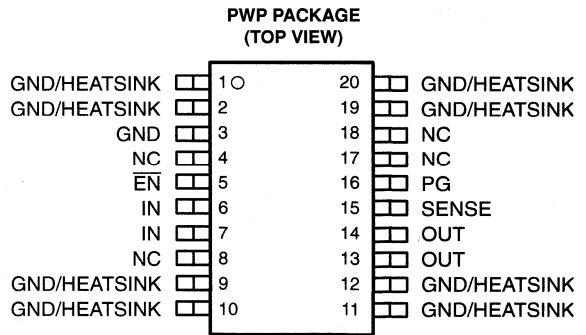
General Information (Vol. 1)	1
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2 Linear Voltage Regulators

TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS101A – FEBRUARY 1995 – REVISED AUGUST 1995

- Thermally Enhanced Surface-Mount Package (PWP)
- High-Current (500-mA) LDO Regulator
- Very Low-Dropout Voltage . . . Maximum of 60 mV at $I_O = 100$ mA
- Extremely Low Sleep-State Current 0.5 μ A Max
- 2% Output-Voltage Tolerance Over Full Range of Load, Line, and Temperature
- Output Current Range of 0 mA to 500 mA
- Power Good (PG) Status Output



NC – No internal connection

description

The TPS7133QPWP is a micropower low-dropout (LDO) voltage regulator with a fixed 3.3-V output voltage, rated for loads up to 500 mA. The device is ideal for applications that require 3.3 V from a 5-V supply, or a constant output from a battery, such as alkaline or lithium ion, that drops off considerably in voltage as it discharges.

To maximize the advantage of its high-output-current capability, the TPS7133QPWP is now offered in a new thermally enhanced surface-mount power package. Designed to the same dimensions as the 20-pin TSSOP (just 1.2 mm high), the part has an innovative thermal pad, which, when soldered to the printed-wiring board (PWB), enables the device to dissipate several watts of power (see Figure 1 and Thermal Information section).

Using a PMOS transistor as the pass element keeps the quiescent current very low and constant, independent of output loading (typically 270 μ A over the full range of output current, 0 mA to 500 mA). Because the PMOS device also behaves as a low-value resistor, the dropout is very low – maximum of 60 mV at 100 mA. These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO also features a sleep mode; applying a TTL high signal to \overline{EN} shuts down the regulator, reducing the quiescent current to 0.5 μ A.

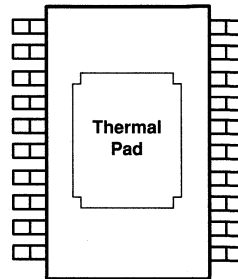


Figure 1. Bottom View of PWP Package, Showing the Thermal Pad

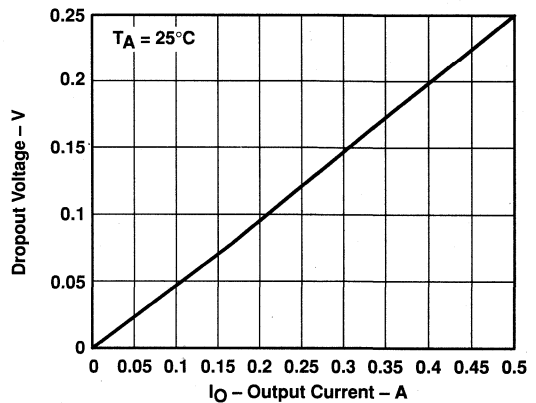


Figure 2. Typical Dropout Voltage Versus Output Current

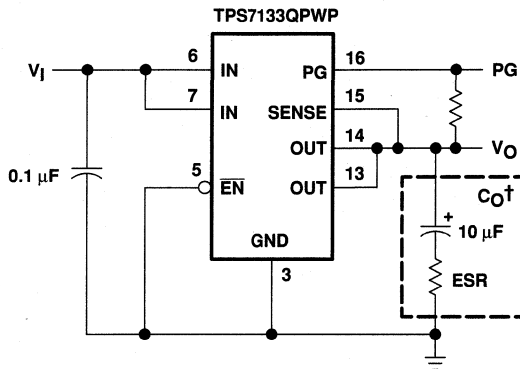
TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS101A – FEBRUARY 1995 – REVISED AUGUST 1995

AVAILABLE OPTIONS†

T _J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES	CHIP FORM (Y)
	MIN	TYP	MAX	THERMALLY-ENHANCED TSSOP (PWP)	
-55°C to 150°C	3.23	3.3	3.37	TPS7133QPWPPWPLE	TPS7133Y

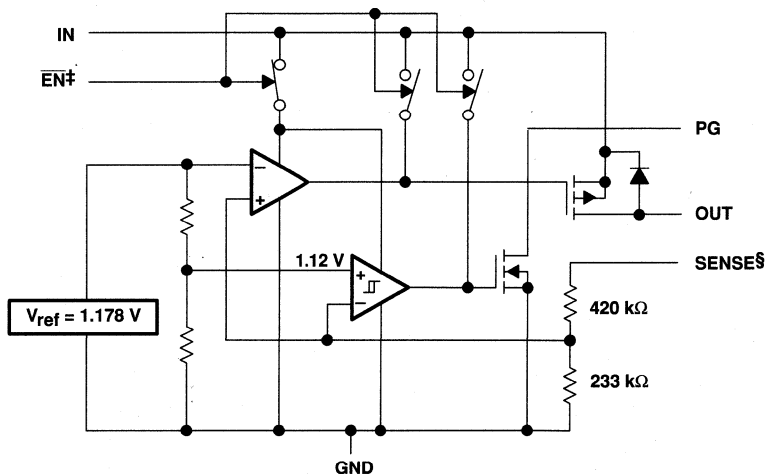
† The PWP package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS7133QPWPLE). The chip form is tested at 25°C.



† Capacitor selection is nontrivial. See application information section for details.

Figure 3. Typical Application Configuration

functional block diagram



Resistors are nominal values only.

‡ Switch positions shown with $\overline{\text{EN}}$ active low.

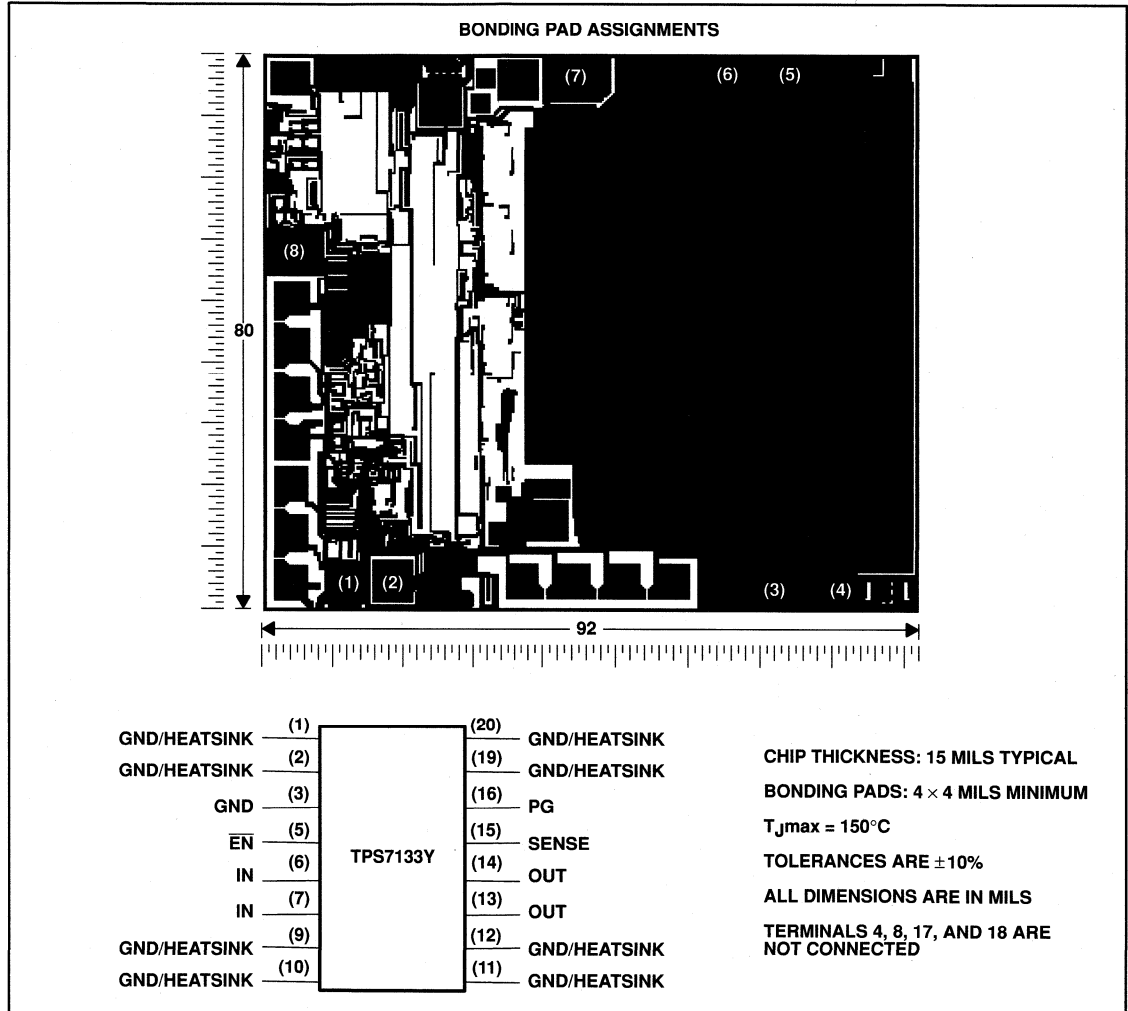
§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

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TPS7133Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS7133QPWP. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I , PG, SENSE, \overline{EN}	–0.3 to 10 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 4)§

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 5)§

PACKAGE	$T_C \leq 62.5^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	7.1 W

MAXIMUM CONTINUOUS DISSIPATION§
vs
FREE-AIR TEMPERATURE

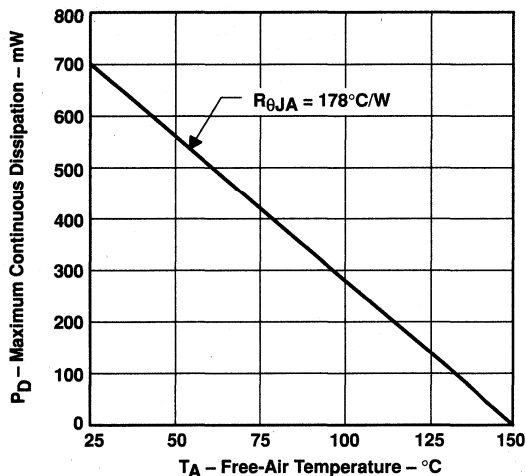


Figure 4

MAXIMUM CONTINUOUS DISSIPATION§
vs
CASE TEMPERATURE

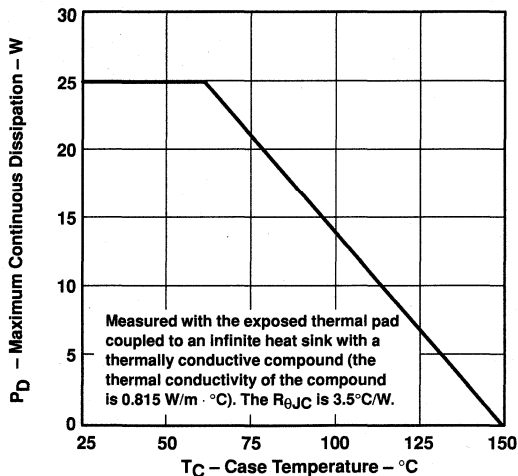


Figure 5

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

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recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I [†]	3.77	10	V
High-level input voltage at \overline{EN} , V_{IH}	2		V
Low-level input voltage at \overline{EN} , V_{IL}		0.5	V
Output current range, I_O	0	500	mA
Operating virtual junction temperature range, T_J	-40	125	°C

[†] Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage V_{DO} [‡] at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

[‡] This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

electrical characteristics at $I_O = 10 \text{ mA}$, $\overline{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F/ESR}^\S = 1 \Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS [§]	T_J	TPS7133QPWP			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5 \text{ V}$, $0 \leq I_O \leq 500 \text{ mA}$	$V_I = V_O + 1 \text{ V}$, 25°C	285	350		μA
		-40°C to 125°C		460		
Input current (standby mode)	$\overline{EN} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C		0.5		μA
		-40°C to 125°C		2		
Output current limit	$V_O = 0$, $V_I = 10 \text{ V}$	25°C	1.2	2		A
		-40°C to 125°C		2		
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C		0.5		μA
		-40°C to 125°C		1		
PG leakage current	Normal operation, $V_{PG} = 10 \text{ V}$	25°C	0.02	0.5		μA
		-40°C to 125°C		0.5		
Output voltage temperature coefficient		-40°C to 125°C	61	75		ppm/°C
Thermal shutdown junction temperature				165		°C
\overline{EN} logic high (standby mode)	$2.5 \text{ V} \leq V_I \leq 6 \text{ V}$ $6 \text{ V} \leq V_I \leq 10 \text{ V}$	-40°C to 125°C	2			V
			2.7			
\overline{EN} logic low (active mode)	$2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C		0.5		V
		-40°C to 125°C		0.5		
\overline{EN} hysteresis voltage		25°C		50		mV
\overline{EN} input current	$0 \leq V_I \leq 10 \text{ V}$	25°C	-0.5	0.5		μA
		-40°C to 125°C	-0.5	0.5		
Minimum V_I for active pass element		25°C	2.05	2.5		V
		-40°C to 125°C		2.5		
Minimum V_I for valid PG	$I_{PG} = 300 \mu\text{A}$	25°C	1.06	1.5		V
		-40°C to 125°C		1.9		

[§] ESR refers to the equivalent series resistance, including internal and external resistance.

[¶] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



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electrical characteristics at $I_O = 10 \text{ mA}$, $V_I = 4.3 \text{ V}$, $\overline{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}/\text{ESR}^\dagger = 1 \Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONST		T _J	TPS7133QPWP			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4.3 \text{ V}$,	$I_O = 10 \text{ mA}$	25°C	3.3			V
	$4.3 \text{ V} \leq V_I \leq 10 \text{ V}$,	$5 \text{ mA} \leq I_O \leq 500 \text{ mA}$	-40°C to 125°C	3.23	3.37		
Dropout voltage	$I_O = 10 \text{ mA}$,	$V_I = 3.23 \text{ V}$	25°C	0.02		6	mV
			-40°C to 125°C			8	
	$I_O = 100 \text{ mA}$,	$V_I = 3.23 \text{ V}$	25°C	47		60	
			-40°C to 125°C			80	
	$I_O = 500 \text{ mA}$,	$V_I = 3.23 \text{ V}$	25°C	235		300	
			-40°C to 125°C			400	
Pass-element series resistance	$(3.23 \text{ V} - V_O)/I_O$,	$V_I = 3.23 \text{ V}$,	25°C	0.47	0.6		Ω
			$I_O = 500 \text{ mA}$	-40°C to 125°C	0.8		
Input voltage regulation	$V_I = 4.3 \text{ V}$ to 10 V,	$50 \mu\text{A} \leq I_O \leq 500 \text{ mA}$	25°C	20		mV	
			-40°C to 125°C	27			
Output voltage regulation	$I_O = 5 \text{ mA}$ to 500 mA,	$4.3 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C	21	38		mV
			-40°C to 125°C	75			
	$I_O = 50 \mu\text{A}$ to 500 mA,	$4.3 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C	30	60		mV
			-40°C to 125°C	120			
Ripple rejection	$f = 120 \text{ Hz}$	$I_O = 50 \mu\text{A}$	25°C	43	54		dB
			-40°C to 125°C	40			
		$I_O = 500 \text{ mA}$	25°C	39	49		
			-40°C to 125°C	36			
Output noise-spectral density	$f = 120 \text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10 \text{ Hz} \leq f \leq 100 \text{ kHz}$,	$C_O = 4.7 \mu\text{F}$	25°C	274		μV_{rms}	
		$C_O = 10 \mu\text{F}$	25°C	228			
		$C_O = 100 \mu\text{F}$	25°C	159			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	$0.92 \times V_{\text{O(nom)}}$	$0.98 \times V_{\text{O(nom)}}$		V
PG hysteresis voltage			25°C	35		mV	
PG output low voltage	$I_{\text{PG}} = 1 \text{ mA}$,	$V_I = 2.8 \text{ V}$	25°C	0.22	0.4		V
			-40°C to 125°C	0.4			

† ESR refers to the equivalent series resistance, including internal and external resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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electrical characteristics at $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\ \mu\text{F}/\text{ESR}^\ddagger = 1\ \Omega$, $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	TPS7133Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5\text{ V}$, $0 \leq I_O \leq 500\text{ mA}$	$V_I = V_O + 1\text{ V}$, 285			μA
Output current limit	$V_O = 0$,	$V_I = 10\text{ V}$, 1.2			A
PG leakage current	Normal operation,	$V_{PG} = 10\text{ V}$, 0.02			μA
Thermal shutdown junction temperature		165			$^\circ\text{C}$
\overline{EN} hysteresis voltage		50			mV
Minimum V_I for active pass element		2.05			V
Minimum V_I for valid PG	$I_{PG} = 300\ \mu\text{A}$	1.06			V

§ ESR refers to the equivalent series resistance, including internal and external resistance.

¶ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\ \mu\text{F}/\text{ESR}^\ddagger = 1\ \Omega$, $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TPS7133Y			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$, $I_O = 10\text{ mA}$	3.3			V
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 3.23\text{ V}$	0.02			mV
	$I_O = 100\text{ mA}$, $V_I = 3.23\text{ V}$	47			
	$I_O = 500\text{ mA}$, $V_I = 3.23\text{ V}$	235			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 3.23\text{ V}$, 0.47			Ω
Output voltage regulation	$I_O = 5\text{ mA to } 500\text{ mA}$, $4.3\text{ V} \leq V_I \leq 10\text{ V}$	21			mV
	$I_O = 50\ \mu\text{A to } 500\text{ mA}$, $4.3\text{ V} \leq V_I \leq 10\text{ V}$	30			mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\ \mu\text{A}$, 54			dB
		$I_O = 500\text{ mA}$, 49			
Output noise-spectral density	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	10 Hz \leq f \leq 100 kHz, ESR $^\ddagger = 1\ \Omega$	$C_O = 4.7\ \mu\text{F}$, 274			μVrms
		$C_O = 10\ \mu\text{F}$, 228			
		$C_O = 100\ \mu\text{F}$, 159			
PG hysteresis voltage		35			mV
PG output low voltage	$I_{PG} = 1\text{ mA}$, $V_I = 2.8\text{ V}$	0.22			V

† ESR refers to the equivalent series resistance, including internal and external resistance.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	6
		vs Input voltage	7
		vs Free-air temperature	8
V_{DO}	Typical dropout voltage	vs Output current	9
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	10
ΔV_O	Change in output voltage	vs Free-air temperature	11
V_O	Output voltage	vs Input voltage	12
ΔV_O	Change in output voltage	vs Input voltage	13
V_O	Output voltage	vs Output current	14
	Ripple rejection	vs Frequency	15
	Output special noise density	vs Frequency	16
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	17
R	Divider resistance	vs Free-air temperature	18
$I_{I(SENSE)}$	SENSE pin current	vs Free-air temperature	19
V_I	Minimum input voltage (active-pass element)	vs Free-air temperature	20
	Minimum input voltage (valid PG)	vs Free-air temperature	21
$I_{I(EN)}$	\overline{EN} Input current	vs Free-air temperature	22
	Output voltage response from Enable (\overline{EN})		23
V_{PG}	Power-good (PG) voltage	vs Output voltage	24
	Total ESR	vs Output current	25
			26
	Total ESR	vs Added ceramic capacitance	27
			28
	Total ESR	vs Output current	29
			30
	Total ESR	vs Added ceramic capacitance	31
			32

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TYPICAL CHARACTERISTICS

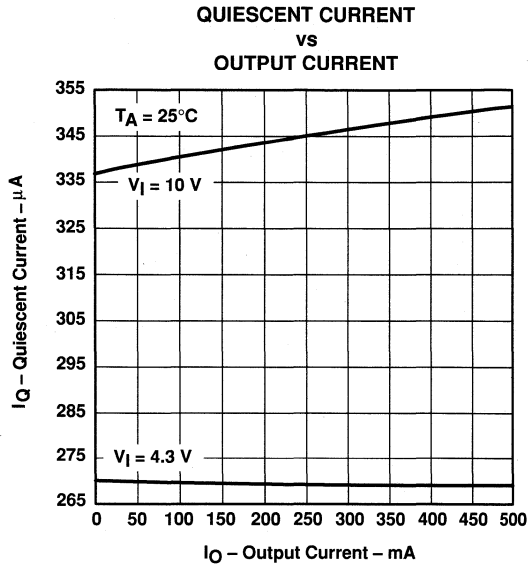


Figure 6

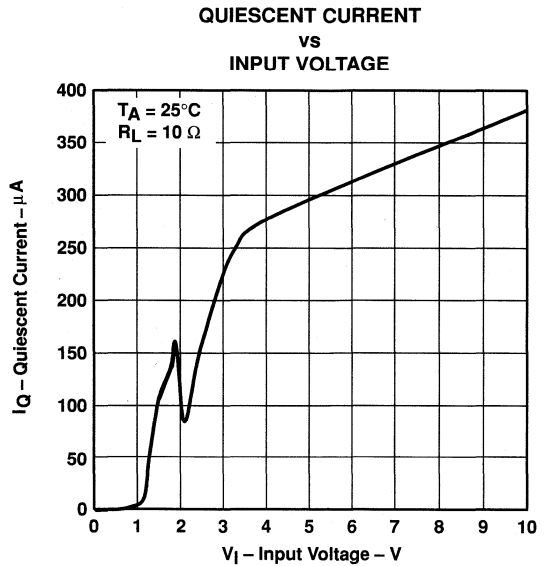


Figure 7

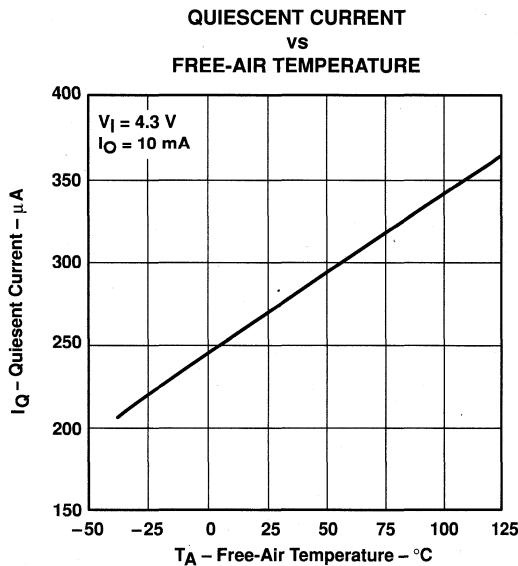


Figure 8

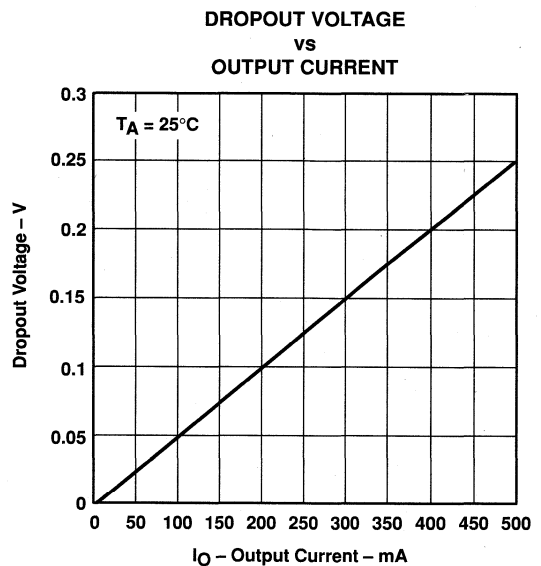


Figure 9

TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

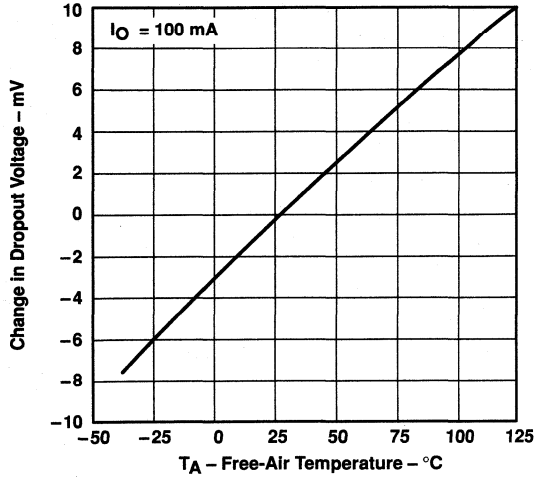


Figure 10

CHANGE IN OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

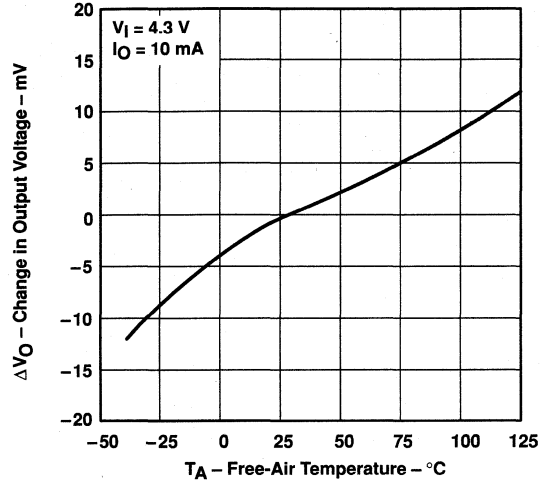


Figure 11

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

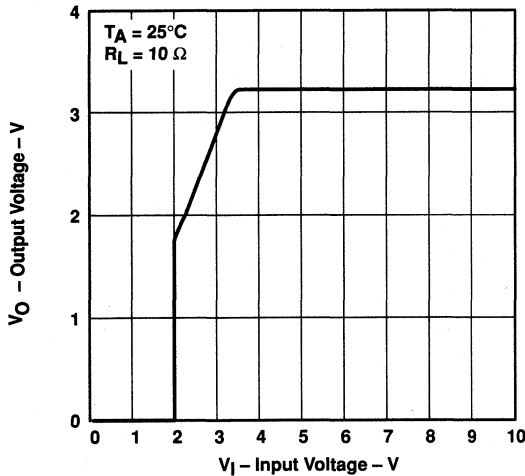


Figure 12

CHANGE IN OUTPUT VOLTAGE
vs
INPUT VOLTAGE

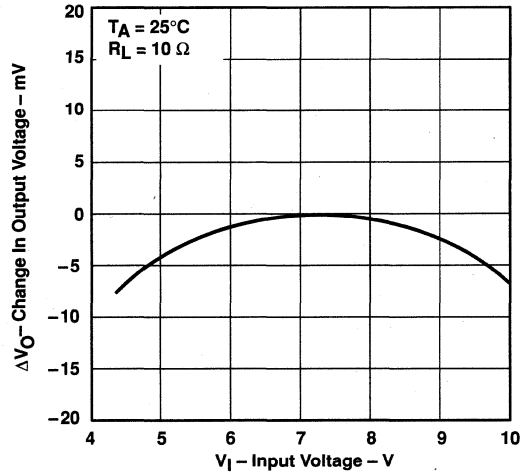
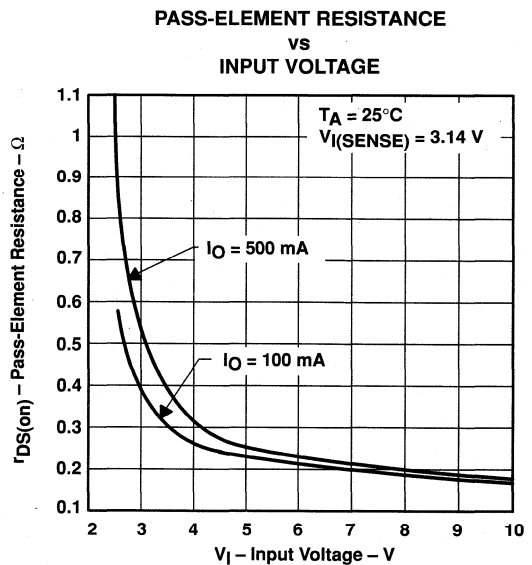
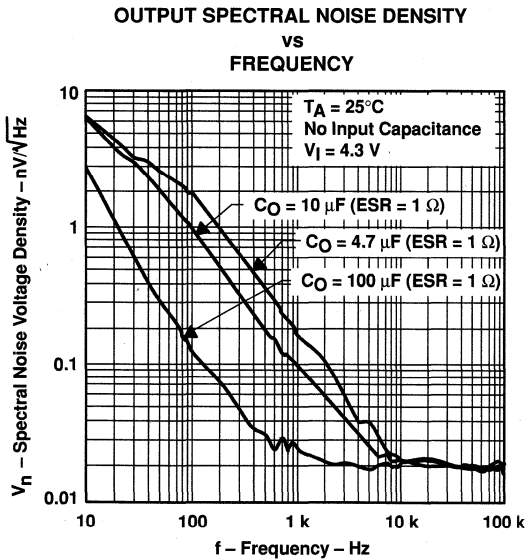
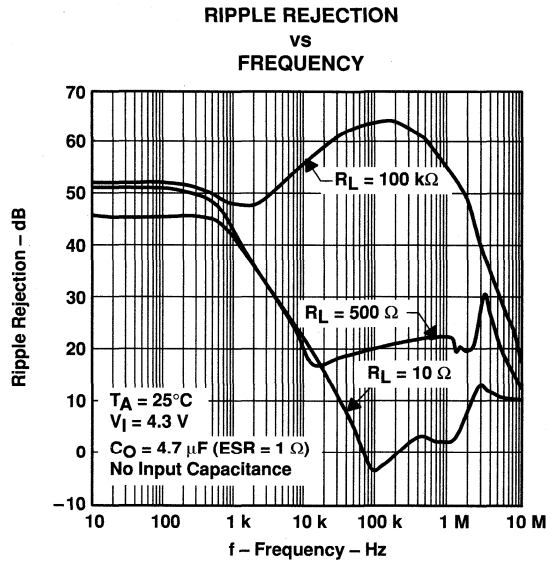
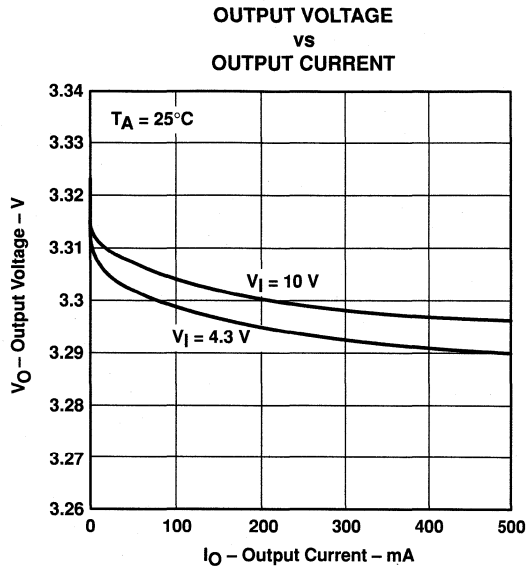


Figure 13

TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

**DIVIDER RESISTANCE
vs
FREE-AIR TEMPERATURE**

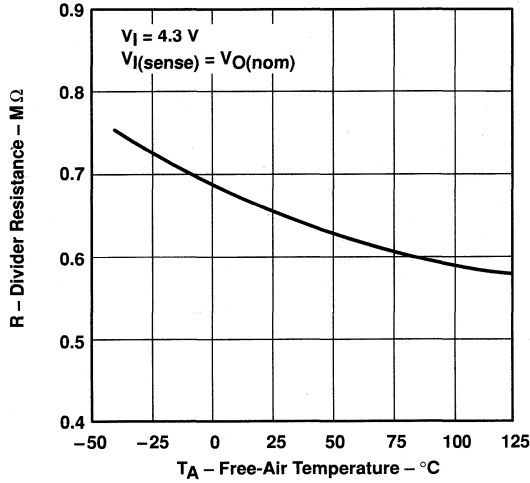


Figure 18

**SENSE PIN CURRENT
vs
FREE-AIR TEMPERATURE**

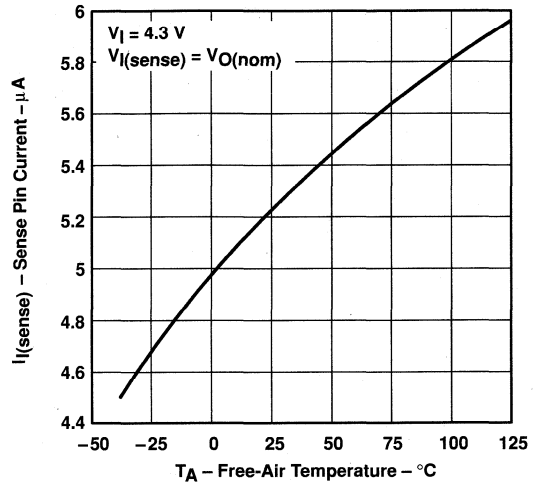


Figure 19

**MINIMUM INPUT VOLTAGE
(ACTIVE PASS ELEMENT)
vs
FREE-AIR TEMPERATURE**

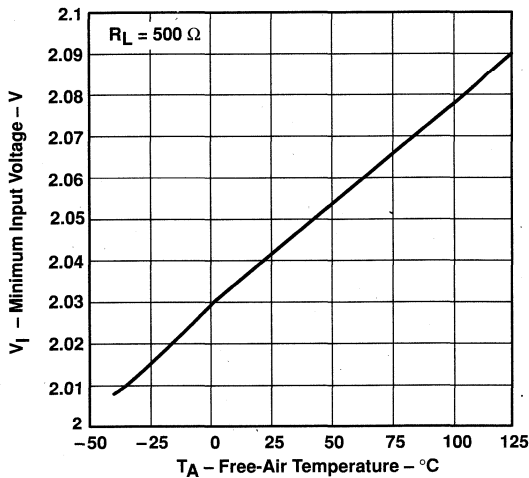


Figure 20

**MINIMUM INPUT VOLTAGE
(VALID PG)
vs
FREE-AIR TEMPERATURE**

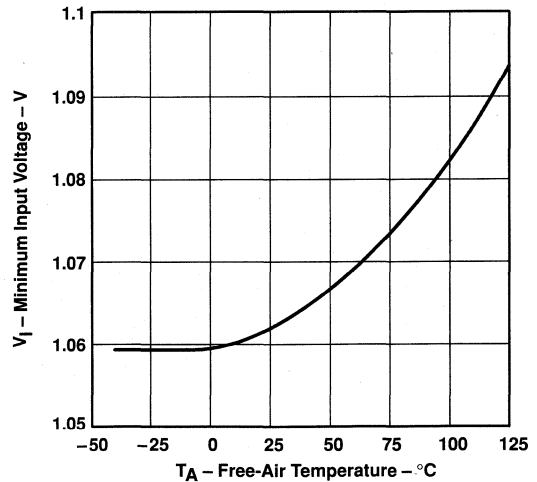


Figure 21

TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**$\overline{\text{EN}}$ INPUT CURRENT
vs
FREE-AIR TEMPERATURE**

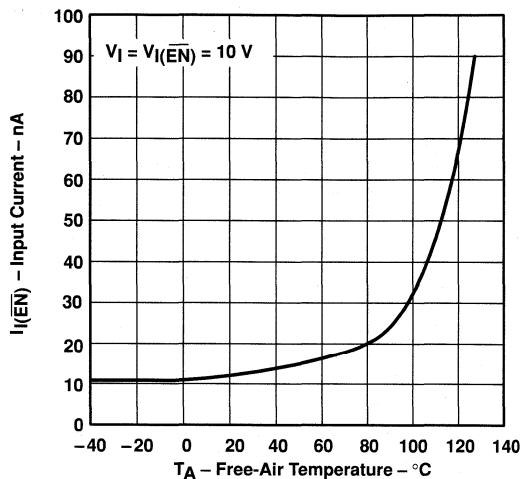


Figure 22

**OUTPUT VOLTAGE RESPONSE FROM
ENABLE ($\overline{\text{EN}}$)**

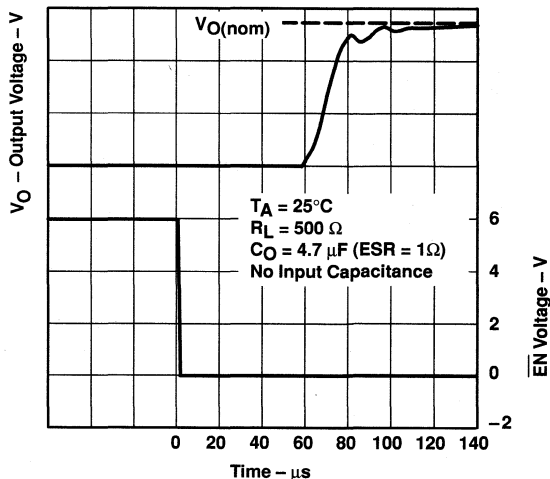


Figure 23

**POWER-GOOD (PG) VOLTAGE
vs
OUTPUT VOLTAGE**

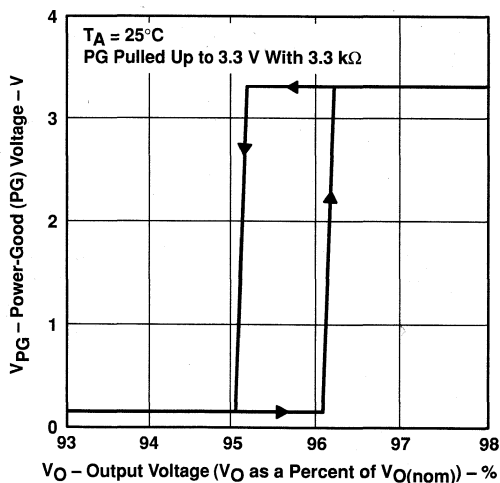


Figure 24

**TPS7133QPWP, TPS7133Y
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TYPICAL CHARACTERISTICS

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT**

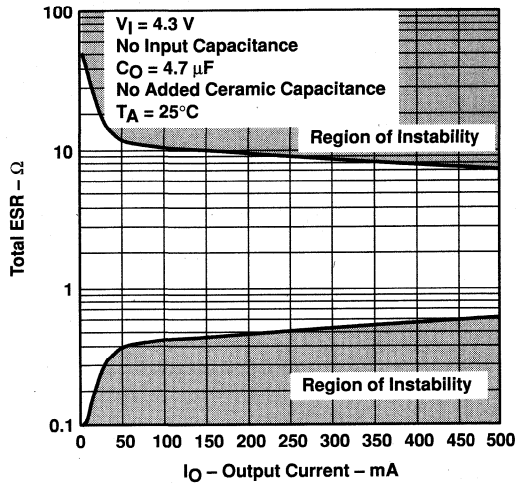


Figure 25

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT**

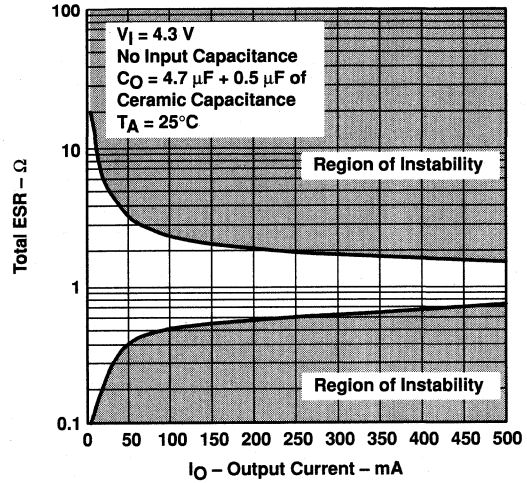


Figure 26

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE**

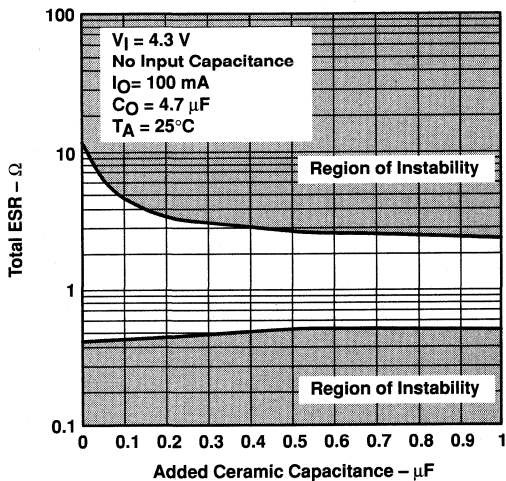


Figure 27

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE**

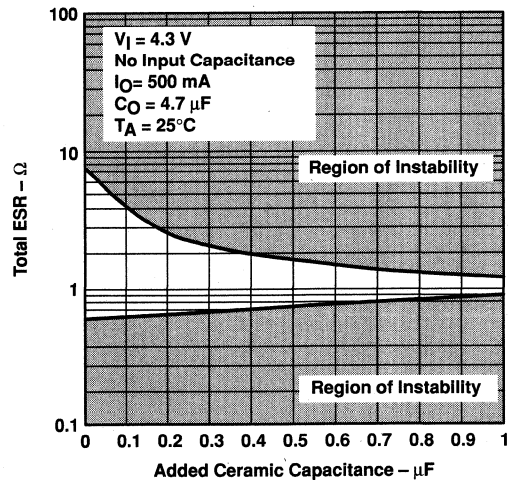


Figure 28



TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

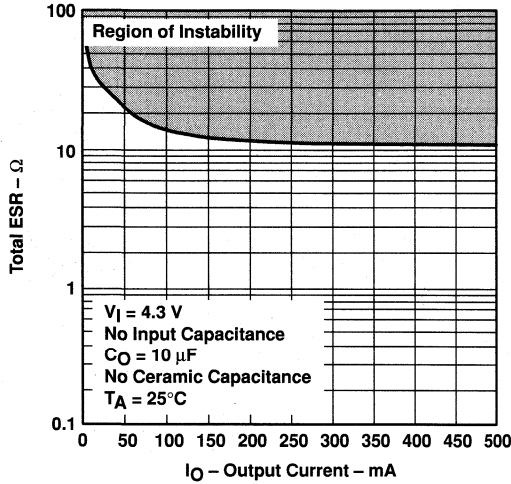


Figure 29

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

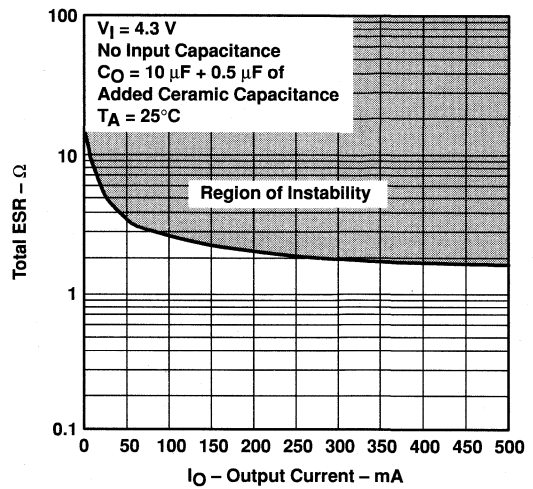


Figure 30

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

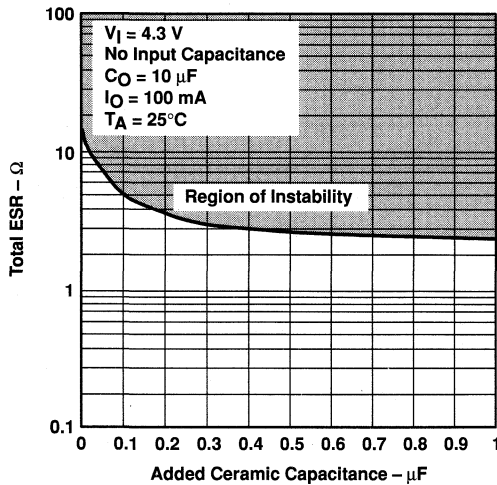


Figure 31

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

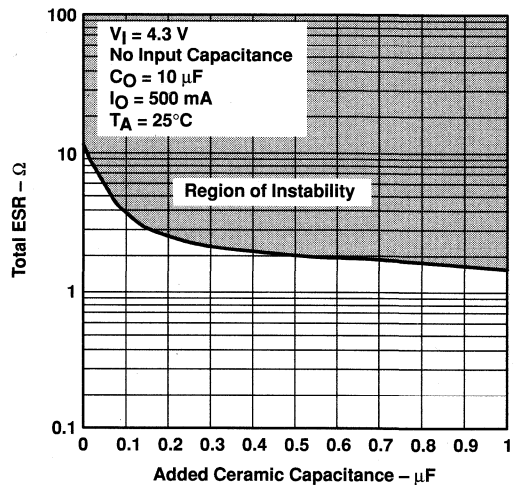


Figure 32

† ESR values below 0.1 Ω are not recommended.

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TYPICAL CHARACTERISTICS

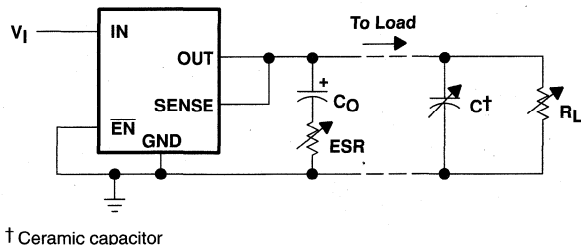


Figure 33. Test Circuit for Typical Regions of Stability (Figures 25 through 32)

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 34(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

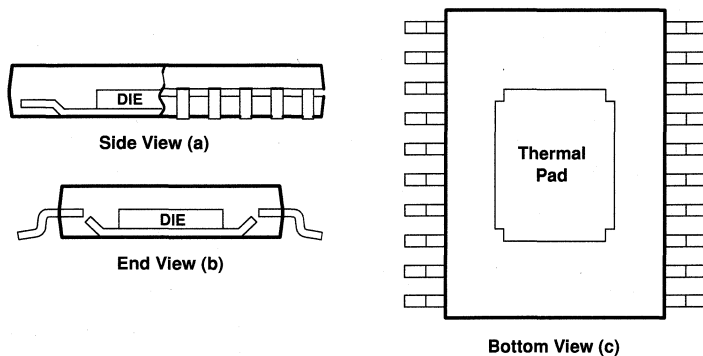


Figure 34. Views of Thermally Enhanced PWP Package

TPS7133QPWP, TPS7133Y MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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THERMAL INFORMATION

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 36(a), 8 cm² of Cu heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 35 and 36). The line drawn at 0.3 cm² in Figures 35 and 36 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 38.

The thermal pad is directly connected to the substrate of the IC, which for the TPS7133QPWP is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWB can be a ground plane or left electrically isolated. In other TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 12 independent leads that can be used as inputs and outputs (Note: leads 1, 2, 9, 10, 11, 12, 19, and 20 are internally connected to the thermal pad and the IC substrate).

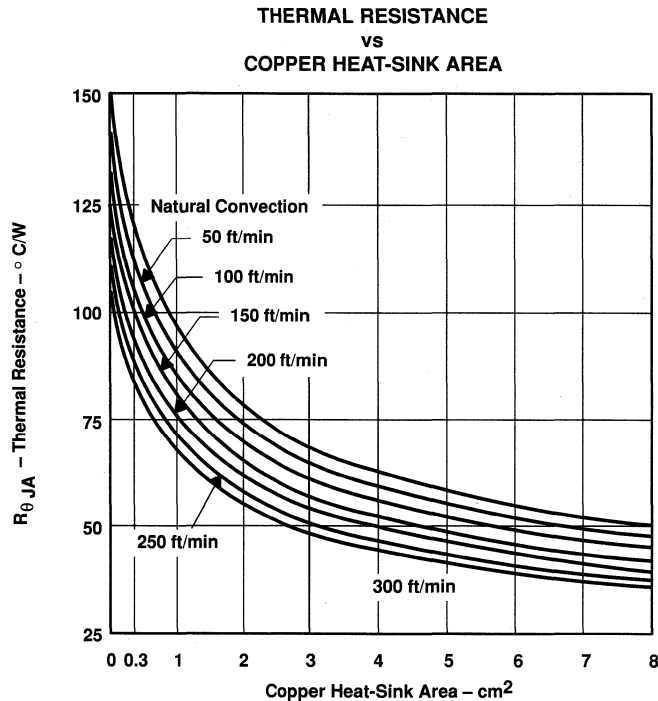
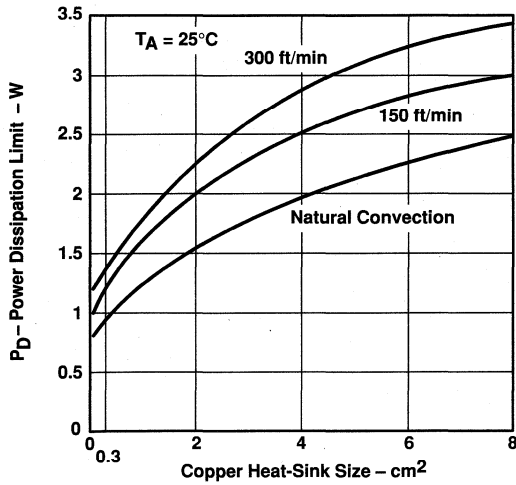


Figure 35

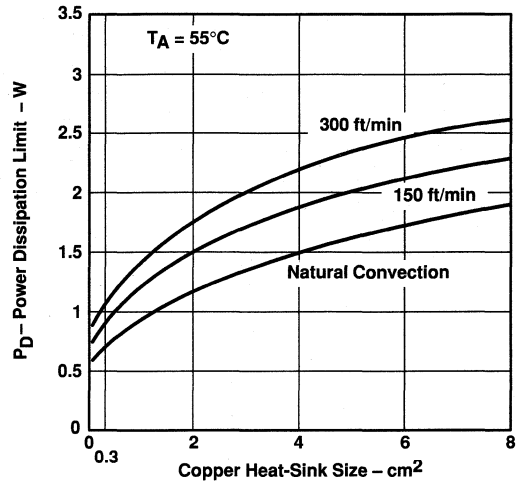
**TPS7133QPWP, TPS7133Y
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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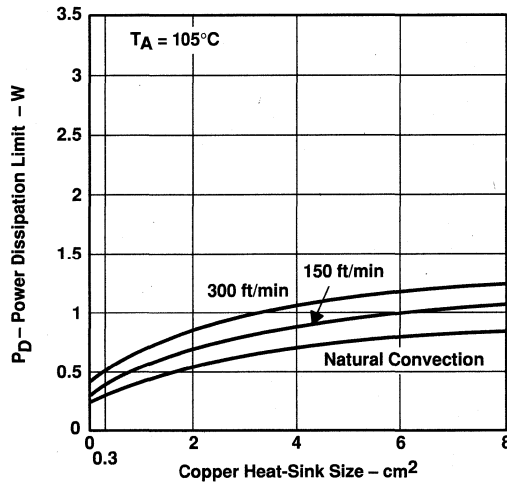
THERMAL INFORMATION



(a)



(b)



(c)

Figure 36. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

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THERMAL INFORMATION

Figure 37 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figures 35 and 36. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 35 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.

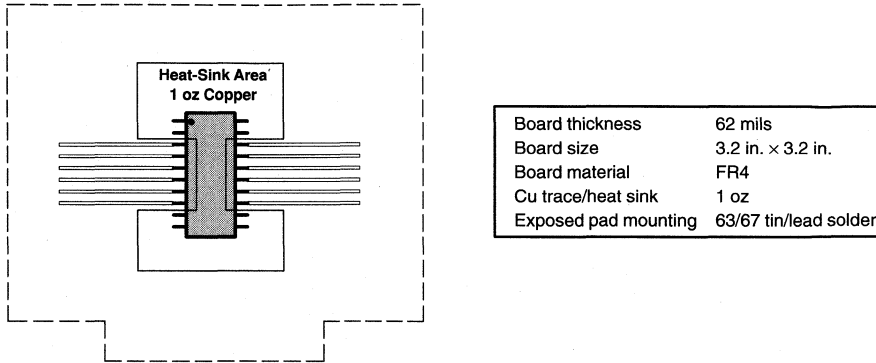


Figure 37. PWB Layout (Including Cu Heatsink Area) for Thermally Enhanced PWP Package

From Figure 35, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}}$$

Where

T_{Jmax} is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS7133QPWP regulator. The equation for calculating total internal power dissipation of the TPS7133QPWP is:

$$P_{D(total)} = (V_I - V_O) \cdot I_O + V_I \cdot I_Q$$

Since the quiescent current of the TPS7133QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \cdot I_O$$

For the case where $T_A = 55^\circ\text{C}$, airflow = 200 ft/min, copper heat-sink area = 4 cm², the maximum power-dissipation limit can be calculated. First, from Figure 35, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{50^\circ\text{C/W}} = 1.4 \text{ W}$$

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If the system implements a TPS7133QPWP regulator, where $V_I = 6\text{ V}$ and $I_O = 500\text{ mA}$, the internal power dissipation is:

$$P_{D(\text{total})} = (V_I - V_O) \cdot I_O = (6 - 3.3) \cdot 0.5 = 1.35\text{ W}$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

Since the thermal pad is not a primary connection for an electrical signal, the importance of the electrical connection is not significant. The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 35 and 36 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 38 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 2, 9, 10, 11, 12, 19, and 20.

reliability information

This section includes demonstrated reliability test results obtained from the qualification program. Accelerated tests are performed at high-stress conditions so that product reliability can be established during a relatively short test duration. Specific stress conditions are chosen to represent accelerated versions of various device-application environments and allow meaningful extrapolation to normal operating conditions.

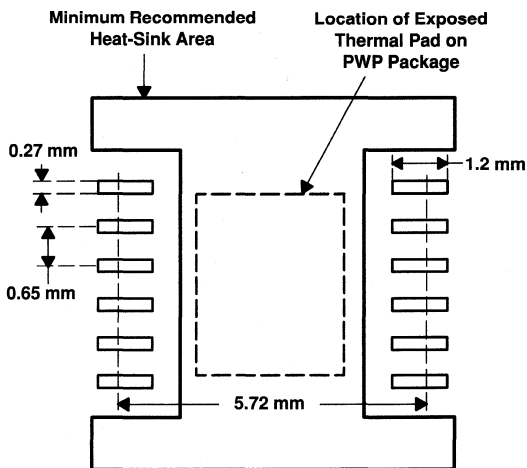


Figure 38. PWP Package Land Pattern

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THERMAL INFORMATION

component level reliability test results

preconditioning

Preconditioning of components prior to reliability testing is employed to simulate the actual board assembly process used by the customer. This ensures that reliability test results are more representative of those that would be seen in the final application. The general form of the preconditioning sequence includes a moisture soak followed by multiple vapor-phase-reflow or infrared-reflow solder exposures. All components used in the following reliability tests were preconditioned in accordance with JEDEC Test Method A113 for Level 1 (not moisture-sensitive) products.

high-temperature life test

High-temperature life testing is used to demonstrate long-term reliability of the product under bias. The potential failure mechanisms evaluated with this stress are those associated with dielectric integrity and design or process sensitivity to mobile-ion phenomena. Components are tested at an elevated ambient temperature of 155°C for an extended period. Results are derated using the Arrhenius equation to an equivalent number of unit hours at a representative application temperature. The corresponding predicted failure rate is expressed in FITs, or failures per billion device-hours. The failure rate shown in this case is data-limited since no actual failures were experienced during qualification testing.

PREDICTED LONG-TERM FAILURE RATE		
Number of Units	Equivalent Unit Hours at 55°C and 0.7 eV	FITs at 50% CL
325	24,468,090	36.2

biased humidity test

Biased humidity testing is used to evaluate the effects of moisture penetration on plastic-encapsulated devices under bias. This stress verifies the integrity of the package construction and the die passivation system. The primary potential failure mechanism is electrolytic corrosion. Components are biased in a low power state to reduce heat dissipation and are subjected to a 120°C, 85%-relative-humidity environment for 100 hours.

BIASED HUMIDITY TEST RESULTS	
Equivalent Unit Hours at 85°C and 85% RH	Failures
357,000	0

autoclave test

The autoclave stress is used to assess the capabilities of the die and package construction materials with respect to moisture ingress and extended exposure. Predominant failure mechanisms include leakage currents that result from internal moisture accumulation and galvanic corrosion resulting from reactions with any present ionic contaminants. Components are subjected to a 121°C, 15 PSIG, 100%-relative-humidity environment for 240 hours.

AUTOCLAVE TEST RESULTS	
Total Unit Hours	Failures
54,720	0

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thermal shock test

Thermal shock testing is used to evaluate the capability of the component to withstand mechanical stress resulting from differences in thermal coefficients of expansion among the die and package construction materials. Failure mechanisms are typically related to physical damage at interface locations between different materials. Components are cycled between -65°C and 150°C in liquid mediums for a total duration of 1000 cycles.

THERMAL SHOCK TEST RESULTS	
Total Unit Cycles	Failures
345,000	0

PWB assembly level reliability results

temperature cycle test

Temperature cycle testing of the PWB assembly is used to evaluate the capability of the assembly to withstand mechanical stress resulting from the differences in thermal coefficients of expansion among die, package, and PWB board materials. This testing is also used to sufficiently age the soldered thermal connection between the thermal pad and the Cu trace on the FR4 board and evaluate the degradation of the thermal resistance for a board-mounted test unit. The assemblies were cycled between temperature extremes of -40°C and 125°C for a total duration of 730 cycles.

TEMPERATURE CYCLE TEST RESULTS		
Total Unit Cycles	Failures	Average Change in $R_{\theta\text{JA}}(\text{system})$
36,500	0	-0.41%

solderability test

Solderability testing is used to simulate actual board-mount performance in a reflow process.

Solderability testing is conducted as follows: The test devices are first steam-aged for 8 hours. A stencil is used to apply a solder-paste terminal pattern on a ceramic substrate (nominal stencil thickness is 0.005 inch). The test units are manually placed on the solder-paste footprint with proper implements to avoid contamination. The ceramic substrate and components are subjected to the IR reflow process as follows:

IR REFLOW PROCESS		
	PREHEAT SOAK	REFLOW
Temperature	150°C to 170°C	215°C to 230°C
Time	60 sec	60 sec

After cooling to room temperature, the component is removed from the ceramic substrate and the component terminals are subjected to visual inspection at 10X magnification.

Test results are acceptable if all terminations exhibit a continuous solder coating free of defects for a minimum 95% of the critical surface area of any individual termination. Causes for rejection include: dewetting, nonwetting, and pin holes. The component leads and the exposed thermal pad were evaluated against this criteria.

SOLDERABILITY TEST RESULTS	
Number of Test Units	Failures
22	0

X-ray test

X-ray testing is used to examine and quantify the voiding of the soldered attachment between the thermal pad and the PWB copper trace. Voiding between 20% and 50% was observed on a 49-piece sample.

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APPLICATION INFORMATION

The TPS7133QPWP low-dropout (LDO) regulator is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator.

device operation

The TPS7133QPWP, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent-current versus load-current curves. The TPS7133QPWP uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS7133QPWP specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS7133QPWP quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS7133QPWP also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under $2\ \mu\text{A}$. $\overline{\text{EN}}$ is pulled down internally, requiring no external connection for continuous operation. Response to an enable transition is quick; regulated output voltage is reestablished in typically $120\ \mu\text{s}$.

minimum load requirements

The TPS7133QPWP is stable even at zero load; no minimum load is required for operation.

sense-pin connection

The SENSE pin must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047-pF to 0.1- μF) improves load transient response and noise rejection if the TPS7133QPWP is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS7133QPWP requires an output capacitor for stability. A low-ESR 10- μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 39). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than $1.2\ \Omega$ over temperature. Capacitors with published ESR specifications such as the



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AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 25 through 32 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μF), the output capacitance can be reduced to 4.7 μF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the ESR graphs (Figures 25 through 32), minimum ESR is not a problem when using 10-μF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS7133QPWP. This information (along with the ESR graphs, Figures 25 through 32) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.



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APPLICATION INFORMATION

external capacitor requirements (continued)

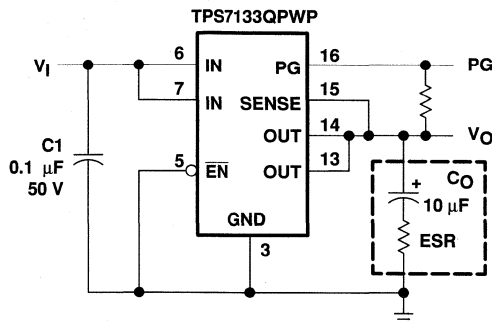


Figure 39. Typical Application Circuit

power-good indicator

The TPS7133QPWP features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS7133QPWP PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS7133QPWP also features internal current limiting and thermal protection. During normal operation, the TPS7133QPWP limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

**TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
LOW-DROPOUT VOLTAGE REGULATORS**

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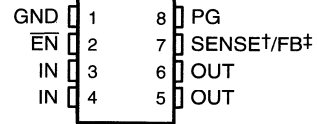
- Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions
- Very Low-Dropout Voltage . . . Maximum of 32 mV at $I_O = 100$ mA (TPS7150)
- Very Low Quiescent Current – Independent of Load . . . 285 μ A Typ
- Extremely Low Sleep-State Current
0.5 μ A Max
- 2% Tolerance Over Specified Conditions For Fixed-Output Versions
- Output Current Range of 0 mA to 500 mA
- TSSOP Package Option Offers Reduced Component Height for Space-Critical Applications
- Power-Good (PG) Status Output

description

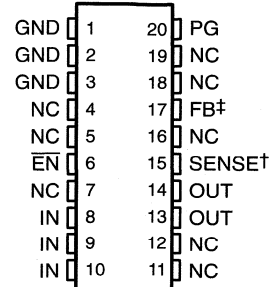
The TPS71xx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS7150) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μ A over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to 0.5 μ A maximum at $T_J = 25^\circ\text{C}$.

**D OR P PACKAGE
(TOP VIEW)**



**PW PACKAGE
(TOP VIEW)**



NC – No internal connection

† SENSE – Fixed voltage options only
(TPS7133, TPS7148, and TPS7150)

‡ FB – Adjustable version only (TPS7101)

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

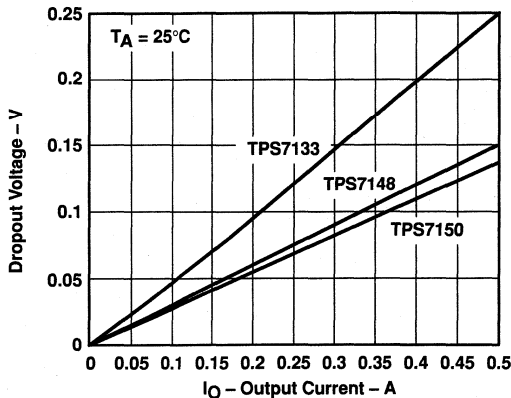


Figure 1. Dropout Voltage Versus Output Current

Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71xx family is available in PDIP (8 pin), SO (8 pin), and TSSOP (20-pin) packages. The TSSOP has a maximum height of 1.2 mm.

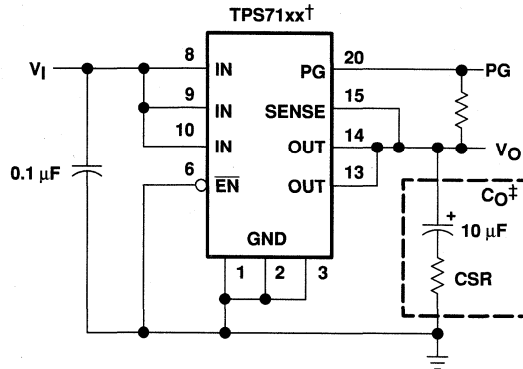
AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
-40°C to 125°C	4.9	5	5.1	TPS7150QD	TPS7150QP	TPS7150QPW	TPS7150Y
	4.75	4.85	4.95	TPS7148QD	TPS7148QP	TPS7148QPW	TPS7148Y
	3.23	3.3	3.37	TPS7133QD	TPS7133QP	TPS7133QPW	TPS7133Y
	Adjustable† 1.2 V to 9.75 V			TPS7101QD	TPS7101QP	TPS7101QPW	TPS7101Y

† The D and PW packages are available taped and reeled. Add R suffix to device type (e.g., TPS7150QDR). The TPS7101Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
 TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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† TPS7133, TPS7148, TPS7150 (fixed-voltage options)

‡ Capacitor selection is nontrivial. See application information section for details.

Figure 2. Typical Application Configuration

TPS71xx chip information

These chips, when properly assembled, display characteristics similar to the TPS71xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 15 MILS TYPICAL
BONDING PADS: 4 × 4 MILS MINIMUM
T_{Jmax} = 150°C
TOLERANCES ARE ±10%.
ALL DIMENSIONS ARE IN MILS.

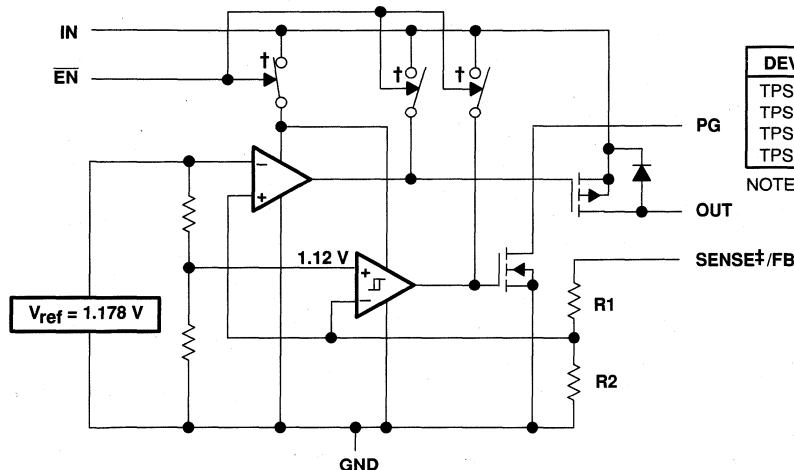
§ SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
 ¶ FB – Adjustable version only (TPS7101)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the Applications Information section of this data sheet.

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TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7101	0	∞	Ω
TPS7133	420	233	kΩ
TPS7148	726	233	kΩ
TPS7150	756	233	kΩ

NOTE A. Resistors are nominal values only.

COMPONENT COUNT

MOS transistors	464
Bipolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

† Switch positions are shown with \overline{EN} low (active).

‡ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in Applications Information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Input voltage range [¶] , V_I , PG, SENSE, \overline{EN}	-0.3 V to 11 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	-55°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

¶ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)[#]

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)[#]

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW	4025 mW	32.2 mW/°C	2576 mW	805 mW

[#] Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

^{||} Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP packages.



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 TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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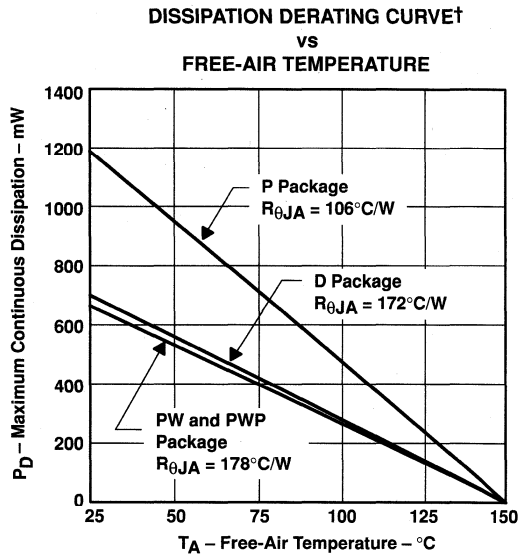


Figure 3

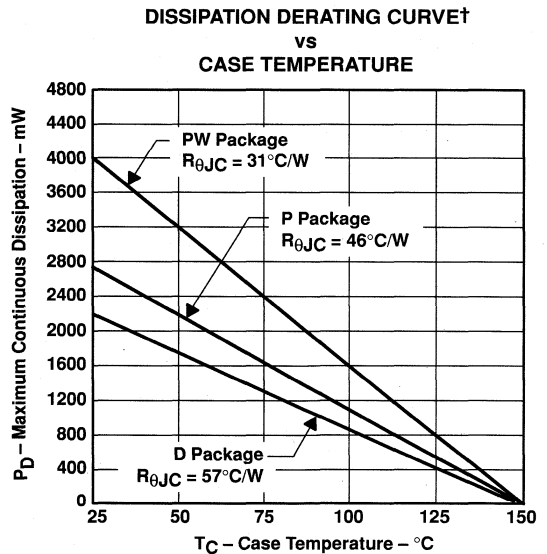


Figure 4

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

	MIN	MAX	UNIT	
Input voltage, V_I ‡	TPS7101Q	2.5	10	V
	TPS7133Q	3.77	10	
	TPS7148Q	5.2	10	
	TPS7150Q	5.33	10	
High-level input voltage at EN, V_{IH}	2		V	
Low-level input voltage at \overline{EN} , V_{IL}		0.5	V	
Output current range, I_O	0	500	mA	
Operating virtual junction temperature range, T_J	-40	125	°C	

‡ Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max \text{ load})}$. Because the TPS7101 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7101.

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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electrical characteristics at $I_O = 10$ mA, $\overline{EN} = 0$ V, $C_O = 4.7$ μ F/CSRT[†] = 1 Ω , SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	TPS7101Q, TPS7133Q TPS7148Q, TPS7150Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5$ V, 0 mA $\leq I_O \leq 500$ mA	$V_I = V_O + 1$ V,	25°C	285	350	μ A
			-40°C to 125°C		460	
Input current (standby mode)	$\overline{EN} = V_I$,	2.7 V $\leq V_I \leq 10$ V	25°C		0.5	μ A
			-40°C to 125°C		2	
Output current limit	$V_O = 0$,	$V_I = 10$ V	25°C	1.2	2	A
			-40°C to 125°C		2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$,	2.7 V $\leq V_I \leq 10$ V	25°C		0.5	μ A
			-40°C to 125°C		1	
PG leakage current	Normal operation,	$V_{PG} = 10$ V	25°C	0.02	0.5	μ A
			-40°C to 125°C		0.5	
Output voltage temperature coefficient		-40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
\overline{EN} logic high (standby mode)	2.5 V $\leq V_I \leq 6$ V	-40°C to 125°C		2		V
	6 V $\leq V_I \leq 10$ V			2.7		
\overline{EN} logic low (active mode)	2.7 V $\leq V_I \leq 10$ V	25°C			0.5	V
		-40°C to 125°C			0.5	
\overline{EN} hysteresis voltage		25°C		50		mV
\overline{EN} input current	0 V $\leq V_I \leq 10$ V	0 V $\leq V_I \leq 10$ V	25°C	-0.5	0.5	μ A
			-40°C to 125°C	-0.5	0.5	
Minimum V_I for active pass element			25°C	2.05	2.5	V
			-40°C to 125°C		2.5	
Minimum V_I for valid PG	$I_{PG} = 300$ μ A	$I_{PG} = 300$ μ A	25°C	1.06	1.5	V
			-40°C to 125°C		1.9	

[†] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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TPS7101 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSR}^\dagger = 1\text{ }\Omega$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		T _J	TPS7101Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	$V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$		25°C		1.178		V
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			-40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	$V_I = 2.4\text{ V}$	$50\text{ }\mu\text{A} \leq I_O \leq 150\text{ mA}$	25°C		0.7	1	Ω
			-40°C to 125°C			1	
	$V_I = 2.4\text{ V}$	$150\text{ mA} \leq I_O \leq 500\text{ mA}$	25°C		0.83	1.3	
			-40°C to 125°C			1.3	
	$V_I = 2.9\text{ V}$	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C		0.52	0.85	
			-40°C to 125°C			0.85	
$V_I = 3.9\text{ V}$	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C		0.32			
		-40°C to 125°C					
Input regulation	$V_I = 2.5\text{ V to } 10\text{ V}$, See Note 1	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C			18	mV
			-40°C to 125°C			25	
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$, See Note 1	$2.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C			14	mV
			-40°C to 125°C			25	
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$, See Note 1	$2.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C			22	mV
			-40°C to 125°C			54	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	48	59	dB	
			-40°C to 125°C	44			
		$I_O = 500\text{ mA}$, See Note 1	25°C	45	54		
			-40°C to 125°C	44			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C		2	$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C		95	μVrms	
		$C_O = 10\text{ }\mu\text{F}$	25°C		89		
		$C_O = 100\text{ }\mu\text{F}$	25°C		74		
PG trip-threshold voltage [§]	V_{FB} voltage decreasing from above V_{PG}		-40°C to 125°C	1.101		1.145	V
PG hysteresis voltage [§]	Measured at V_{FB}		25°C		12		mV
PG output low voltage [§]	$I_{\text{PG}} = 400\text{ }\mu\text{A}$, $V_I = 2.13\text{ V}$	25°C		0.1	0.4	V	
		-40°C to 125°C			0.4		
FB input current		25°C		-10	0.1	10	nA
		-40°C to 125°C			-20	20	

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

[§] Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9\text{ V}$ and $I_O > 150\text{ mA}$ simultaneously, pass element $r_{\text{DS(on)}}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$$

$r_{\text{DS(on)}}$ is a function of both output current and input voltage. The parametric table lists $r_{\text{DS(on)}}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 26.



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TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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TPS7133 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSR}^\dagger = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS7133Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$,	$I_O = 10\text{ mA}$	25°C	3.3		V	
	$4.3\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	3.23	3.37		
Dropout voltage	$I_O = 10\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	4.5	7	mV	
			-40°C to 125°C	8			
	$I_O = 100\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	47	60		
			-40°C to 125°C	80			
	$I_O = 500\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	235	300		
			-40°C to 125°C	400			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$,	$V_I = 3.23\text{ V}$,	25°C	0.47	0.6	Ω	
			$I_O = 500\text{ mA}$	-40°C to 125°C	0.8		
Input regulation	$V_I = 4.3\text{ V to }10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	20		mV	
			-40°C to 125°C	27			
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$,	$4.3\text{ V} \leq V_I \leq 10\text{ V}$	25°C	21	38	mV	
			-40°C to 125°C	75			
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$,	$4.3\text{ V} \leq V_I \leq 10\text{ V}$	25°C	30	60	mV	
			-40°C to 125°C	120			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	43	54	dB	
			-40°C to 125°C	40			
		$I_O = 500\text{ mA}$	25°C	39	49		
			-40°C to 125°C	36			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\text{Hz}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$,	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		μVrms	
		$C_O = 10\text{ }\mu\text{F}$	25°C	228			
		$C_O = 100\text{ }\mu\text{F}$	25°C	159			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	2.868	3	V	
PG hysteresis voltage			25°C	35		mV	
PG output low voltage	$I_{PG} = 1\text{ mA}$,	$V_I = 2.8\text{ V}$	25°C	0.22	0.4	V	
			-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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TPS7148 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 5.85\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSRT} = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T _J	TPS7148Q		UNIT
				MIN	TYP	
Output voltage	$V_I = 5.85\text{ V}$, $I_O = 10\text{ mA}$		25°C	4.85		V
	$5.85\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 500\text{ mA}$		-40°C to 125°C	4.75	4.95	
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 4.75\text{ V}$		25°C	2.9	6	mV
			-40°C to 125°C	8		
	$I_O = 100\text{ mA}$, $V_I = 4.75\text{ V}$		25°C	30	37	
			-40°C to 125°C	54		
	$I_O = 500\text{ mA}$, $V_I = 4.75\text{ V}$		25°C	150	180	
			-40°C to 125°C	250		
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 4.75\text{ V}$	25°C	0.32	0.35	Ω
			-40°C to 125°C	0.52		
Input regulation	$V_I = 5.85\text{ V}$ to 10 V, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		25°C	27		mV
			-40°C to 125°C	37		
Output regulation	$I_O = 5\text{ mA}$ to 500 mA, $5.85\text{ V} \leq V_I \leq 10\text{ V}$		25°C	12	42	mV
			-40°C to 125°C	80		
	$I_O = 50\text{ }\mu\text{A}$ to 500 mA, $5.85\text{ V} \leq V_I \leq 10\text{ V}$		25°C	42	60	mV
			-40°C to 125°C	130		
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	42	53	dB
			-40°C to 125°C	39		
		$I_O = 500\text{ mA}$	25°C	39	50	
			-40°C to 125°C	35		
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT} = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	410		μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$	25°C	328		
		$C_O = 100\text{ }\mu\text{F}$	25°C	212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	4.5	4.7	V
PG hysteresis voltage			25°C	50		mV
PG output low voltage	$I_{\text{PG}} = 1.2\text{ mA}$, $V_I = 4.12\text{ V}$		25°C	0.2	0.4	V
			-40°C to 125°C	0.4		

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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TPS7150 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSRT} = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	TPS7150Q			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V}$, $6\text{ V} \leq V_I \leq 10\text{ V}$	$I_O = 10\text{ mA}$ $5\text{ mA} \leq I_O \leq 500\text{ mA}$	25°C	5		V
			-40°C to 125°C	4.9	5.1	
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	2.9		6	mV
					8	
	$I_O = 100\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	27		32	
					47	
$I_O = 500\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	146		170		
				230		
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 4.88\text{ V}$	25°C	0.29	0.32	Ω
			-40°C to 125°C	0.47		
Input regulation	$V_I = 6\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	25		mV	
			-40°C to 125°C	32		
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	30		45	mV
					86	
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	45		65	mV
					140	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	45	55	dB
			-40°C to 125°C	40		
		$I_O = 500\text{ mA}$	25°C	42	52	
			-40°C to 125°C	36		
Output noise-spectral density	$f = 120\text{ Hz}$	25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT} = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	430		μVrms
		$C_O = 10\text{ }\mu\text{F}$	25°C	345		
		$C_O = 100\text{ }\mu\text{F}$	25°C	220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}	-40°C to 125°C	4.55	4.75		V
PG hysteresis voltage		25°C	53		mV	
PG output low voltage	$I_{PG} = 1.2\text{ mA}$, $V_I = 4.25\text{ V}$	25°C	0.2	0.4		V
		-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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electrical characteristics at $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\ \mu\text{F}/\text{CSR}^\dagger = 1\ \Omega$, $T_J = 25^\circ\text{C}$, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7101Y, TPS7133Y TPS7148Y, TPS7150Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5\text{ V}$, $0\text{ mA} \leq I_O \leq 500\text{ mA}$	$V_I = V_O + 1\text{ V}$, 285			μA
Output current limit	$V_O = 0$, $V_I = 10\text{ V}$	1.2			A
PG leakage current	Normal operation, $V_{PG} = 10\text{ V}$	0.02			μA
Thermal shutdown junction temperature		165			$^\circ\text{C}$
\overline{EN} hysteresis voltage		50			mV
Minimum V_I for active pass element		2.05			V
Minimum V_I for valid PG	$I_{PG} = 300\ \mu\text{A}$	1.06			V

PARAMETER	TEST CONDITIONS‡	TPS7101Y			UNIT
		MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	$V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$	1.178			V
Pass-element series resistance (see Note 2)	$V_I = 2.4\text{ V}$, $50\ \mu\text{A} \leq I_O \leq 150\text{ mA}$	0.7			Ω
	$V_I = 2.4\text{ V}$, $150\text{ mA} \leq I_O \leq 500\text{ mA}$	0.83			
	$V_I = 2.9\text{ V}$, $50\ \mu\text{A} \leq I_O \leq 500\text{ mA}$	0.52			
	$V_I = 3.9\text{ V}$, $50\ \mu\text{A} \leq I_O \leq 500\text{ mA}$	0.32			
	$V_I = 5.9\text{ V}$, $50\ \mu\text{A} \leq I_O \leq 500\text{ mA}$	0.23			
Input regulation	$V_I = 2.5\text{ V to } 10\text{ V}$, See Note 1	$50\ \mu\text{A} \leq I_O \leq 500\text{ mA}$,	18		mV
Output regulation	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$I_O = 5\text{ mA to } 500\text{ mA}$,	14		mV
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$I_O = 50\ \mu\text{A to } 500\text{ mA}$,	22		mV
Ripple rejection	$V_I = 3.5\text{ V}$, $I_O = 50\ \mu\text{A}$	$f = 120\text{ Hz}$,	59		dB
Output noise-spectral density	$V_I = 3.5\text{ V}$,	$f = 120\text{ Hz}$	2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 3.5\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\ \Omega$	$C_O = 4.7\ \mu\text{F}$	95		μVrms
		$C_O = 10\ \mu\text{F}$	89		
		$C_O = 100\ \mu\text{F}$	74		
PG hysteresis voltage§	$V_I = 3.5\text{ V}$,	Measured at V_{FB}	12		mV
PG output low voltage§	$V_I = 2.13\text{ V}$,	$I_{PG} = 400\ \mu\text{A}$	0.1		V
FB input current	$V_I = 3.5\text{ V}$	$V_I = 3.5\text{ V}$	0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9\text{ V}$ and $I_O > 150\text{ mA}$ simultaneously, pass element $r_{DS(on)}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 26.



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electrical characteristics at $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSRT}^\dagger = 1\text{ }\Omega$, $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡	TPS7133Y			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$, $I_O = 10\text{ mA}$	3.3			V
Dropout voltage	$V_I = 3.23\text{ V}$, $I_O = 10\text{ mA}$	0.02			mV
	$V_I = 3.23\text{ V}$, $I_O = 100\text{ mA}$	47			
	$V_I = 3.23\text{ V}$, $I_O = 500\text{ mA}$	235			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $V_I = 3.23\text{ V}$, $I_O = 500\text{ mA}$	0.47			Ω
Output regulation	$4.3\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to }500\text{ mA}$	21			mV
	$4.3\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to }500\text{ mA}$	30			mV
Ripple rejection	$V_I = 4.3\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	54		dB
		$I_O = 500\text{ mA}$	49		
Output noise-spectral density	$V_I = 4.3\text{ V}$, $f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 4.3\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	274		μVrms
		$C_O = 10\text{ }\mu\text{F}$	228		
		$C_O = 100\text{ }\mu\text{F}$	159		
PG hysteresis voltage	$V_I = 4.3\text{ V}$	35			mV
PG output low voltage	$V_I = 2.8\text{ V}$, $I_{PG} = 1\text{ mA}$	0.22			V

PARAMETER	TEST CONDITIONS‡	TPS7148Y			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 5.85\text{ V}$, $I_O = 10\text{ mA}$	4.85			V
Dropout voltage	$V_I = 4.75\text{ V}$, $I_O = 10\text{ mA}$	0.08			mV
	$V_I = 4.75\text{ V}$, $I_O = 100\text{ mA}$	30			
	$V_I = 4.75\text{ V}$, $I_O = 500\text{ mA}$	150			
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$, $V_I = 4.75\text{ V}$, $I_O = 500\text{ mA}$	0.32			Ω
Output regulation	$5.85\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to }500\text{ mA}$	12			mV
	$5.85\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to }500\text{ mA}$	42			mV
Ripple rejection	$V_I = 5.85\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	53		dB
		$I_O = 500\text{ mA}$	50		
Output noise-spectral density	$V_I = 5.85\text{ V}$, $f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 5.85\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	410		μVrms
		$C_O = 10\text{ }\mu\text{F}$	328		
		$C_O = 100\text{ }\mu\text{F}$	212		
PG hysteresis voltage	$V_I = 5.85\text{ V}$	50			mV
PG output low voltage	$V_I = 4.12\text{ V}$, $I_{PG} = 1.2\text{ mA}$	0.2 0.4			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
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electrical characteristics at $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSR}^\dagger = 1\text{ }\Omega$, $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7150Y			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V}$,	$I_O = 10\text{ mA}$	5			V
Dropout voltage	$V_I = 4.88\text{ V}$,	$I_O = 10\text{ mA}$	0.13			mV
	$V_I = 4.88\text{ V}$,	$I_O = 100\text{ mA}$	27			
	$V_I = 4.88\text{ V}$,	$I_O = 500\text{ }\mu\text{A}$	146			
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 4.88\text{ V}$,	0.29			Ω
Output regulation	$6\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 5\text{ mA to } 500\text{ mA}$	30			mV
	$6\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$	45			mV
Ripple rejection	$V_I = 6\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	55			dB
		$I_O = 500\text{ mA}$	52			
Output noise-spectral density	$V_I = 6\text{ V}$,	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 6\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	430			μVrms
		$C_O = 10\text{ }\mu\text{F}$	345			
		$C_O = 100\text{ }\mu\text{F}$	220			
PG hysteresis voltage	$V_I = 6\text{ V}$		53			mV
PG output low voltage	$V_I = 4.25\text{ V}$,	$P_G = 1.2\text{ mA}$	0.2			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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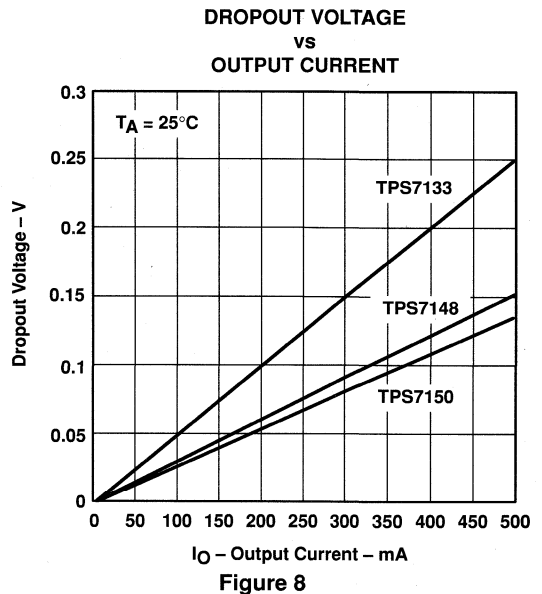
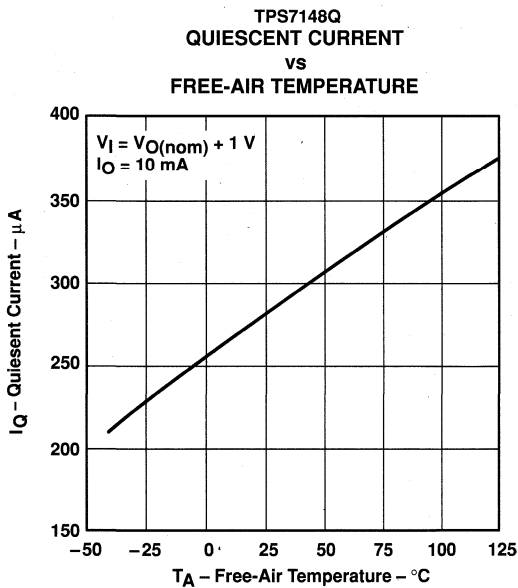
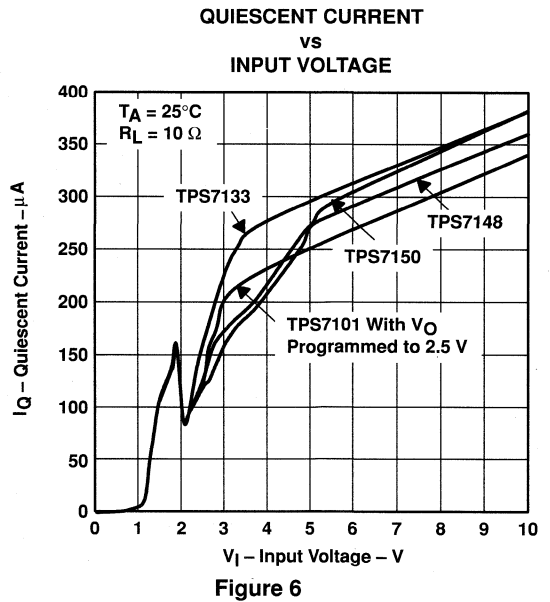
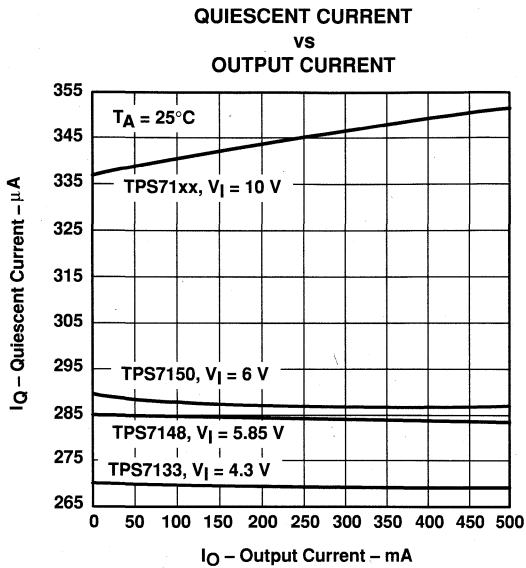
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CHANGE IN DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

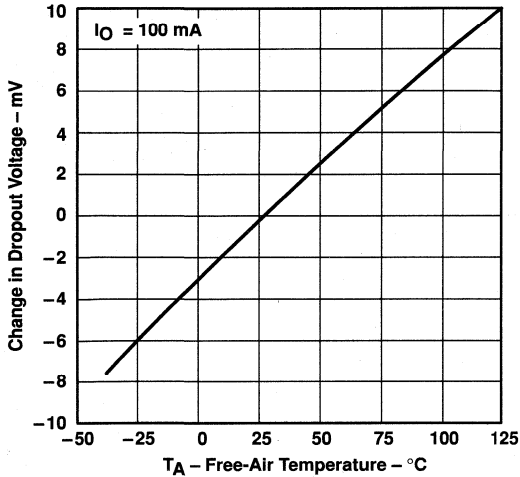


Figure 9

CHANGE IN OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

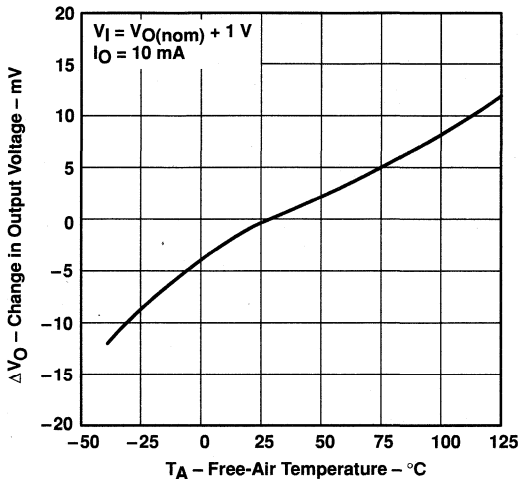


Figure 10

OUTPUT VOLTAGE
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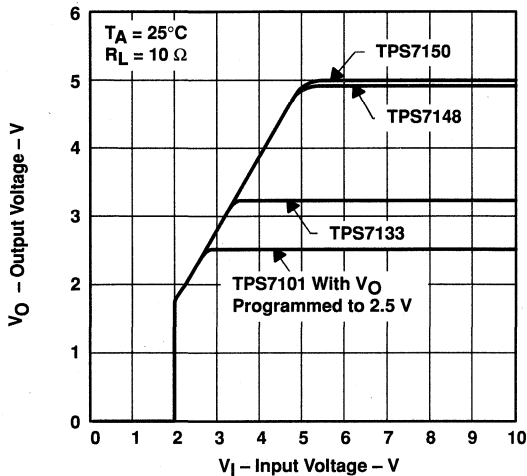


Figure 11

CHANGE IN OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

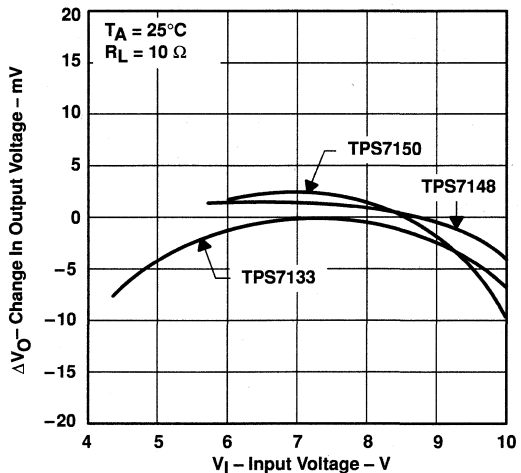
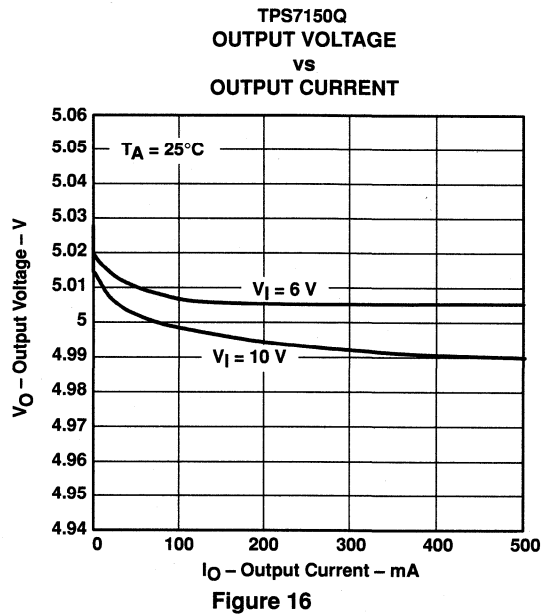
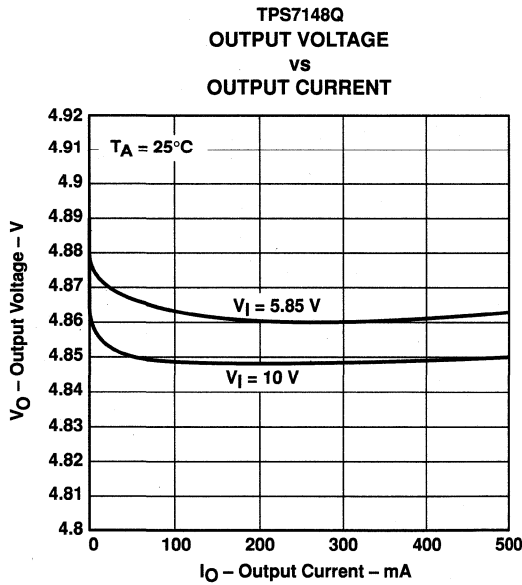
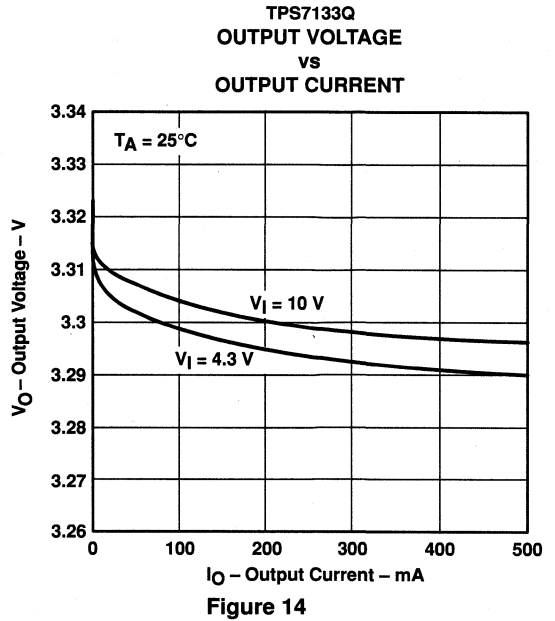
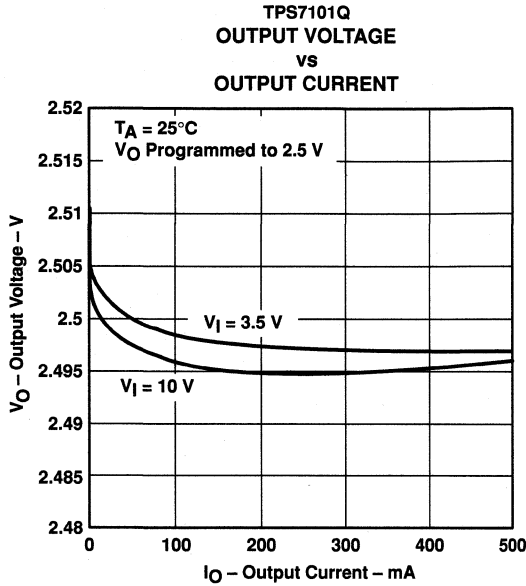


Figure 12

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

TPS7101Q
RIPPLE REJECTION
vs
FREQUENCY

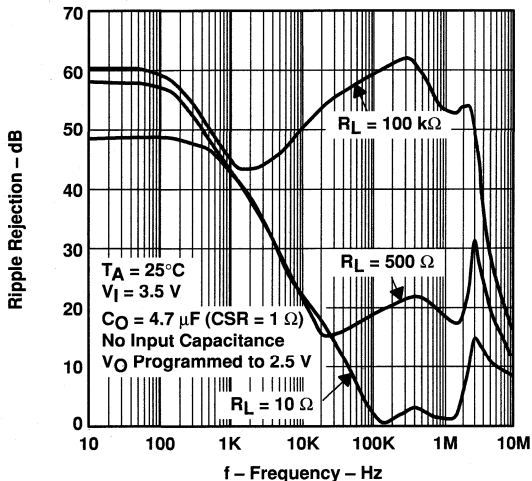


Figure 17

TPS7133Q
RIPPLE REJECTION
vs
FREQUENCY

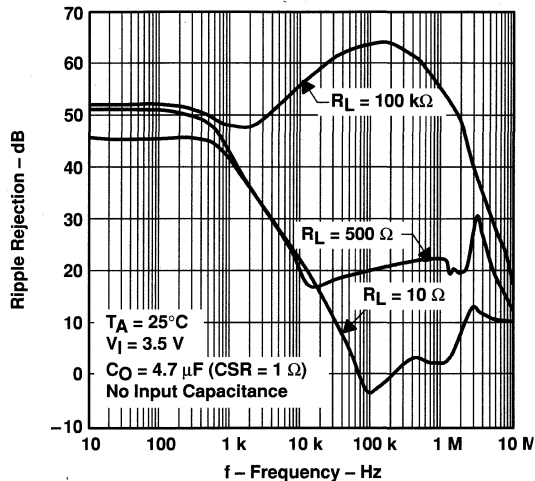


Figure 18

TPS7148Q
RIPPLE REJECTION
vs
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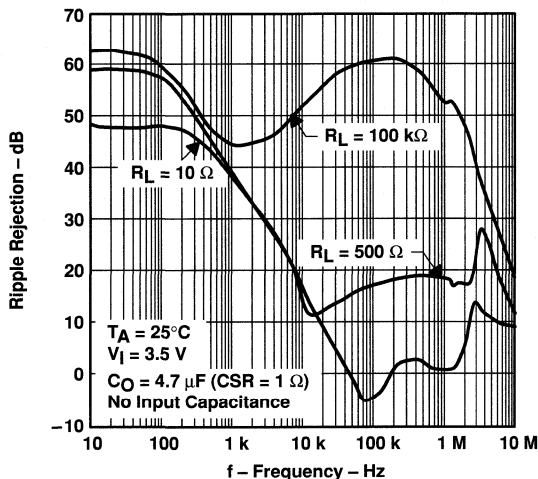


Figure 19

TPS7150Q
RIPPLE REJECTION
vs
FREQUENCY

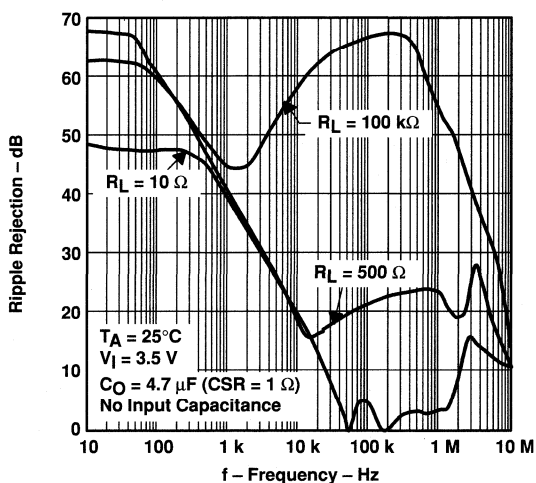


Figure 20

TYPICAL CHARACTERISTICS

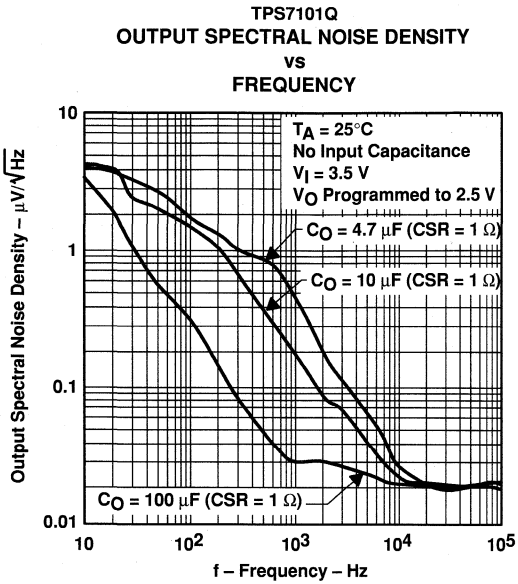


Figure 21

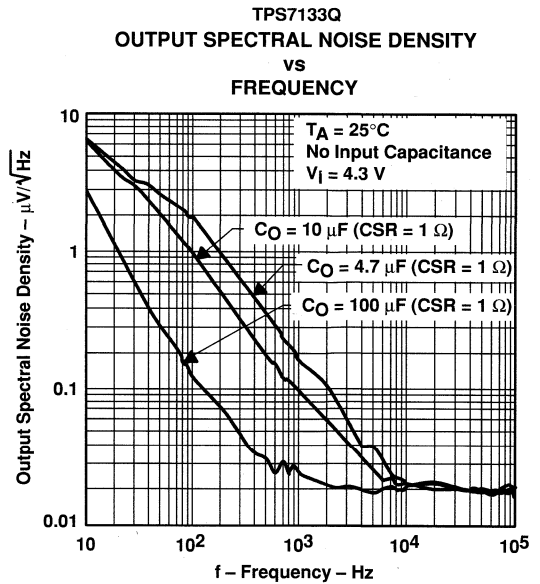


Figure 22

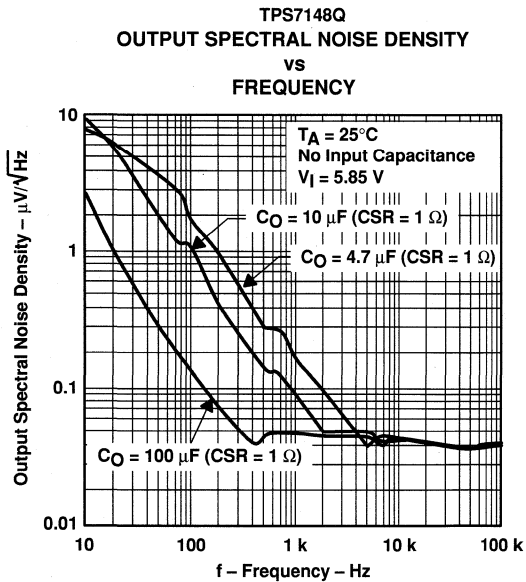


Figure 23

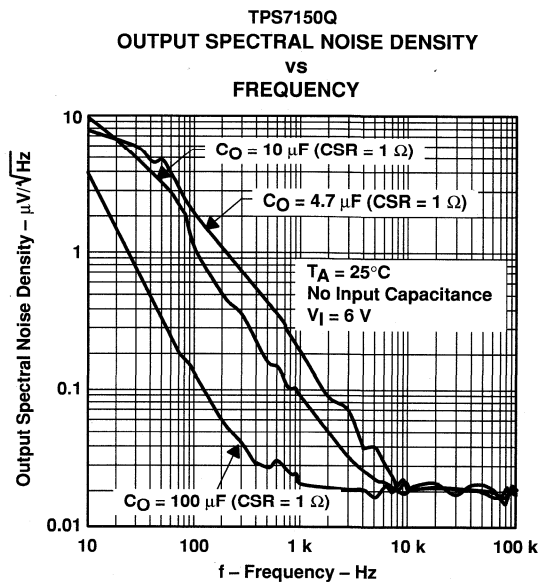


Figure 24

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE
 vs
 INPUT VOLTAGE

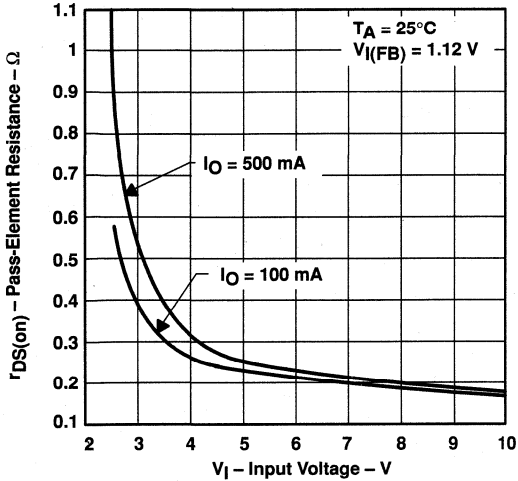


Figure 25

DIVIDER RESISTANCE
 vs
 FREE-AIR TEMPERATURE

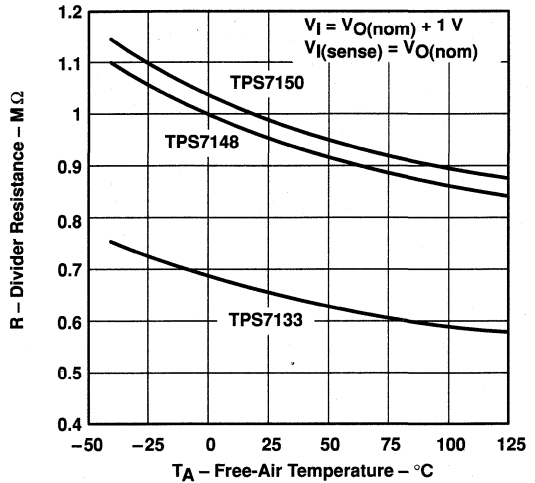


Figure 26

FIXED-OUTPUT VERSIONS
 SENSE PIN CURRENT
 vs
 FREE-AIR TEMPERATURE

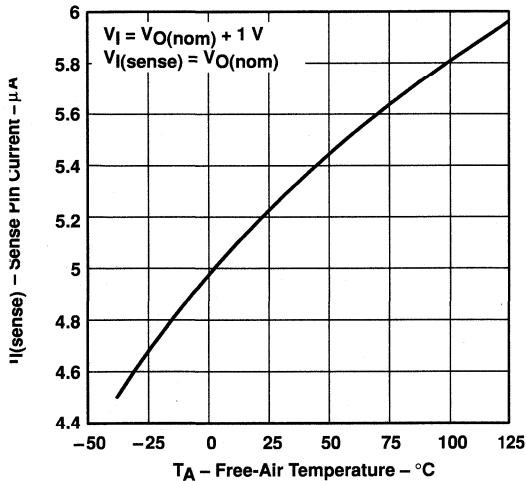


Figure 27

ADJUSTABLE VERSION
 FB LEAKAGE CURRENT
 vs
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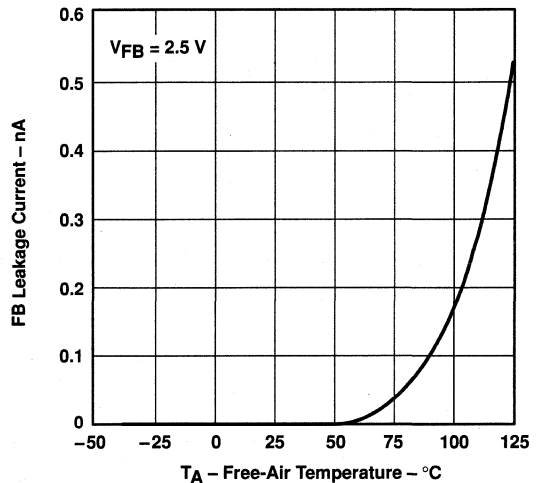


Figure 28

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE
 PASS ELEMENT
 vs
 FREE-AIR TEMPERATURE

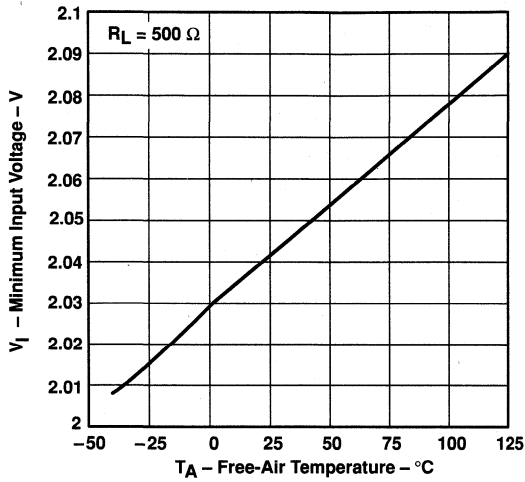


Figure 29

MINIMUM INPUT VOLTAGE FOR VALID
 POWER GOOD (PG)
 vs
 FREE-AIR TEMPERATURE

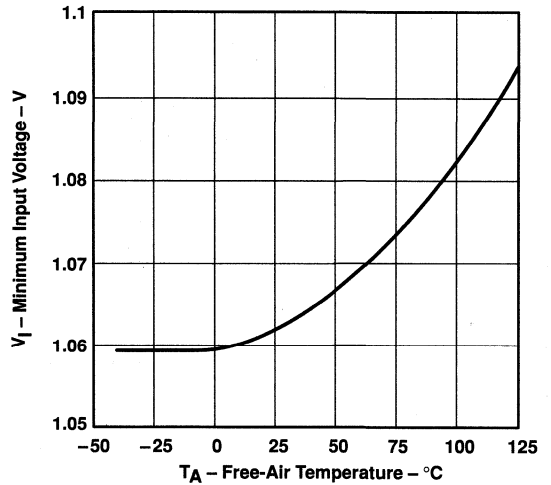


Figure 30

\overline{EN} INPUT CURRENT
 vs
 FREE-AIR TEMPERATURE

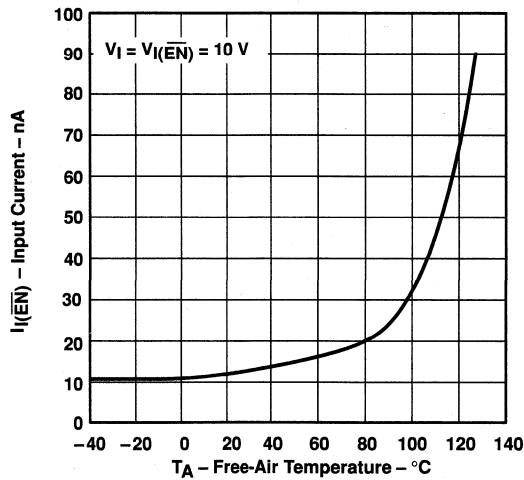


Figure 31

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
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OUTPUT VOLTAGE RESPONSE FROM
 ENABLE (EN)

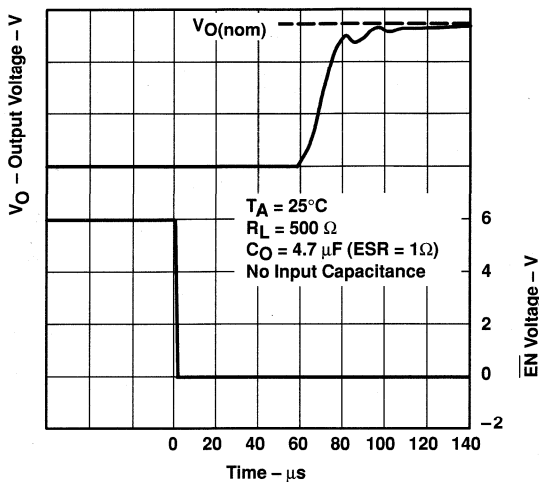


Figure 32

POWER-GOOD (PG) VOLTAGE
 vs
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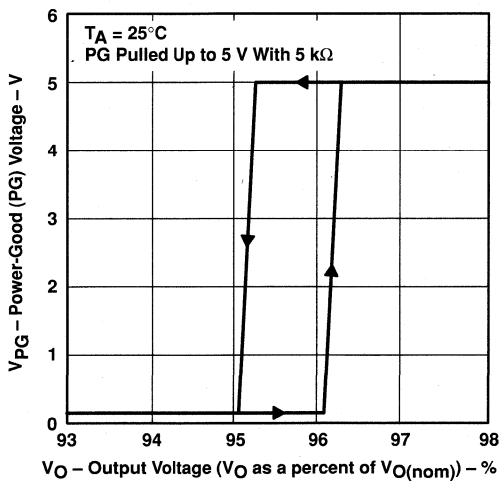


Figure 33

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE
 vs
 OUTPUT CURRENT

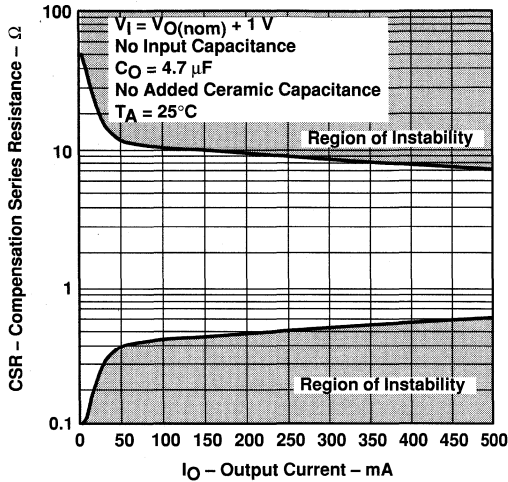


Figure 34

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE
 vs
 OUTPUT CURRENT

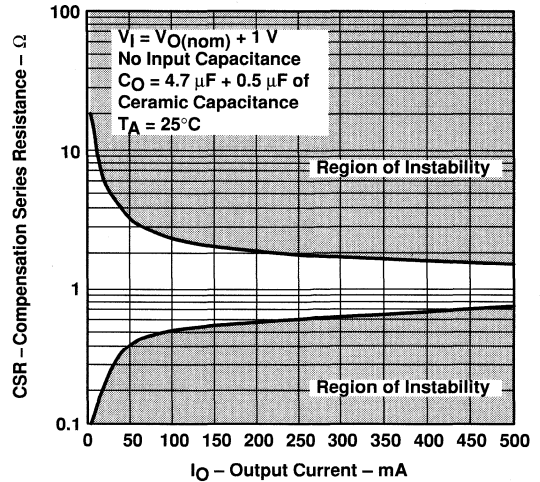


Figure 35

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE
 vs
 ADDED CERAMIC CAPACITANCE

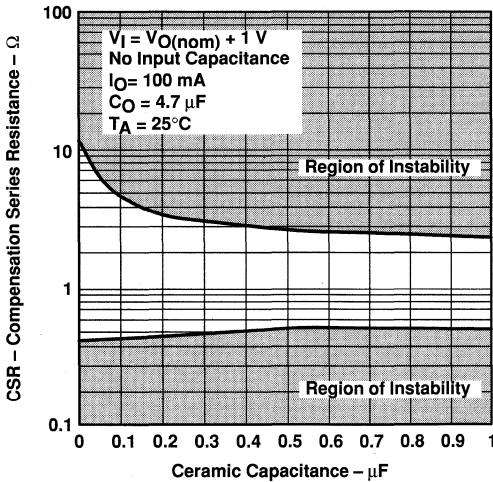


Figure 36

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE
 vs
 ADDED CERAMIC CAPACITANCE

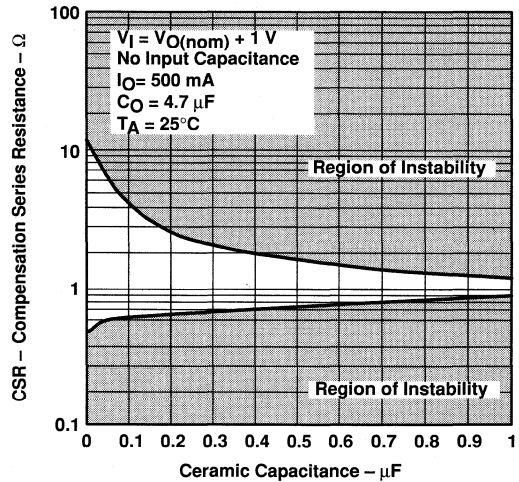


Figure 37

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**TYPICAL REGIONS OF STABILITY†
 COMPENSATION SERIES RESISTANCE
 vs
 OUTPUT CURRENT**

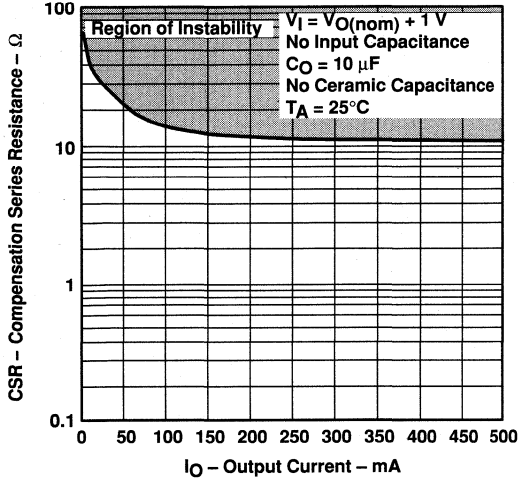


Figure 38

**TYPICAL REGIONS OF STABILITY†
 COMPENSATION SERIES RESISTANCE
 vs
 OUTPUT CURRENT**

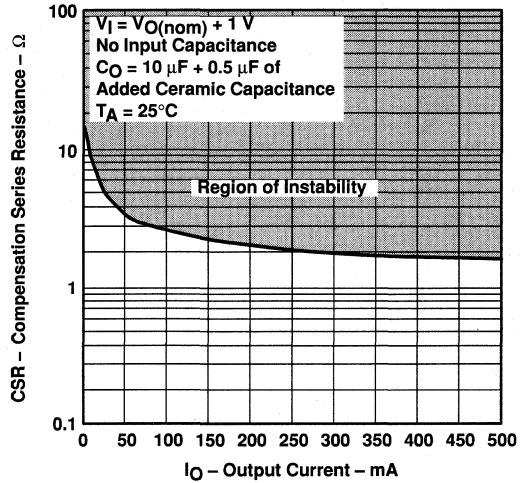


Figure 39

**TYPICAL REGIONS OF STABILITY†
 COMPENSATION SERIES RESISTANCE
 vs
 ADDED CERAMIC CAPACITANCE**

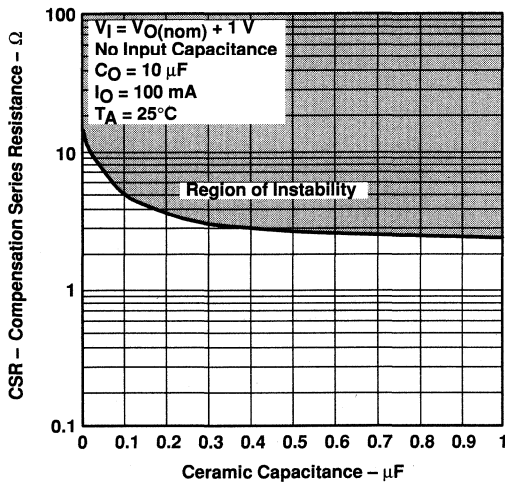


Figure 40

**TYPICAL REGIONS OF STABILITY†
 COMPENSATION SERIES RESISTANCE
 vs
 ADDED CERAMIC CAPACITANCE**

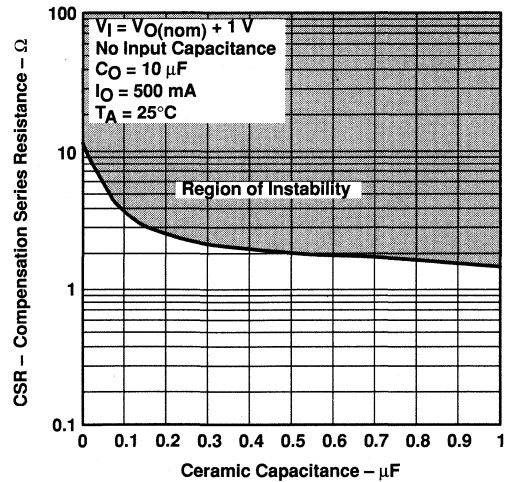


Figure 41

† CSR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS

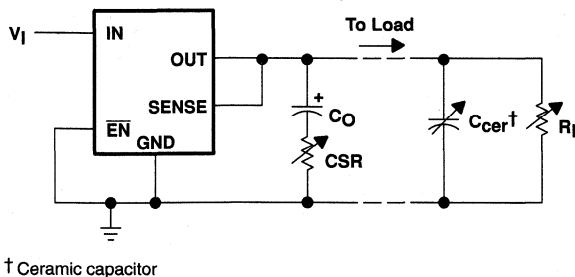


Figure 42. Test Circuit for Typical Regions of Stability (Figures 34 through 41)

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

The TPS71xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71xx family includes three fixed-output voltage regulators: the TPS7133 (3.3 V), the TPS7148 (4.85 V), and the TPS7150 (5 V). The family also offers an adjustable device, the TPS7101 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71xx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71xx family is a 4.85-V regulator, the TPS7148. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within $\pm 2\%$, allows for operation within the low-end limit of 5-V systems specified to $\pm 5\%$ tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under $2 \mu\text{A}$. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically $120 \mu\text{s}$.

minimum load requirements

The TPS71xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection if the TPS71xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.



APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS71xx family requires an output capacitor for stability. A low-ESR 10- μ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 43). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m Ω (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- μ F devices can be screened for ESR. Figures 34 through 41 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μ F), the output capacitance can be reduced to 4.7 μ F, provided ESR is maintained between 0.7 and 2.5 Ω . Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5- Ω to 1- Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 34 through 41), minimum ESR is not a problem when using 10- μ F or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71xx family. This information (along with the ESR graphs, Figures 34 through 41) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 μ F of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
T421C226M010AS	Kemet	22 μ F, 10 V	0.5	2.8 \times 6 \times 3.2
593D156X0025D2W	Sprague	15 μ F, 25 V	0.3	2.8 \times 7.3 \times 4.3
593D106X0035D2W	Sprague	10 μ F, 35 V	0.3	2.8 \times 7.3 \times 4.3
TPSD106M035R0300	AVX	10 μ F, 35 V	0.3	2.8 \times 7.3 \times 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
592D156X0020R2T	Sprague	15 μ F, 20 V	1.1	1.2 \times 7.2 \times 6
595D156X0025C2T	Sprague	15 μ F, 25 V	1	2.5 \times 7.1 \times 3.2
595D106X0025C2T	Sprague	10 μ F, 25 V	1.2	2.5 \times 7.1 \times 3.2
293D226X0016D2W	Sprague	22 μ F, 16 V	1.1	2.8 \times 7.3 \times 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
195D106X06R3V2T	Sprague	10 μ F, 6.3 V	1.5	1.3 \times 3.5 \times 2.7
195D106X0016X2T	Sprague	10 μ F, 16 V	1.5	1.3 \times 7 \times 2.7
595D156X0016B2T	Sprague	15 μ F, 16 V	1.8	1.6 \times 3.8 \times 2.6
695D226X0015F2T	Sprague	22 μ F, 15 V	1.4	1.8 \times 6.5 \times 3.4
695D156X0020F2T	Sprague	15 μ F, 20 V	1.5	1.8 \times 6.5 \times 3.4
695D106X0035G2T	Sprague	10 μ F, 35 V	1.3	2.5 \times 7.6 \times 2.5

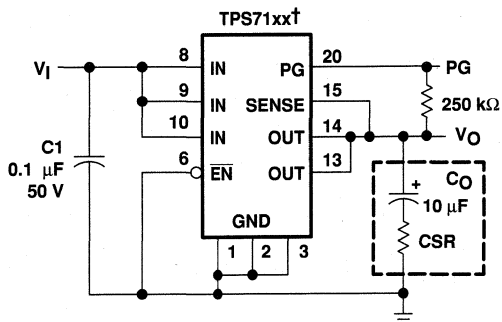
† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q
TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y
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APPLICATION INFORMATION

external capacitor requirements (continued)



† TPS7133, TPS7148, TPS7150 (fixed-voltage options)

Figure 43. Typical Application Circuit

programming the TPS7101 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 44. The equation governing the output voltage is:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right)$$

where

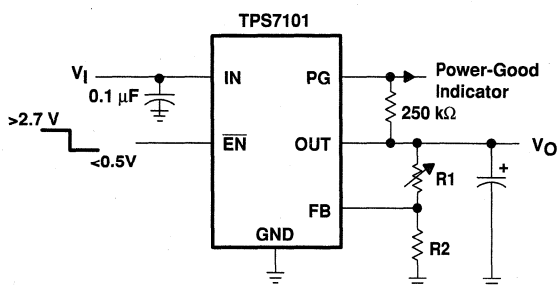
V_{ref} = reference voltage, 1.178 V typ

APPLICATION INFORMATION

programming the TPS7101 adjustable LDO regulator (continued)

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. A recommended value for R2 is 169 k Ω with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \cdot R2$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	k Ω
3.3 V	309	169	k Ω
3.6 V	348	169	k Ω
4 V	402	169	k Ω
5 V	549	169	k Ω
6.4 V	750	169	k Ω

Figure 44. TPS7101 Adjustable LDO Regulator Programming

power-good indicator

The TPS71xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS71xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71xx also features internal current limiting and thermal protection. During normal operation, the TPS71xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TPS71025 LOW-DROPOUT VOLTAGE REGULATOR

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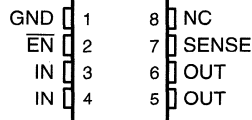
- 2.5-V Fixed-Output Regulator
- Very Low-Dropout (LDO) Voltage . . . 57 mV
Typical at $I_O = 100$ mA
- Very Low Quiescent Current, Independent
of Load . . . 292 μ A Typ
- Extremely Low Sleep-State Current,
0.5 μ A Max
- 2% Tolerance Over Specified Conditions
- Output Current Range . . . 0 mA to 500 mA
- Available in Space Saving 8-Pin SOIC and
20-Pin TSSOP Packages
- 0°C to 125°C Operating Junction
Temperature Range

description

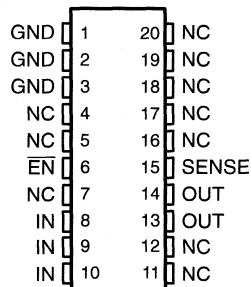
The TPS71025 low-dropout regulator offers an order of magnitude reduction in both dropout voltage and quiescent current over conventional LDO performance. The improvement results from replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 95 mV at an output current of 100 mA) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 292 μ A over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The TPS71025 also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to 0.5 μ A maximum at $T_J = 25^\circ\text{C}$.

**D OR P PACKAGE
(TOP VIEW)**



**PW PACKAGE
(TOP VIEW)**



NC – No internal connection

AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 125°C	2.45	2.5	2.55	TPS71025D	TPS71025P	TPS71025PWLE	TPS71025Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS71025DR). The PW package is only available left-end taped and reeled and is indicated by the LE suffix on the device type.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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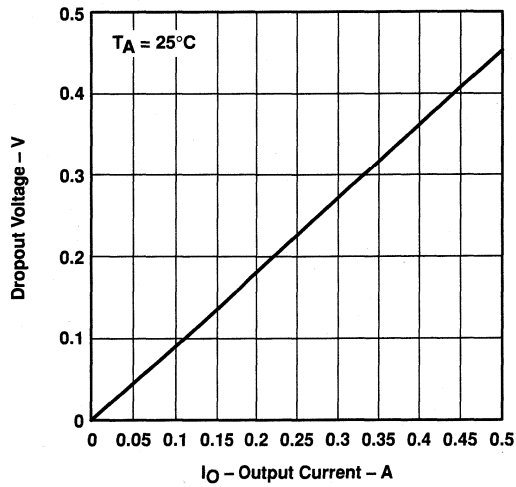
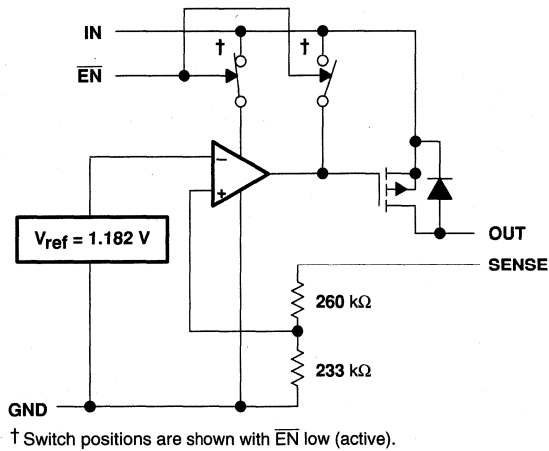


Figure 1. Dropout Voltage Versus Output Current

functional block diagram



TPS71025 LOW-DROPOUT VOLTAGE REGULATOR

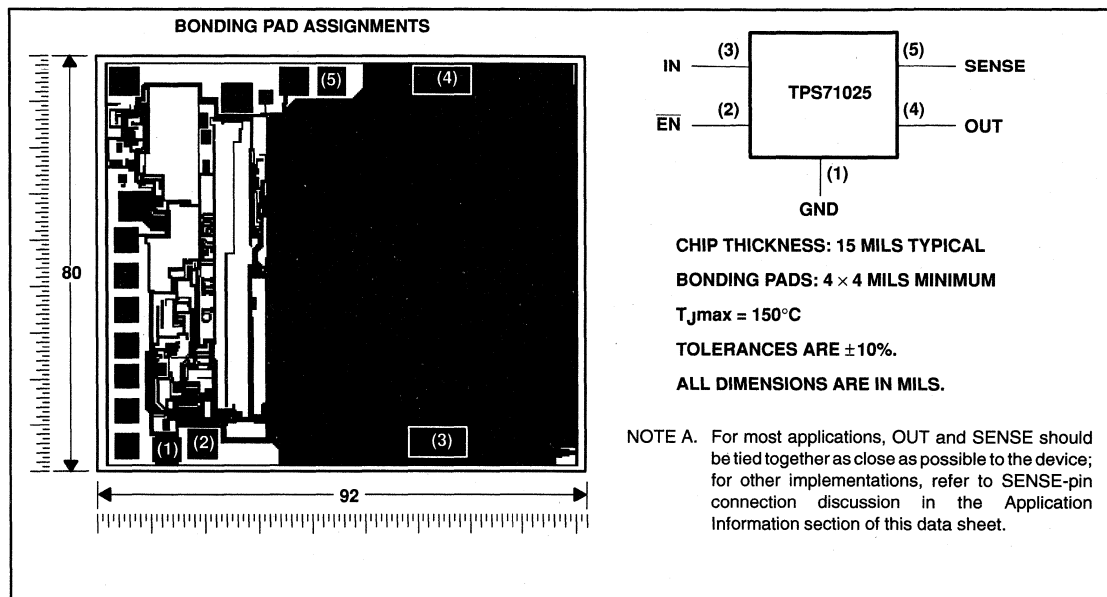
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Terminal Functions

NAME	TERMINAL NO.		DESCRIPTION
	NO.		
	D or P	PW	
EN	2	6	Enable input. Logic low enables output
GND	1	1–3	Ground
IN	3, 4	8–10	Input supply voltage
OUT	5, 6	13, 14	Output voltage
SENSE	7	15	Output voltage sense input

TPS71025Y chip information

These chips, when properly assembled, display characteristics similar to those of the TPS71025. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I , \overline{EN} (see Note 1)	–0.3 V to 11 V
Continuous output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–0°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE‡

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE‡

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW	4025 mW	32.2 mW/°C	2576 mW	805 mW

‡ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	2.97	10	V
High-level input voltage at \overline{EN} , V_{IH}	2		V
Low-level input voltage at \overline{EN} , V_{IL}	0	0.5	V
Output current range, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

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electrical characteristics over recommended operating junction temperature range, $V_{I(IN)} = 3.5\text{ V}$, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSR}^\dagger = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	MIN	TYP	MAX	UNIT
Output voltage	$3.5\text{ V} \leq V_I \leq 10\text{ V}$		25°C	2.5			V
			0°C to 125°C	2.45	2.55		
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 2.45\text{ V}$		25°C	5.7	7.5		mV
			0°C to 125°C	10			
	$I_O = 100\text{ mA}$, $V_I = 2.45\text{ V}$		25°C	57	95		
			0°C to 125°C	105			
	$I_O = 500\text{ mA}$, $V_I = 2.45\text{ V}$		25°C	330	450		
			0°C to 125°C	500			
Pass-element series resistance			25°C	0.66	0.9		Ω
			0°C to 125°C	1			
Input regulation	$V_I = 3.5\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		25°C	7	23		mV
			0°C to 125°C	12.7		29	
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$, $3.5\text{ V} \leq V_I \leq 10\text{ V}$		25°C	18	38		mV
			0°C to 125°C	75			
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$, $3.5\text{ V} \leq V_I \leq 10\text{ V}$		25°C	24	60		mV
			0°C to 125°C	120			
Ripple rejection	$f = 120\text{ Hz}$, $I_O = 50\text{ }\mu\text{A}$		25°C	43	53		dB
			0°C to 125°C	40			
	$f = 120\text{ Hz}$, $I_O = 500\text{ mA}$		25°C	39	51		
			0°C to 125°C	36			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR} = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		μVrms	
		$C_O = 10\text{ }\mu\text{F}$	25°C	228			
		$C_O = 100\text{ }\mu\text{F}$	25°C	159			
Quiescent current (active mode)	$\overline{EN} \leq 0.5\text{ V}$, $0\text{ mA} \leq I_O \leq 500\text{ mA}$		25°C	292	390	μA	
			0°C to 125°C	540			
Supply current (standby mode)	$\overline{EN} = V_I$, $2.7\text{ V} \leq V_I \leq 10\text{ V}$		25°C	18	475	nA	
			0°C to 125°C	1900			
Output current limit	$V_O = 0$, $V_I = 10\text{ V}$		25°C	1.07	2	A	
			0°C to 125°C	2			
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, $2.7\text{ V} \leq V_I \leq 10\text{ V}$		25°C	0.223	0.5	μA	
			0°C to 125°C	1			
Output voltage temperature coefficient			0°C to 125°C	61	75	ppm/°C	
Thermal shutdown junction temperature				165		°C	
Logic high input voltage (standby mode), \overline{EN}	$2.5\text{ V} \leq V_I \leq 6\text{ V}$		25°C	2		V	
	$6\text{ V} \leq V_I \leq 10\text{ V}$		0°C to 125°C	2.7			
Logic low input voltage (active mode), \overline{EN}	$2.7\text{ V} \leq V_I \leq 10\text{ V}$		25°C	0.5		V	
			0°C to 125°C	0.5			
Hysteresis voltage, \overline{EN}			0°C to 125°C	50		mV	
Input current, \overline{EN}	$0\text{ V} \leq V_I \leq 10\text{ V}$		25°C	-0.5	0.5	μA	
			0°C to 125°C	-0.5			
Input voltage, minimum for active pass element			25°C	2	2.5	V	
			0°C to 125°C	2.5			

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS71025

LOW-DROPOUT VOLTAGE REGULATOR

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electrical characteristics at $T_J = 25^\circ\text{C}$, $V_{I(IN)} = 3.5\text{ V}$, $I_O = 10\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 4.7\ \mu\text{F}/\text{CSR}^\dagger = 1\ \Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS71025Y			UNIT
		MIN	TYP	MAX	
Output voltage	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	2.5			V
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 2.45\text{ V}$	5.7			mV
	$I_O = 100\text{ mA}$, $V_I = 2.45\text{ V}$	57			
	$I_O = 500\text{ mA}$, $V_I = 2.45\text{ V}$	330			
Pass-element series resistance		0.66			Ω
Input regulation	$V_I = 3.5\text{ V}$ to 10 V	7			mV
Output regulation	$I_O = 5\text{ mA}$ to 500 mA	18			mV
	$I_O = 50\ \mu\text{A}$ to 500 mA	24			mV
Ripple rejection	$f = 120\text{ Hz}$, $I_O = 50\ \mu\text{A}$	53			dB
	$f = 120\text{ Hz}$, $I_O = 500\text{ mA}$	51			
Output noise-spectral density	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR} = 1\ \Omega$	$C_O = 4.7\ \mu\text{F}$	274		μVrms
		$C_O = 10\ \mu\text{F}$	228		
		$C_O = 100\ \mu\text{F}$	159		
Quiescent current (active mode)	$\overline{\text{EN}} = 0\text{ V}$, $0\text{ mA} \leq I_O \leq 500\text{ mA}$	292			μA
Supply current (standby mode)	$\overline{\text{EN}} = V_I$, $2.7\text{ V} \leq V_I \leq 10\text{ V}$	18			nA
Output current limit	$V_O = 0$, $V_I = 10\text{ V}$	1.07			A
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, $2.7\text{ V} \leq V_I \leq 10\text{ V}$	0.223			μA
Output voltage temperature coefficient		61			$\text{ppm}/^\circ\text{C}$
Thermal shutdown junction temperature		165			$^\circ\text{C}$
Logic high input voltage (standby mode), $\overline{\text{EN}}$	$2.5\text{ V} \leq V_I \leq 6\text{ V}$	2			V
	$6\text{ V} \leq V_I \leq 10\text{ V}$	2.7			
Logic low input voltage (active mode), $\overline{\text{EN}}$	$2.7\text{ V} \leq V_I \leq 10\text{ V}$	0.5			V
Hysteresis voltage, $\overline{\text{EN}}$		50			mV
Input current, $\overline{\text{EN}}$	$0\text{ V} \leq V_I \leq 10\text{ V}$	0			μA
Input voltage, minimum for active pass element		2			V

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TYPICAL CHARACTERISTICS

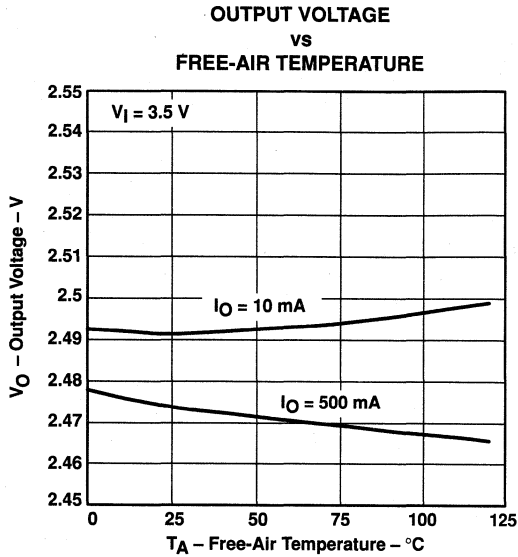


Figure 2

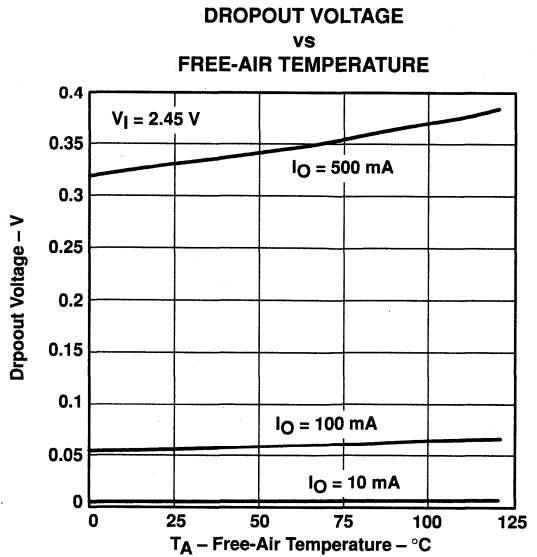


Figure 3

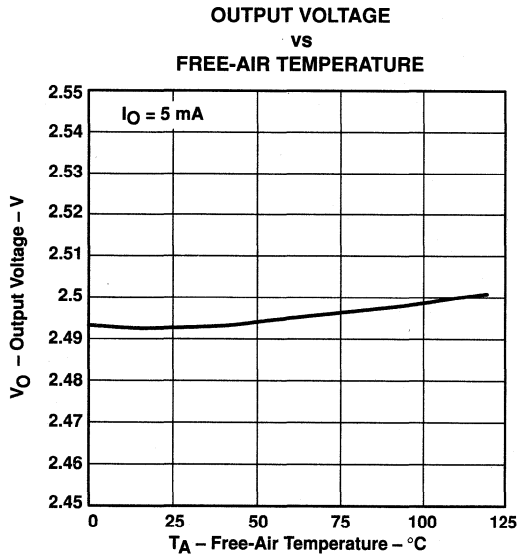


Figure 4

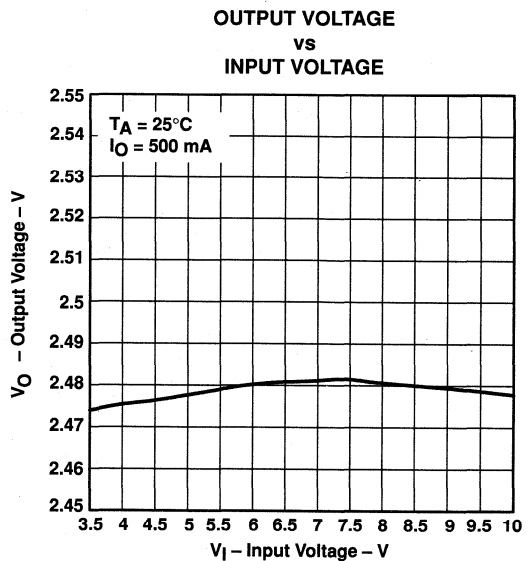


Figure 5

TPS71025 LOW-DROPOUT VOLTAGE REGULATOR

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

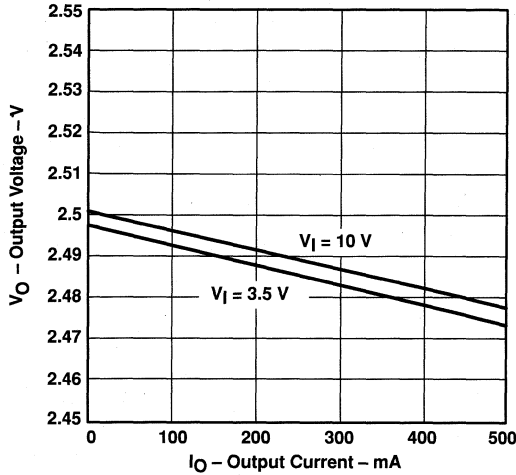


Figure 6

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

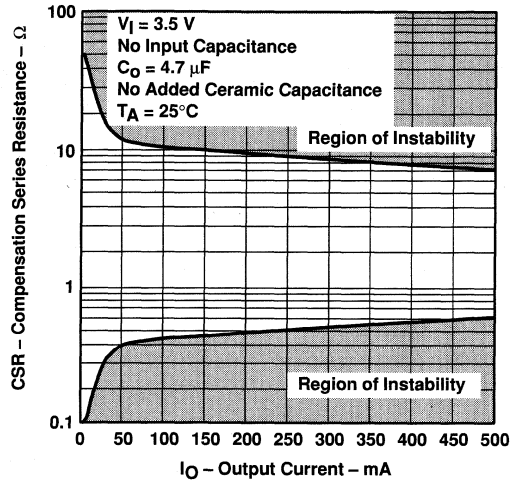


Figure 7

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

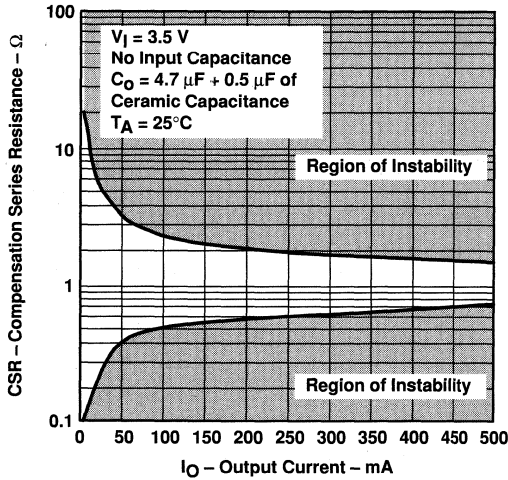


Figure 8

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

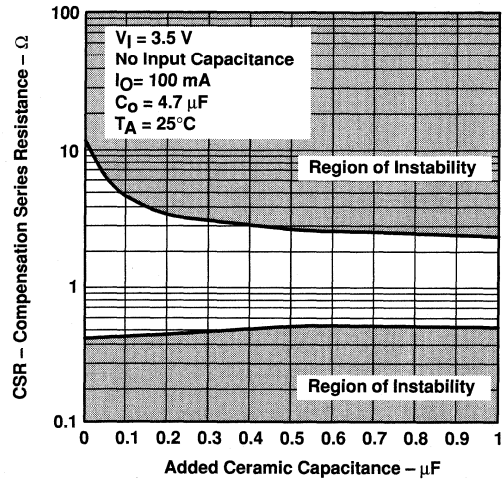


Figure 9

TYPICAL CHARACTERISTICS

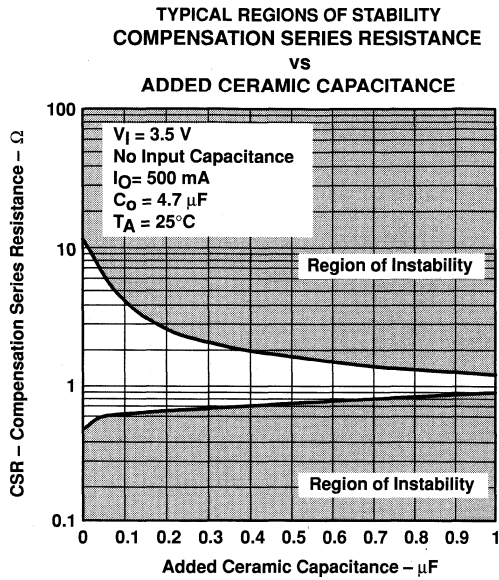


Figure 10

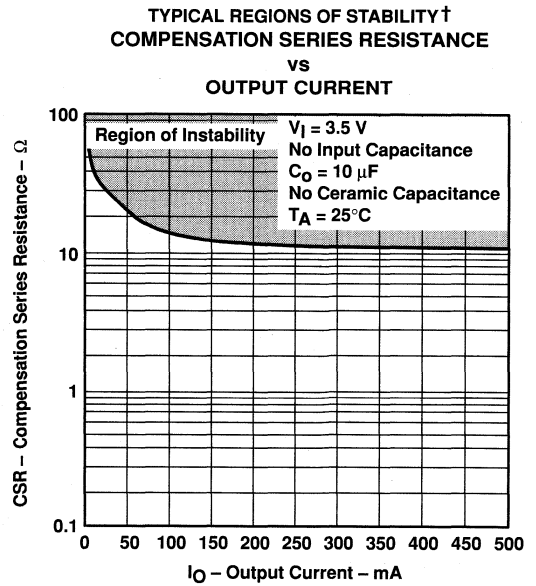


Figure 11

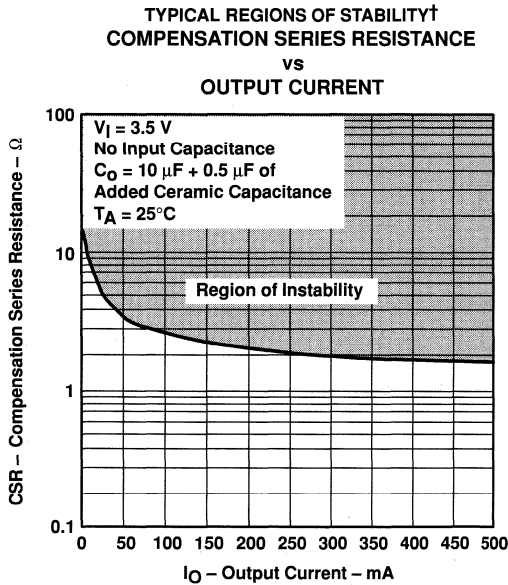


Figure 12

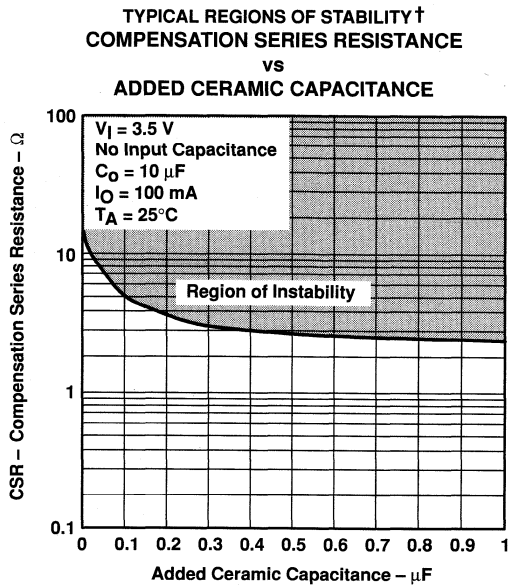


Figure 13

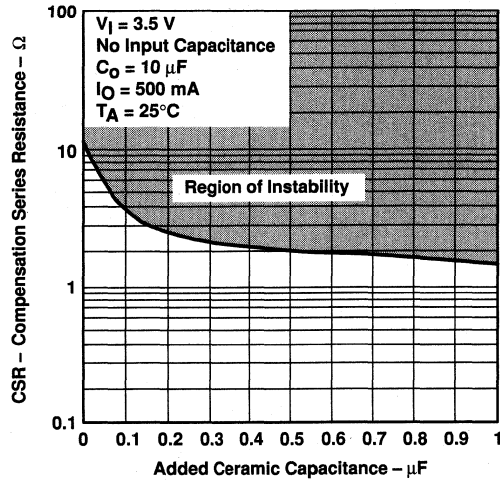
† CSR values below 0.1 Ω are not recommended.

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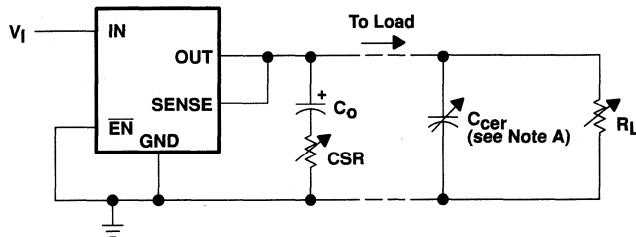
TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE



† CSR values below 0.1Ω are not recommended.

Figure 14



NOTE A. Ceramic capacitor

Figure 15. Test Circuit for Typical Regions of Stability (Figures 7 through 14)

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 16 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 17. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board ($L \times W \times H = 3.2 \text{ inch} \times 3.2 \text{ inch} \times 0.062 \text{ inch}$); the board traces and heat sink area are 1-oz (per square foot) copper.

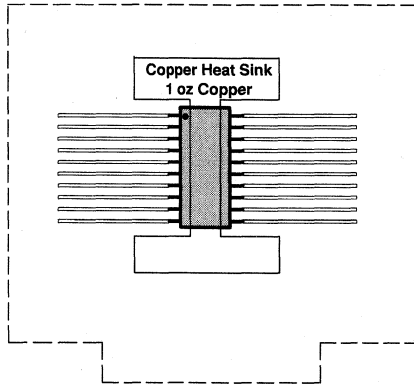


Figure 16. Thermally Enhanced PWB Layout (Not to Scale) for the 20-Pin TSSOP

Figure 18 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is $0.815 \text{ W/m} \times ^\circ\text{C}$.

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THERMAL INFORMATION

**THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
VS
AIR FLOW**

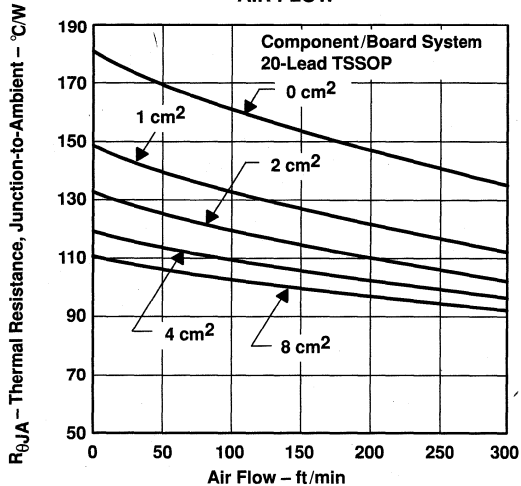


Figure 17

**THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
VS
AIR FLOW**

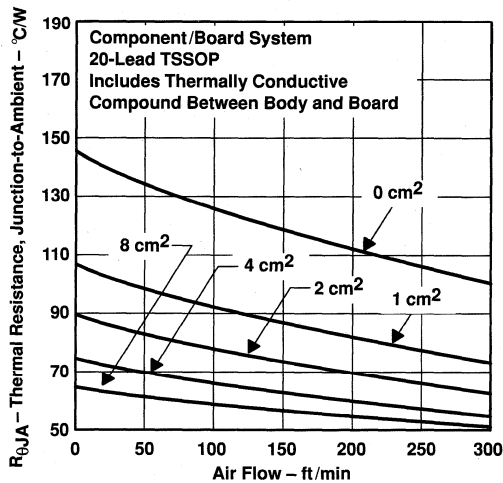


Figure 18

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation $P_{D(max)}$ limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature (i.e., 150°C absolute maximum or 125°C maximum recommended operating temperature for specified operation).

This limit should then be applied to the internal power dissipated by the TPS71025 regulator. The equation for calculating total internal power dissipation of the device is:

$$P_{D(total)} = (V_I - V_O) \times I_O + (V_I \times I_Q)$$

Because the quiescent current is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \times I_O$$

THERMAL INFORMATION

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55^\circ\text{C}$, airflow = 100 ft/min, and copper heat sink area = 1 cm², the maximum power-dissipation limit can be calculated. As indicated in Figure 18, the system $R_{\theta\text{JA}}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{R_{\theta\text{JA}(\text{system})}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{94^\circ\text{C/W}} = 745 \text{ mW}$$

If the system implements a TPS71025 regulator where $V_I = 3.3 \text{ V}$ and $I_O = 385 \text{ mA}$, the internal power dissipation is:

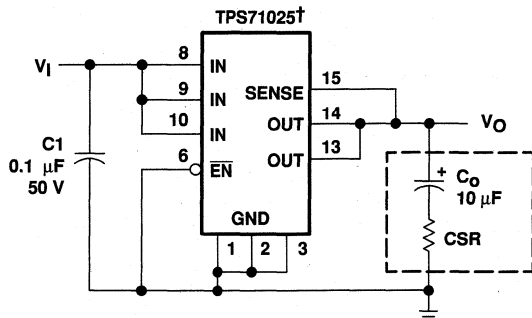
$$P_{D(\text{total})} = (V_I - V_O) \times I_O = (3.3 - 2.5) \times 0.385 = 308 \text{ mW}$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

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APPLICATION INFORMATION



† Capacitor selection is nontrivial. See external capacitor requirements section.

Figure 19. Typical Application Circuit

The TPS71025 low-dropout (LDO) regulator overcomes many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode.

device operation

The TPS71025, unlike many other LDOs, features very low quiescent current that remains virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71025 uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and stable over the full load range. The TPS71025 specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71025 quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS71025 also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under $2 \mu\text{A}$. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically $120 \mu\text{s}$.

minimum load requirements

The TPS71025 family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μ F) improves load transient response and noise rejection if the TPS71025 is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS71025 requires an output capacitor for stability. A low-ESR 10- μ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 11). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m Ω (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- μ F devices can be screened for ESR. Figure 7 through Figure 14 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μ F), the output capacitance can be reduced to 4.7 μ F, provided ESR is maintained between 0.7 and 2.5 Ω . Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5- Ω to 1- Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the ESR graphs (Figure 7 through Figure 14), minimum ESR is not a problem when using 10- μ F or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71025. This information (along with the ESR graphs, Figure 7 through Figure 14) is included to assist in selection of suitable capacitance for the application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

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APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF , 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF , 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF , 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF , 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF , 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF , 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF , 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF , 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF , 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF , 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF , 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF , 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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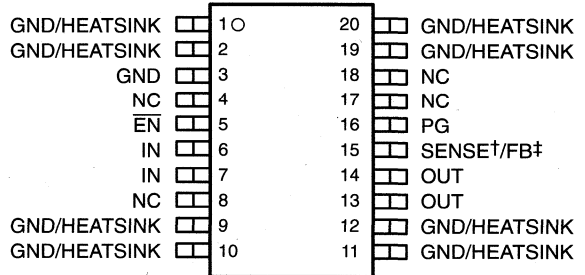
- Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions
- Very Low-Dropout Voltage . . . Maximum of 32 mV at $I_O = 100$ mA (TPS71H50)
- Very Low Quiescent Current – Independent of Load . . . 285 μ A Typ
- Extremely Low Sleep-State Current 0.5 μ A Max
- 2% Tolerance Over Specified Conditions For Fixed-Output Versions
- Output Current Range of 0 mA to 500 mA
- TSSOP Package Option Offers Reduced Component Height for Space-Critical Applications
- Thermally Enhanced Surface-Mount Package
- Power-Good (PG) Status Output

description

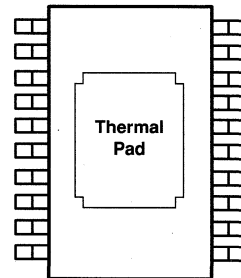
The TPS71Hxx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS71H50) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μ A over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to 0.5 μ A maximum at $T_J = 25^\circ\text{C}$.

PWP PACKAGE
(TOP VIEW)



PWP PACKAGE
(BOTTOM VIEW)



NC – No internal connection

† SENSE – Fixed voltage options only (TPS71H33, TPS71H48, and TPS71H50)

‡ FB – Adjustable version only (TPS71H01)

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

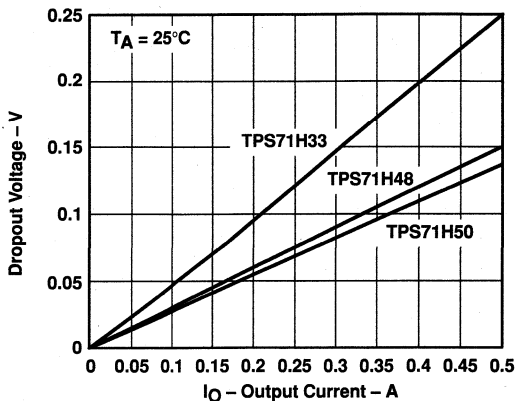


Figure 1. Dropout Voltage Versus Output Current

Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71Hxx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71Hxx family is available in a TSSOP (20-pin) thermally enhanced surface-mount power package. The package has an innovative thermal pad that, when soldered to the printed-wiring board (PWB), enables the device to dissipate several watts of power (see Thermal Information section). Maximum height of the package is 1.2 mm.

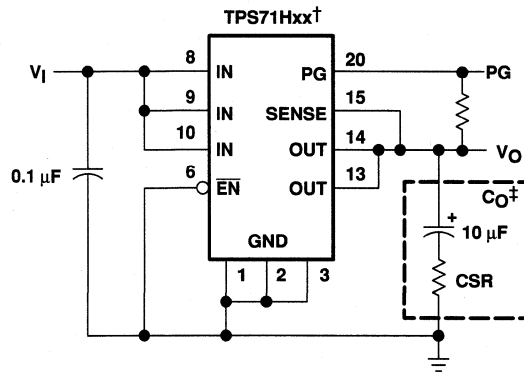
AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)			TSSOP (PWP)
	MIN	TYP	MAX	
-55°C to 150°C	4.9	5	5.1	TPS71H50QPWP
	4.75	4.85	4.95	TPS71H48QPWP
	3.23	3.3	3.37	TPS71H33QPWP
	Adjustable† 1.2 V to 9.75 V			TPS71H01QPWP

† The PWP package is only available left-end taped and reeled, as indicated by the LE suffix on the device type. The TPS71H01Q is programmable using an external resistor divider (see application information).

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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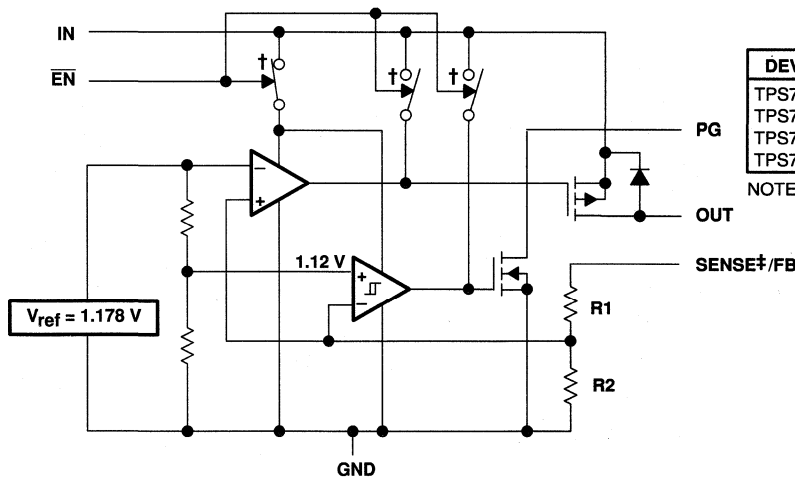


† TPS71H33, TPS71H48, TPS71H50 (fixed-voltage options)

‡ Capacitor selection is nontrivial. See application information section for details.

Figure 2. Typical Application Configuration

functional block diagram



† Switch positions are shown with $\overline{\text{EN}}$ low (active).

‡ For most applications, SENSE should be externally connected to OUT as close as possible to the device. (For other implementations, refer to SENSE-pin connection discussion in Applications Information section.)

RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS71H01	0	∞	Ω
TPS71H33	420	233	k Ω
TPS71H48	726	233	k Ω
TPS71H50	756	233	k Ω

NOTE A. Resistors are nominal values only.

COMPONENT COUNT

MOS transistors	464
Bipolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I , PG, SENSE, \overline{EN}	-0.3 V to 11 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	-55°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)§

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
PWP¶	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)§

PACKAGE	$T_C \leq 62.5^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
PWP¶	25 W	285.7 mW/°C	22.9 W	7.1 W

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

¶ Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP packages.



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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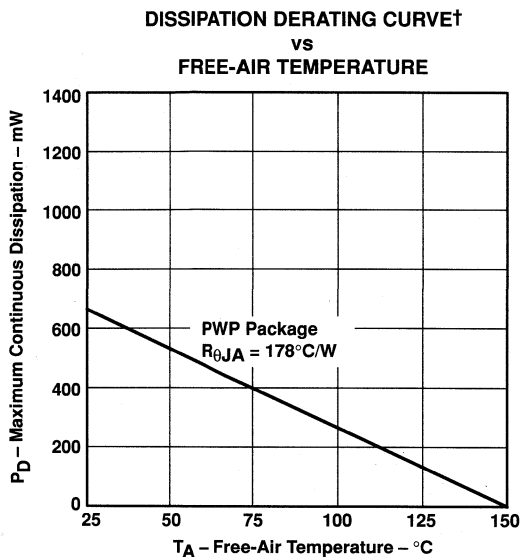


Figure 3

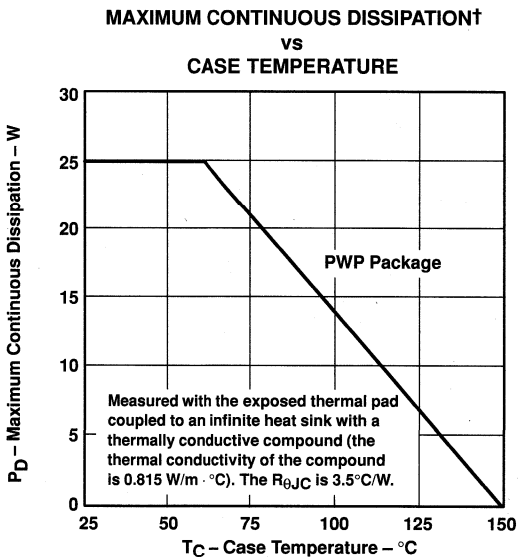


Figure 4

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I †	TPS71H01Q	2.5	10	V
	TPS71H33Q	3.77	10	
	TPS71H48Q	5.2	10	
	TPS71H50Q	5.33	10	
High-level input voltage at \overline{EN} , V_{IH}		2		V
Low-level input voltage at \overline{EN} , V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		-40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_O(\max) + V_{DO(\max \text{ load})}$. Because the TPS71H01 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS71H01.

electrical characteristics at $I_O = 10 \text{ mA}$, $\overline{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}/\text{CSR}^\ddagger = 1 \Omega$, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	T_J	TPS71H01Q, TPS71H33Q TPS71H48Q, TPS71H50Q			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5 \text{ V}$, $0 \text{ mA} \leq I_O \leq 500 \text{ mA}$	25°C		285	350	μA
		-40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C			0.5	μA
		-40°C to 125°C			2	
Output current limit	$V_O = 0$, $V_I = 10 \text{ V}$	25°C		1.2	2	A
		-40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C			0.5	μA
		-40°C to 125°C			1	
PG leakage current	Normal operation, $V_{PG} = 10 \text{ V}$	25°C		0.02	0.5	μA
		-40°C to 125°C			0.5	
Output voltage temperature coefficient		-40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature					165	°C
\overline{EN} logic high (standby mode)	$2.5 \text{ V} \leq V_I \leq 6 \text{ V}$ $6 \text{ V} \leq V_I \leq 10 \text{ V}$	-40°C to 125°C		2		V
				2.7		
\overline{EN} logic low (active mode)	$2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C			0.5	V
		-40°C to 125°C			0.5	
\overline{EN} hysteresis voltage		25°C		50		mV
\overline{EN} input current	$0 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C	-0.5		0.5	μA
		-40°C to 125°C	-0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		-40°C to 125°C			2.5	
Minimum V_I for valid PG	$I_{PG} = 300 \mu\text{A}$ $I_{PG} = 300 \mu\text{A}$	25°C		1.06	1.5	V
		-40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TPS71H01 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSRT} = 1\text{ }\Omega$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T _J	TPS71H01Q			UNIT	
				MIN	TYP	MAX		
Reference voltage (measured at FB with OUT connected to FB)	$V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$		25°C	1.178			V	
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	1.143	1.213		V	
Reference voltage temperature coefficient			-40°C to 125°C	61 75			ppm/°C	
Pass-element series resistance (see Note 2)	$V_I = 2.4\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 150\text{ mA}$		25°C	0.7 1				
			-40°C to 125°C	1				
	$V_I = 2.4\text{ V}$, $150\text{ mA} \leq I_O \leq 500\text{ mA}$			25°C	0.83 1.3			
				-40°C to 125°C	1.3			
	$V_I = 2.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$			25°C	0.52 0.85			
				-40°C to 125°C	0.85			
$V_I = 3.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$			25°C	0.32				
			-40°C to 125°C	0.23				
Input regulation	$V_I = 2.5\text{ V to }10\text{ V}$, See Note 1	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	18			mV	
			-40°C to 125°C	25				
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$, See Note 1	$2.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	14			mV	
			-40°C to 125°C	25				
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$, See Note 1	$2.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	22			mV	
			-40°C to 125°C	54				
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	48 59			dB	
			-40°C to 125°C	44				
		$I_O = 500\text{ mA}$, See Note 1	25°C	45 54				
			-40°C to 125°C	44				
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2			$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT} = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	95			μV_{rms}	
		$C_O = 10\text{ }\mu\text{F}$	25°C	89				
		$C_O = 100\text{ }\mu\text{F}$	25°C	74				
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		-40°C to 125°C	1.101	1.145		V	
PG hysteresis voltage§	Measured at V_{FB}		25°C	12			mV	
PG output low voltage§	$I_{\text{PG}} = 400\text{ }\mu\text{A}$, $V_I = 2.13\text{ V}$		25°C	0.1 0.4			V	
			-40°C to 125°C	0.4				
FB input current			25°C	-10	0.1 10		nA	
			-40°C to 125°C	-20	20			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9\text{ V}$ and $I_O > 150\text{ mA}$ simultaneously, pass element $r_{\text{DS(on)}}$ increases (see Figure 27) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$$

$r_{\text{DS(on)}}$ is a function of both output current and input voltage. The parametric table lists $r_{\text{DS(on)}}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. (For other programmed values, see Figure 26.)

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TPS71H33 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ / $\text{CSR}^\dagger = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS71H33Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$, $I_O = 10\text{ mA}$		25°C	3.3			V
	$4.3\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 500\text{ mA}$		-40°C to 125°C	3.23		3.37	
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 3.23\text{ V}$		25°C	4.5		7	mV
			-40°C to 125°C	8			
	$I_O = 100\text{ mA}$, $V_I = 3.23\text{ V}$		25°C	47		60	
			-40°C to 125°C	80			
	$I_O = 500\text{ mA}$, $V_I = 3.23\text{ V}$		25°C	235		300	
			-40°C to 125°C	400			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 3.23\text{ V}$	25°C	0.47		0.6	Ω
			-40°C to 125°C	0.8			
Input regulation	$V_I = 4.3\text{ V}$ to 10 V, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		25°C			20	mV
			-40°C to 125°C	27			
Output regulation	$I_O = 5\text{ mA}$ to 500 mA, $4.3\text{ V} \leq V_I \leq 10\text{ V}$		25°C	21		38	mV
			-40°C to 125°C	75			
	$I_O = 50\text{ }\mu\text{A}$ to 500 mA, $4.3\text{ V} \leq V_I \leq 10\text{ V}$		25°C	30		60	mV
			-40°C to 125°C	120			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	43		54	dB
			-40°C to 125°C	40			
		$I_O = 500\text{ mA}$	25°C	39		49	
			-40°C to 125°C	36			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		μV_{rms}	
		$C_O = 10\text{ }\mu\text{F}$	25°C	228			
		$C_O = 100\text{ }\mu\text{F}$	25°C	159			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	2.868		3	V
PG hysteresis voltage			25°C	35			mV
PG output low voltage	$I_{\text{PG}} = 1\text{ mA}$, $V_I = 2.8\text{ V}$		25°C	0.22		0.4	V
			-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TPS71H48 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 5.85\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ /CSRT† = 1 Ω , SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS71H48Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 5.85\text{ V}$, $5.85\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 10\text{ mA}$, $5\text{ mA} \leq I_O \leq 500\text{ mA}$	25°C –40°C to 125°C	4.85			V
				4.75	4.95		
Dropout voltage	$I_O = 10\text{ mA}$, $I_O = 100\text{ mA}$,	$V_I = 4.75\text{ V}$, $V_I = 4.75\text{ V}$	25°C	2.9	6	mV	
			–40°C to 125°C		8		
	25°C	30	37				
	–40°C to 125°C		54				
	25°C	150	180				
	–40°C to 125°C		250				
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$	$V_I = 4.75\text{ V}$,	25°C	0.32	0.35	Ω	
			–40°C to 125°C		0.52		
Input regulation	$V_I = 5.85\text{ V to } 10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	27		mV	
			–40°C to 125°C	37			
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$,	$5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C	12	42	mV	
			–40°C to 125°C	80			
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$,	$5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C	42	60	mV	
			–40°C to 125°C	130			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	42	53	dB	
			–40°C to 125°C	39			
		$I_O = 500\text{ mA}$	25°C	39	50		
			–40°C to 125°C	35			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, CSRT† = 1 Ω	$C_O = 4.7\text{ }\mu\text{F}$	25°C	410		μV_{rms}	
		$C_O = 10\text{ }\mu\text{F}$	25°C	328			
		$C_O = 100\text{ }\mu\text{F}$	25°C	212			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	4.5	4.7	V	
PG hysteresis voltage			25°C	50		mV	
PG output low voltage	$I_{\text{PG}} = 1.2\text{ mA}$,	$V_I = 4.12\text{ V}$	25°C	0.2	0.4	V	
			–40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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TPS71H50 electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSRT}^\dagger = 1\text{ }\Omega$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS71H50Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V}$,	$I_O = 10\text{ mA}$	25°C	5			V
	$6\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	4.9	5.1		
Dropout voltage	$I_O = 10\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	2.9		6	mV
			-40°C to 125°C			8	
	$I_O = 100\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	27		32	
			-40°C to 125°C			47	
	$I_O = 500\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	146		170	
			-40°C to 125°C			230	
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$,	$V_I = 4.88\text{ V}$,	25°C	0.29		0.32	Ω
			$I_O = 500\text{ mA}$	-40°C to 125°C			
Input regulation	$V_I = 6\text{ V}$ to 10 V,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C			25	mV
			-40°C to 125°C			32	
Output regulation	$I_O = 5\text{ mA}$ to 500 mA,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	30		45	mV
			-40°C to 125°C			86	
	$I_O = 50\text{ }\mu\text{A}$ to 500 mA,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	45		65	mV
			-40°C to 125°C			140	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	45	55		dB
			-40°C to 125°C	40			
		$I_O = 500\text{ mA}$	25°C	42	52		
			-40°C to 125°C	36			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$,	$\text{CSRT}^\dagger = 1\text{ }\Omega$	25°C	430		μV_{rms}	
			25°C	345			
			25°C	220			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	4.55	4.75		V
PG hysteresis voltage			25°C	53		mV	
PG output low voltage	$I_{\text{PG}} = 1.2\text{ mA}$,	$V_I = 4.25\text{ V}$	25°C	0.2		0.4	V
			-40°C to 125°C			0.4	

† CSRT refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	5
		vs Input voltage	6
		vs Free-air temperature	7
V_{DO}	Typical dropout voltage	vs Output current	8
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	9
ΔV_O	Change in output voltage	vs Free-air temperature	10
V_O	Output voltage	vs Input voltage	11
ΔV_O	Change in output voltage	vs Input voltage	12
V_O	Output voltage	vs Output current	13
			14
			15
			16
			17
Ripple rejection	Ripple rejection	vs Frequency	18
			19
			20
			21
Output spectral noise density	Output spectral noise density	vs Frequency	22
			23
			24
			25
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	25
R	Divider resistance	vs Free-air temperature	26
$I_{I(SENSE)}$	SENSE current	vs Free-air temperature	27
	FB leakage current	vs Free-air temperature	28
V_I	Minimum input voltage for active-pass element	vs Free-air temperature	29
	Minimum input voltage for valid PG	vs Free-air temperature	30
$I_{I(EN)}$	Input current (\overline{EN})	vs Free-air temperature	31
	Output voltage response from Enable (\overline{EN})		32
V_{PG}	Power-good (PG) voltage	vs Output voltage	33
CSR	Compensation series resistance	vs Output current	34
		35	
CSR	Compensation series resistance	vs Ceramic capacitance	36
		37	
CSR	Compensation series resistance	vs Output current	38
		39	
CSR	Compensation series resistance	vs Ceramic capacitance	40
		41	

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
OUTPUT CURRENT

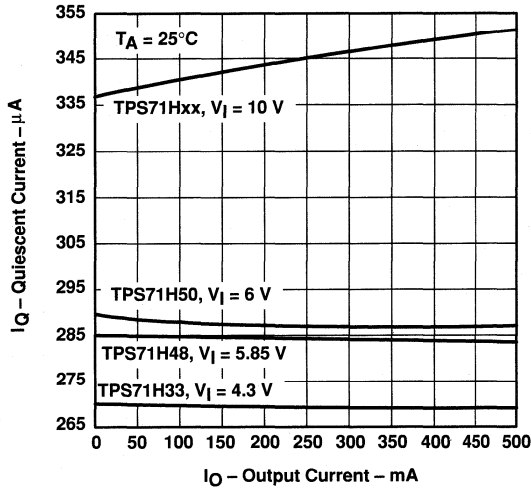


Figure 5

QUIESCENT CURRENT
vs
INPUT VOLTAGE

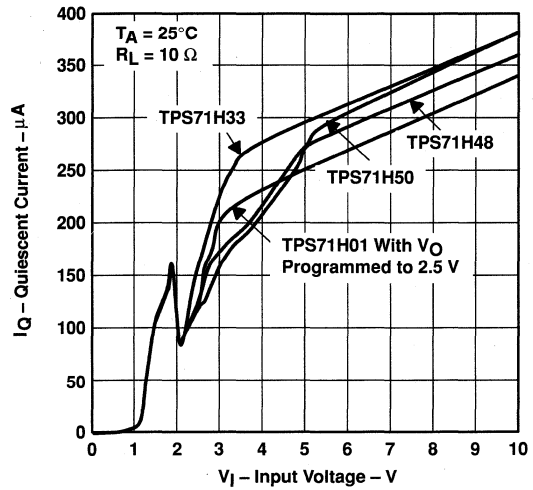


Figure 6

TPS71H48Q
QUIESCENT CURRENT
vs
FREE-AIR TEMPERATURE

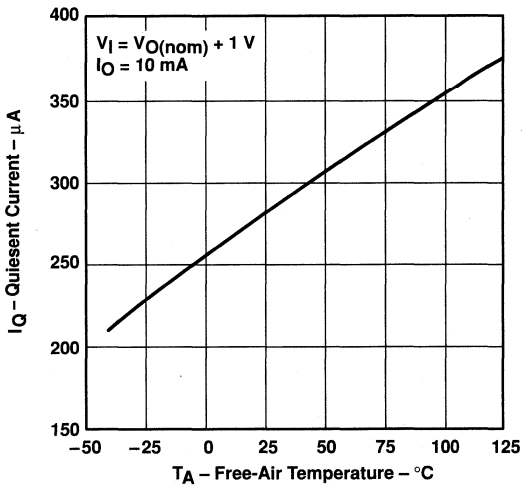


Figure 7

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

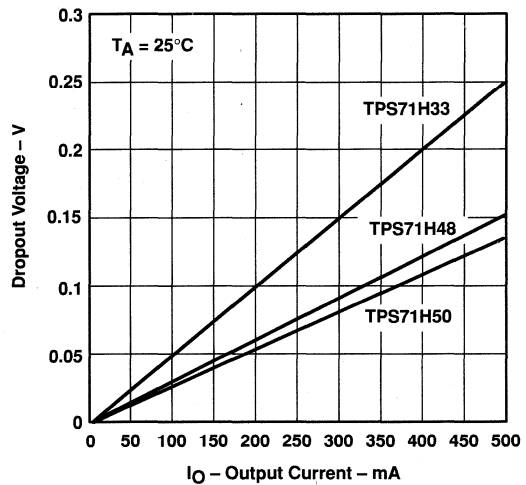


Figure 8



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

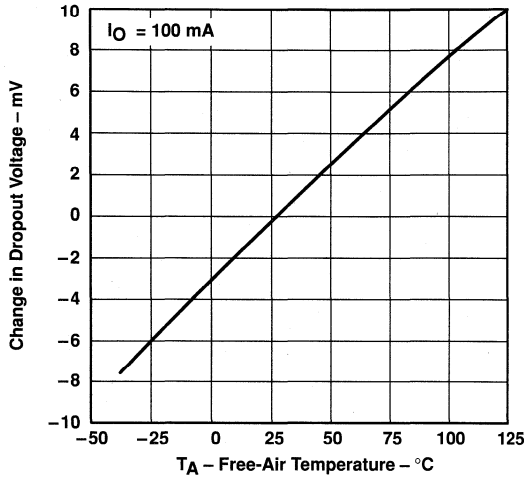


Figure 9

CHANGE IN OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

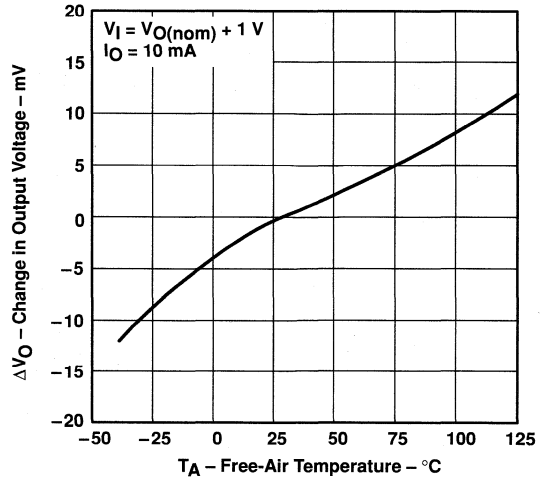


Figure 10

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

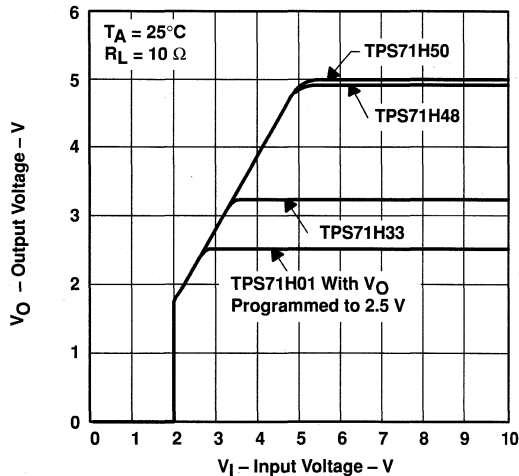


Figure 11

CHANGE IN OUTPUT VOLTAGE
vs
INPUT VOLTAGE

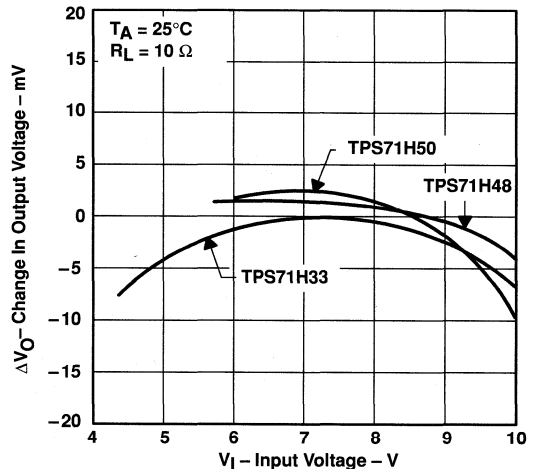


Figure 12

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TPS71H01Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

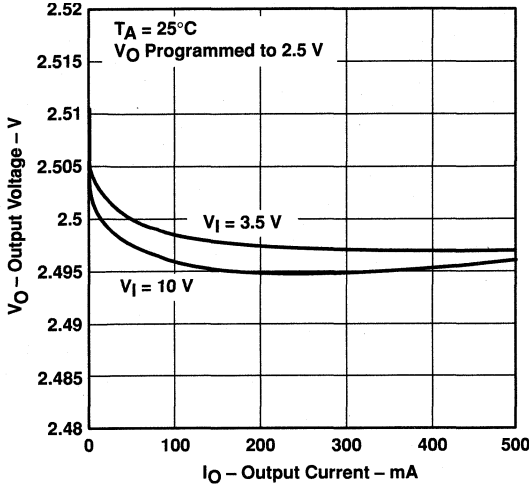


Figure 13

TPS71H33Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

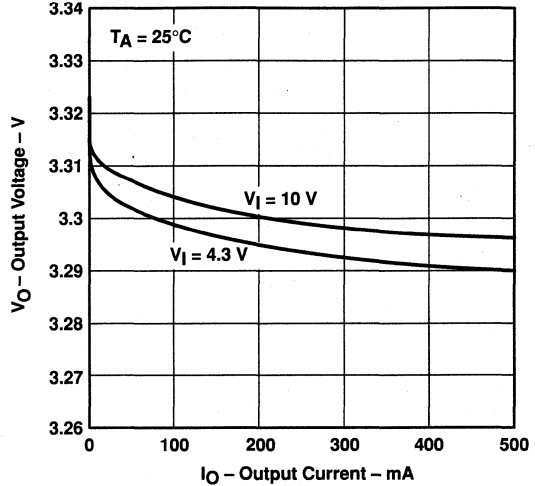


Figure 14

TPS71H48Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

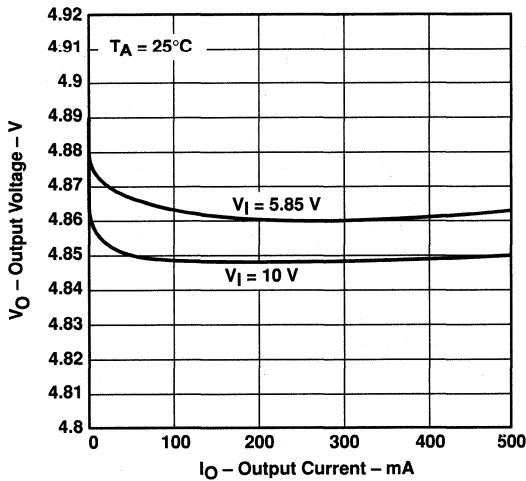


Figure 15

TPS71H50Q
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

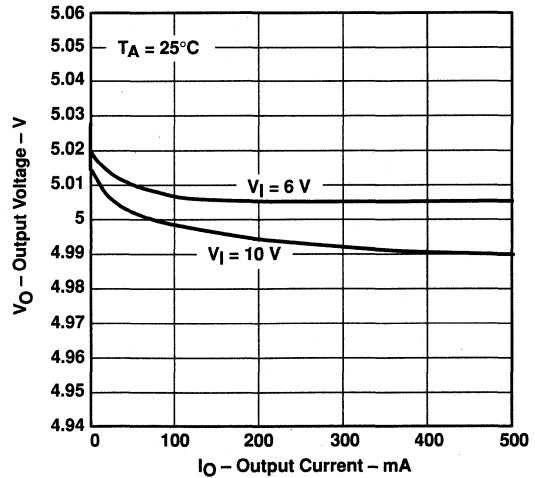
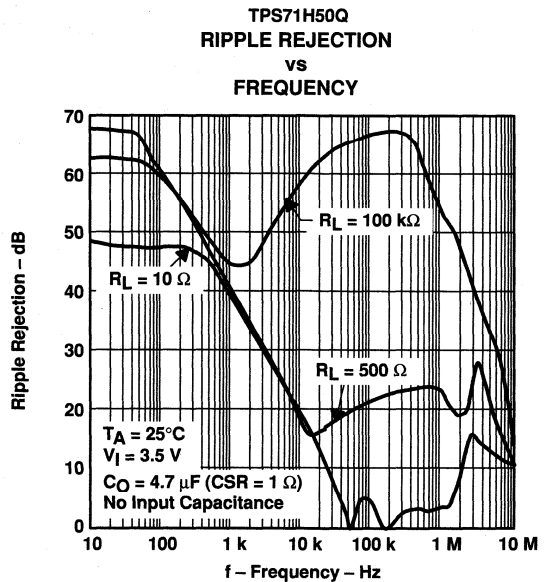
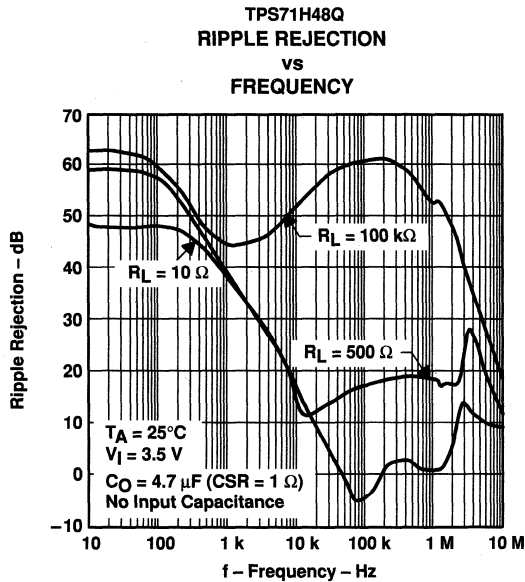
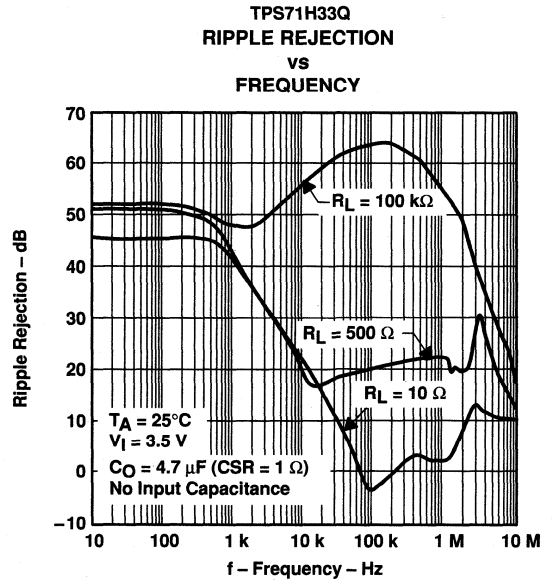
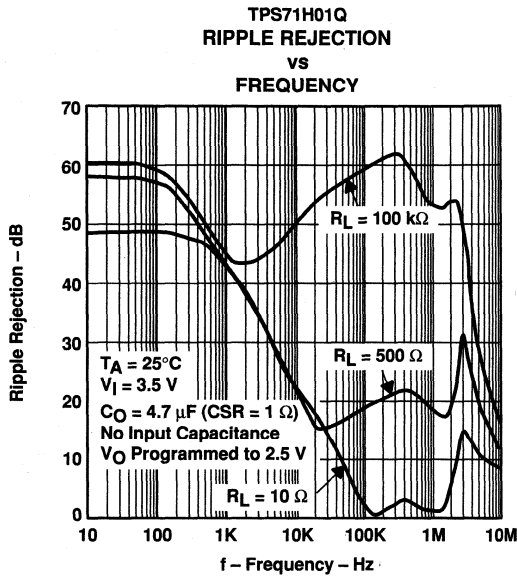


Figure 16

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TPS71H01Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

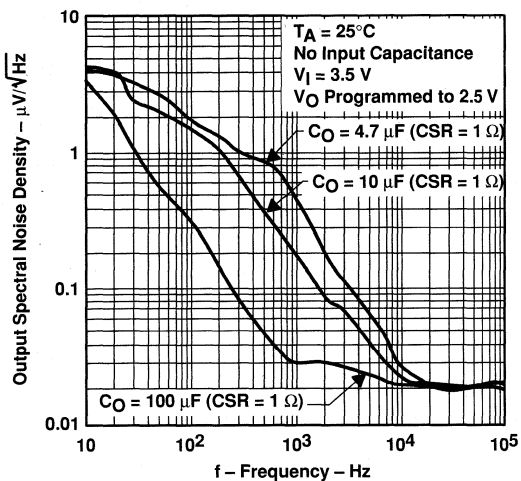


Figure 21

TPS71H33Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

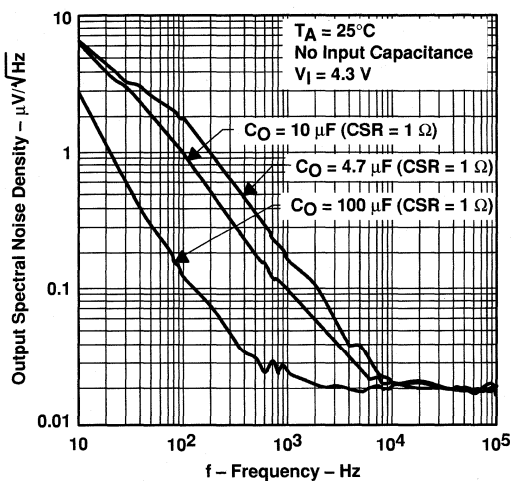


Figure 22

TPS71H48Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

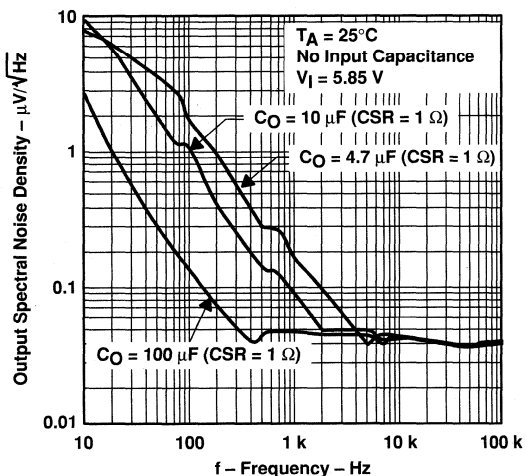


Figure 23

TPS71H50Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

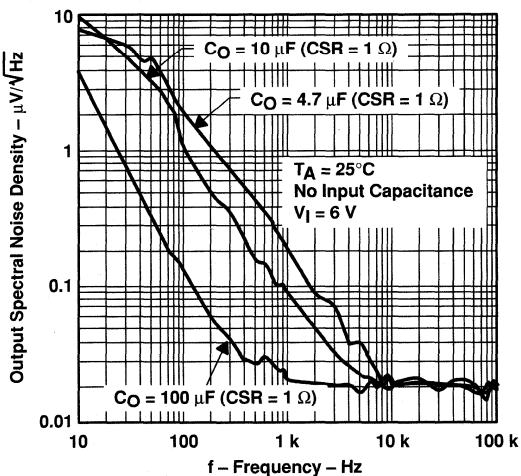


Figure 24



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TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**PASS-ELEMENT RESISTANCE
vs
INPUT VOLTAGE**

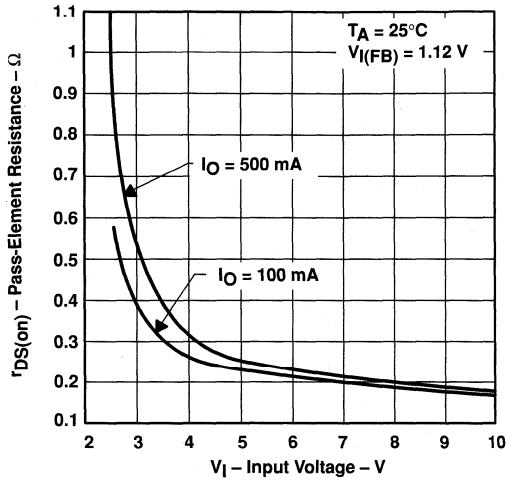


Figure 25

**DIVIDER RESISTANCE
vs
FREE-AIR TEMPERATURE**

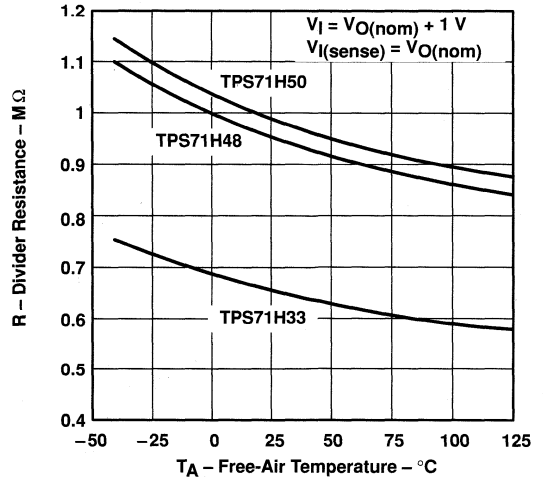


Figure 26

**FIXED-OUTPUT VERSIONS
SENSE PIN CURRENT
vs
FREE-AIR TEMPERATURE**

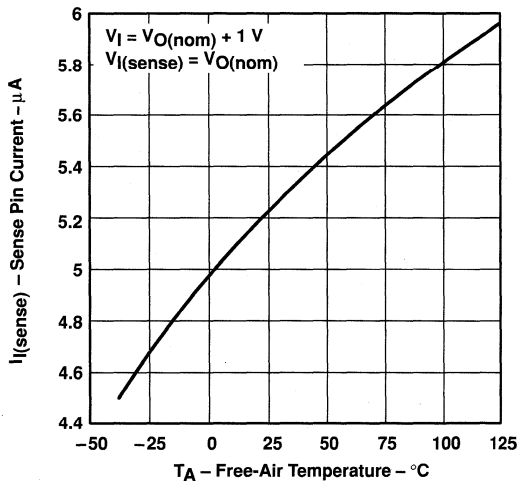


Figure 27

**ADJUSTABLE VERSION
FB LEAKAGE CURRENT
vs
FREE-AIR TEMPERATURE**

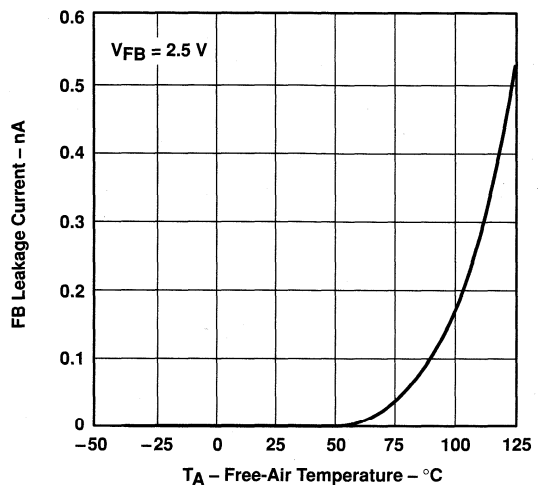


Figure 28

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE
PASS ELEMENT
vs
FREE-AIR TEMPERATURE

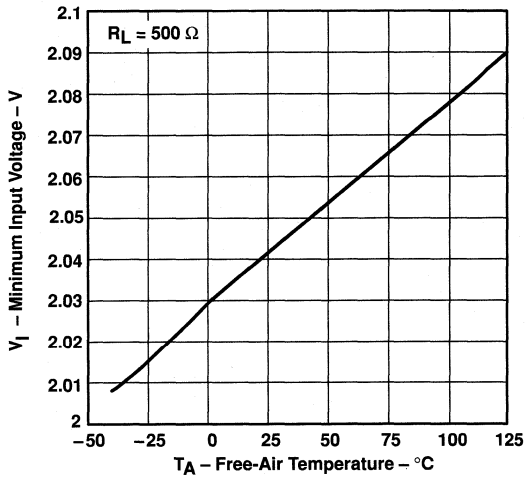


Figure 29

MINIMUM INPUT VOLTAGE FOR VALID
POWER GOOD (PG)
vs
FREE-AIR TEMPERATURE

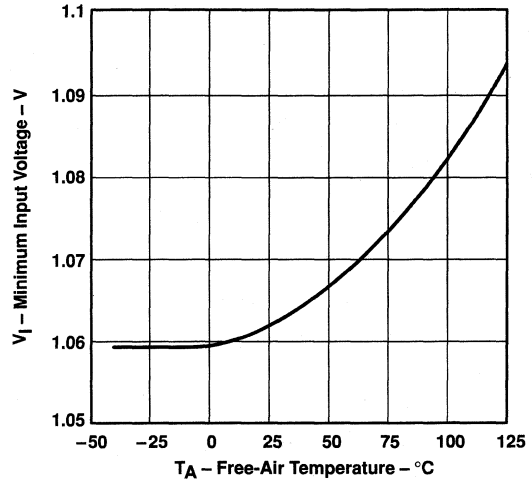


Figure 30

EN INPUT CURRENT
vs
FREE-AIR TEMPERATURE

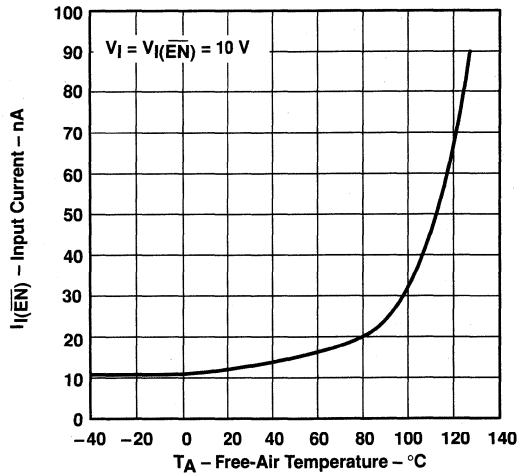


Figure 31

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE (EN)

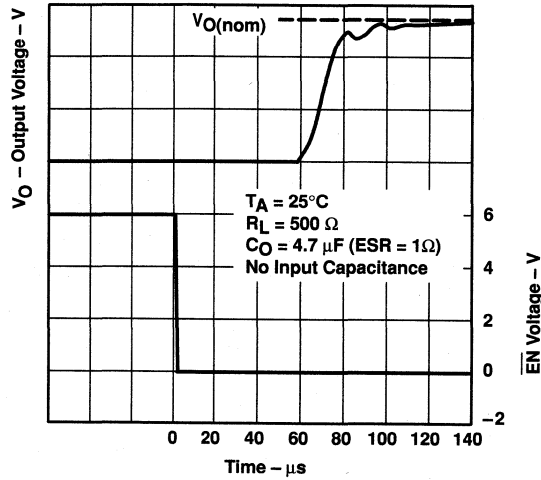


Figure 32

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

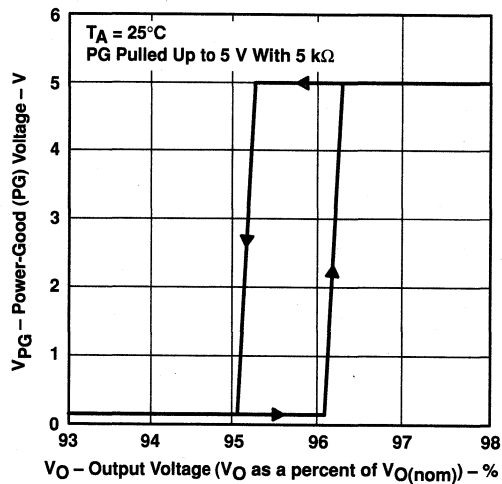


Figure 33

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

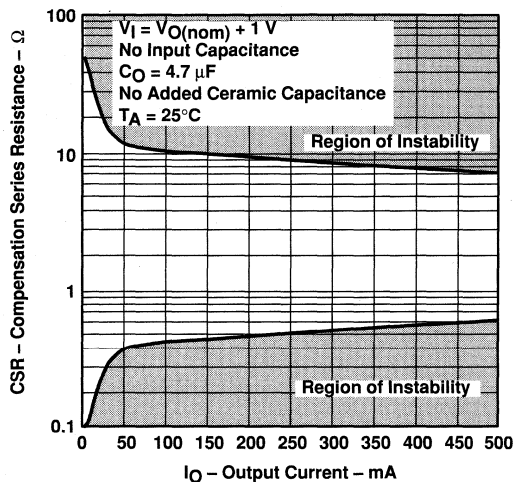


Figure 34

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

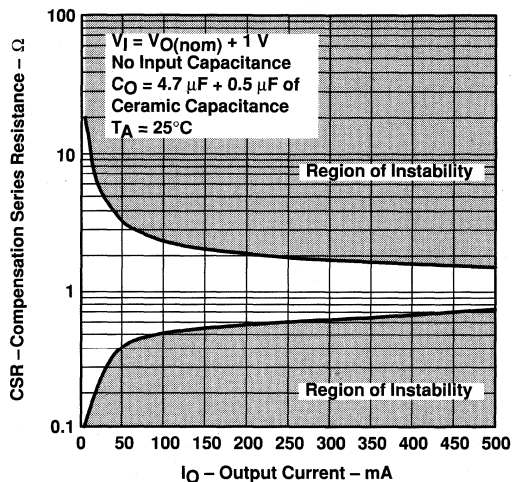


Figure 35

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

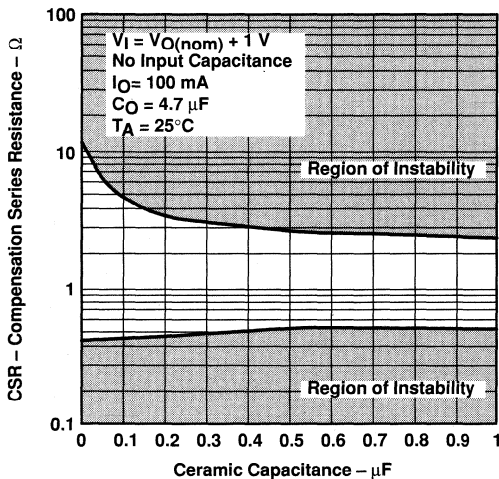


Figure 36

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

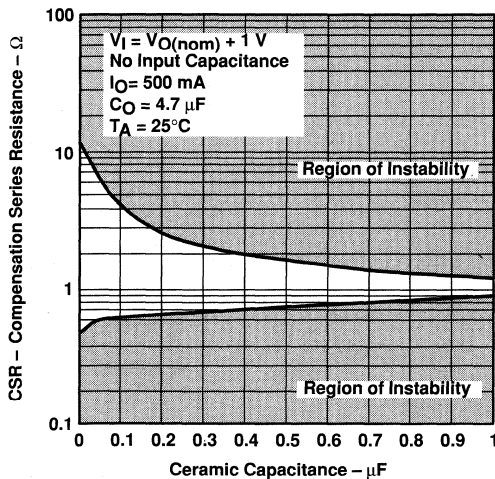


Figure 37

TYPICAL CHARACTERISTICS

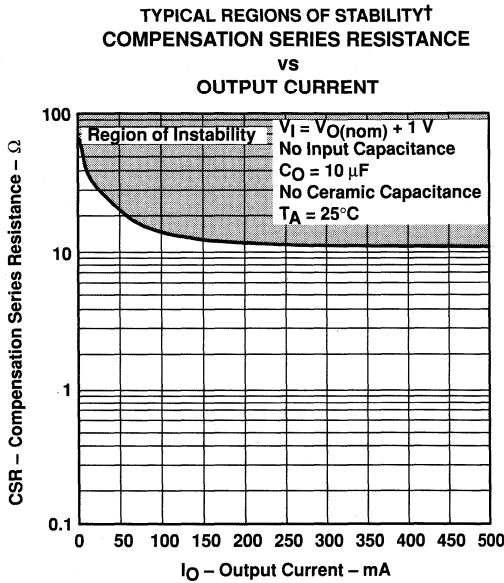


Figure 38

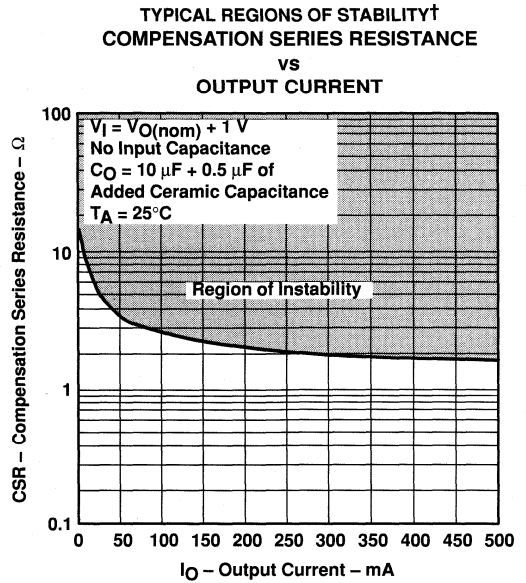


Figure 39

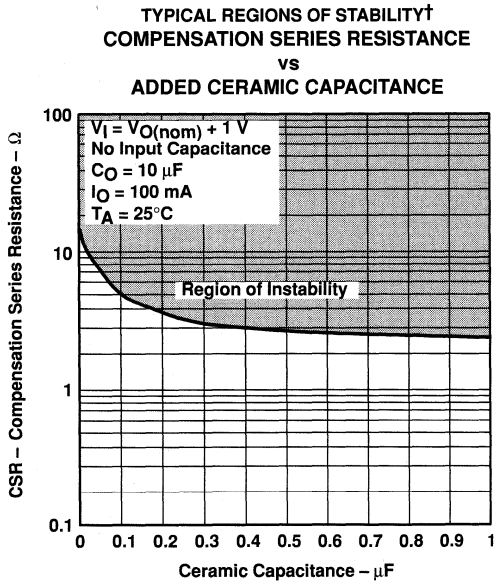


Figure 40

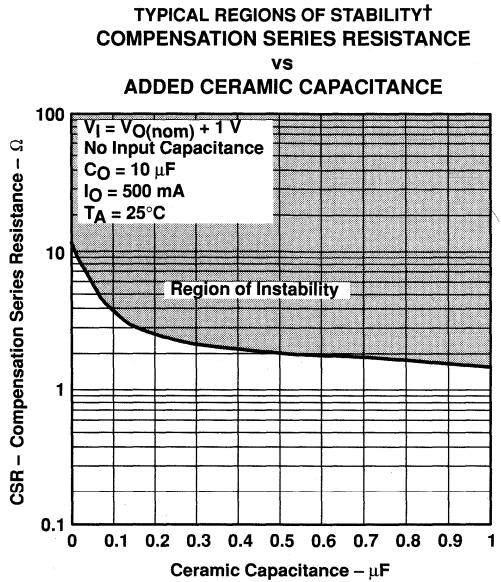


Figure 41

† CSR values below 0.1 Ω are not recommended.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

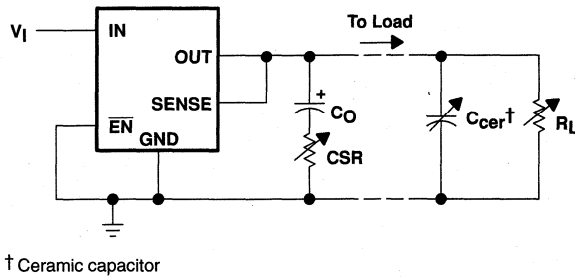


Figure 42. Test Circuit for Typical Regions of Stability (see Figures 34 through 41)

THERMAL INFORMATION

standard TSSOP-20

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 43 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 44. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board ($L \times W \times H = 3.2 \text{ inch} \times 3.2 \text{ inch} \times 0.062 \text{ inch}$); the board traces and heat sink area are 1-oz (per square foot) copper.

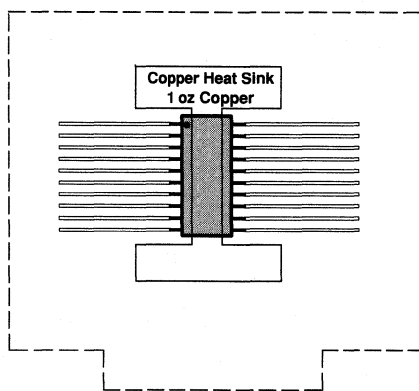


Figure 43. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

Figure 45 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is $0.815 \text{ W/m} \times ^\circ\text{C}$.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

standard TSSOP-20 (continued)

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
vs
AIR FLOW

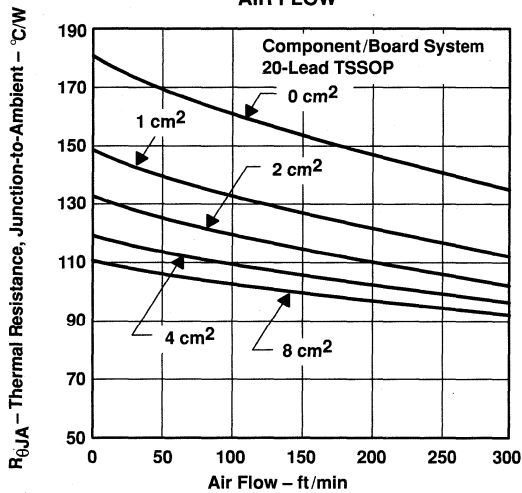


Figure 44

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT
vs
AIR FLOW

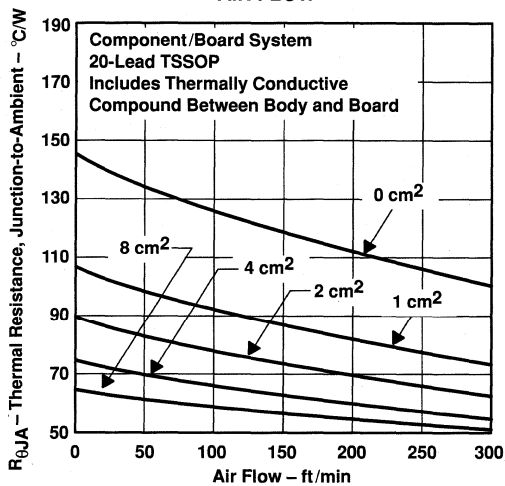


Figure 45

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature (i.e., 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation).

This limit should then be applied to the internal power dissipated by the TPS71Hxx regulator. The equation for calculating total internal power dissipation of the TPS71Hxx is:

$$P_{D(total)} = (V_I - V_O) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS71Hxx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \cdot I_O$$

THERMAL INFORMATION

standard TSSOP-20 (continued)

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55^\circ\text{C}$, airflow = 100 ft/min, copper heat sink area = 1 cm², the maximum power-dissipation limit can be calculated. As indicated in Figure 45, the system $R_{\theta\text{JA}}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{R_{\theta\text{JA}(\text{system})}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{94^\circ\text{C/W}} = 745 \text{ mW}$$

If the system implements a TPS71H48 regulator where $V_I = 6 \text{ V}$ and $I_O = 385 \text{ mA}$, the internal power dissipation is:

$$P_{D(\text{total})} = (V_I - V_O) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

thermally enhanced TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 46(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

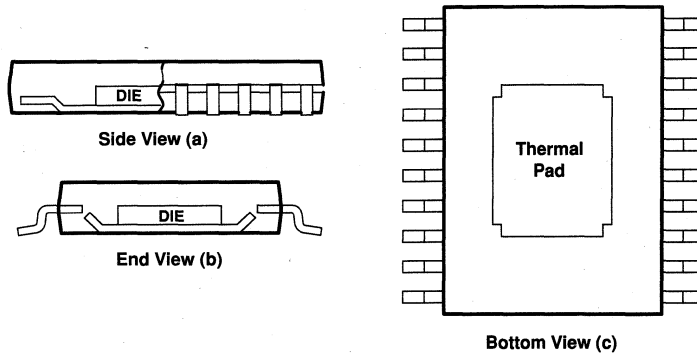


Figure 46. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 48(a), 8 cm² of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 47 and 48). The line drawn at 0.3 cm² in Figures 47 and 48 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 50.

The thermal pad is directly connected to the substrate of the IC, which for the TPS71HxxQPWP series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWB can be a ground plane or left electrically isolated. In other TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 12 independent leads that can be used as inputs and outputs (Note: leads 1, 2, 9, 10, 11, 12, 19, and 20 are internally connected to the thermal pad and the IC substrate).

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

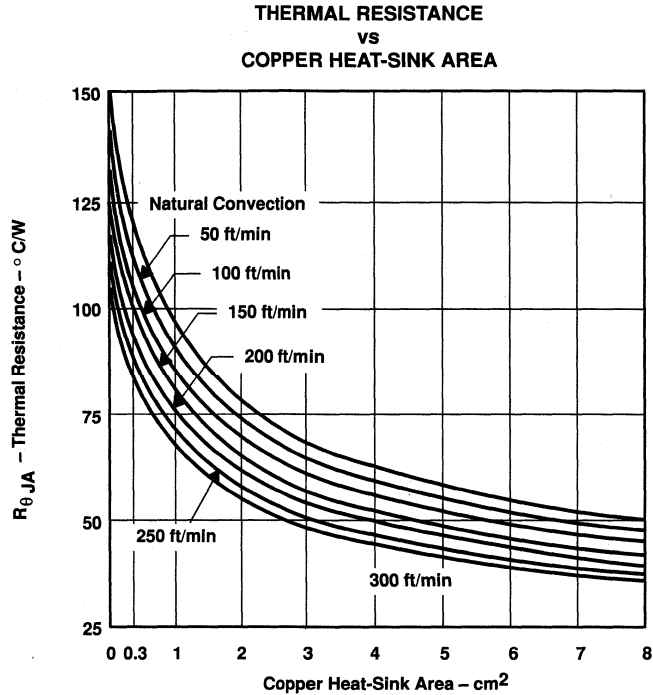


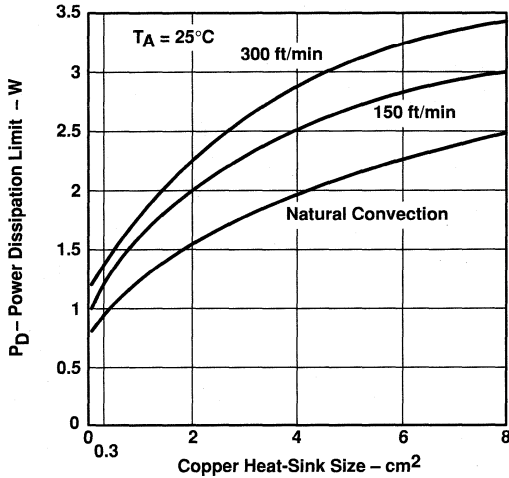
Figure 47

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q
LOW-DROPOUT VOLTAGE REGULATORS

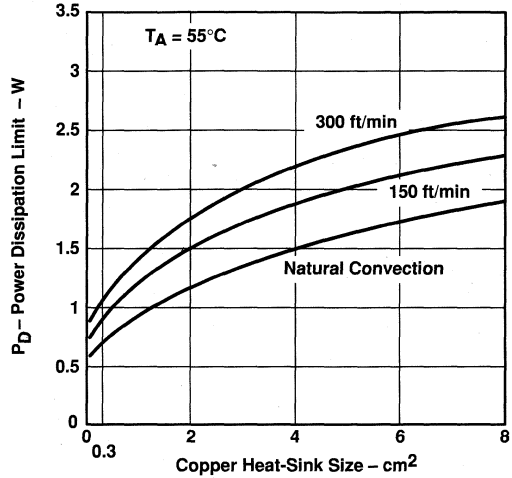
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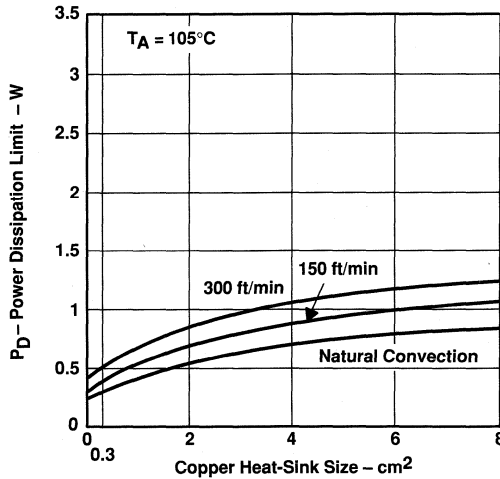
thermally enhanced TSSOP-20 (continued)



(a)



(b)



(c)

Figure 48. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

Figure 49 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figures 47 and 48. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 47 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.

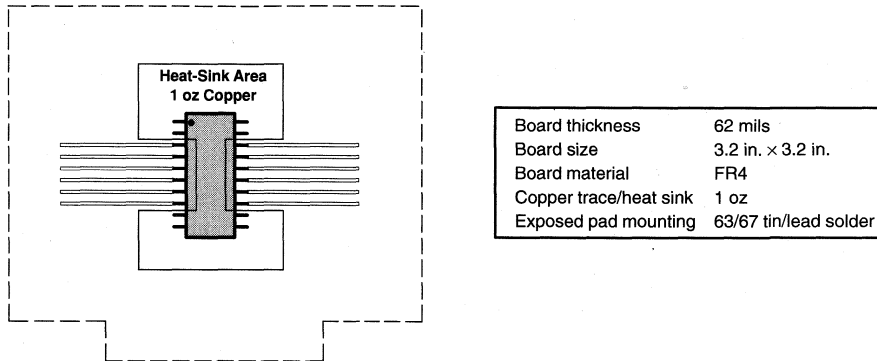


Figure 49. PWB Layout (Including Copper Heatsink Area) for Thermally Enhanced PWP Package

From Figure 47, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}}$$

Where

T_{Jmax} is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS71H33QPWP regulator. The equation for calculating total internal power dissipation of the TPS71H33QPWP is:

$$P_{D(total)} = (V_I - V_O) \times I_O + V_I \times I_Q$$

Since the quiescent current of the TPS71H33QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \times I_O$$

For the case where $T_A = 55^\circ\text{C}$, airflow = 200 ft/min, copper heat-sink area = 4 cm², the maximum power-dissipation limit can be calculated. First, from Figure 47, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{50^\circ\text{C/W}} = 1.4 \text{ W}$$

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

If the system implements a TPS71H33QPWP regulator, where $V_I = 6\text{ V}$ and $I_O = 500\text{ mA}$, the internal power dissipation is:

$$P_{D(\text{total})} = (V_I - V_O) \times I_O = (6 - 3.3) \times 0.5 = 1.35\text{ W}$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

Since the thermal pad is not a primary connection for an electrical signal, the importance of the electrical connection is not significant. The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 47 and 48 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 50 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 2, 9, 10, 11, 12, 19, and 20.

reliability information

This section includes demonstrated reliability test results obtained from the qualification program. Accelerated tests are performed at high-stress conditions so that product reliability can be established during a relatively short test duration. Specific stress conditions are chosen to represent accelerated versions of various device-application environments and allow meaningful extrapolation to normal operating conditions.

component level reliability test results

preconditioning

Preconditioning of components prior to reliability testing is employed to simulate the actual board assembly process used by the customer. This ensures that reliability test results are more representative of those that would be seen in the final application. The general form of the preconditioning sequence includes a moisture soak followed by multiple vapor-phase-reflow or infrared-reflow solder exposures. All components used in the following reliability tests were preconditioned in accordance with JEDEC Test Method A113 for Level 1 (not moisture-sensitive) products.

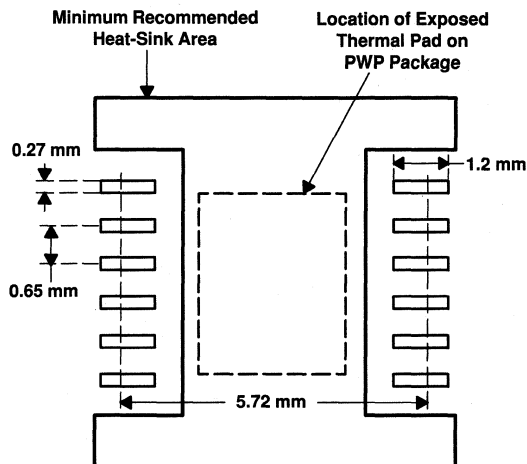


Figure 50. PWP Package Land Pattern

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

high-temperature life test

High-temperature life testing is used to demonstrate long-term reliability of the product under bias. The potential failure mechanisms evaluated with this stress are those associated with dielectric integrity and design or process sensitivity to mobile-ion phenomena. Components are tested at an elevated ambient temperature of 155°C for an extended period. Results are derated using the Arrhenius equation to an equivalent number of unit hours at a representative application temperature. The corresponding predicted failure rate is expressed in FITs, or failures per billion device-hours. The failure rate shown in this case is data-limited since no actual failures were experienced during qualification testing.

PREDICTED LONG-TERM FAILURE RATE

Number of Units	Equivalent Unit Hours at 55°C and 0.7 eV	FITs at 50% CL
325	24,468,090	36.2

biased humidity test

Biased humidity testing is used to evaluate the effects of moisture penetration on plastic-encapsulated devices under bias. This stress verifies the integrity of the package construction and the die passivation system. The primary potential failure mechanism is electrolytic corrosion. Components are biased in a low power state to reduce heat dissipation and are subjected to a 120°C, 85%-relative-humidity environment for 100 hours.

BIASED HUMIDITY TEST RESULTS

Equivalent Unit Hours at 85°C and 85% RH	Failures
357,000	0

autoclave test

The autoclave stress is used to assess the capabilities of the die and package construction materials with respect to moisture ingress and extended exposure. Predominant failure mechanisms include leakage currents that result from internal moisture accumulation and galvanic corrosion resulting from reactions with any present ionic contaminants. Components are subjected to a 121°C, 15 PSIG, 100%-relative-humidity environment for 240 hours.

AUTOCLAVE TEST RESULTS

Total Unit Hours	Failures
54,720	0

thermal shock test

Thermal shock testing is used to evaluate the capability of the component to withstand mechanical stress resulting from differences in thermal coefficients of expansion among the die and package construction materials. Failure mechanisms are typically related to physical damage at interface locations between different materials. Components are cycled between -65°C and 150°C in liquid mediums for a total duration of 1000 cycles.

THERMAL SHOCK TEST RESULTS

Total Unit Cycles	Failures
345,000	0

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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THERMAL INFORMATION

PWB assembly level reliability results

temperature cycle test

Temperature cycle testing of the PWB assembly is used to evaluate the capability of the assembly to withstand mechanical stress resulting from the differences in thermal coefficients of expansion among die, package, and PWB board materials. This testing is also used to sufficiently age the soldered thermal connection between the thermal pad and the Cu trace on the FR4 board and evaluate the degradation of the thermal resistance for a board-mounted test unit. The assemblies were cycled between temperature extremes of -40°C and 125°C for a total duration of 730 cycles.

TEMPERATURE CYCLE TEST RESULTS

Total Unit Cycles	Failures	Average Change in $R_{\theta\text{JA}}(\text{system})$
36,500	0	-0.41%

solderability test

Solderability testing is used to simulate actual board-mount performance in a reflow process.

Solderability testing is conducted as follows: The test devices are first steam-aged for 8 hours. A stencil is used to apply a solder-paste terminal pattern on a ceramic substrate (nominal stencil thickness is 0.005 inch). The test units are manually placed on the solder-paste footprint with proper implements to avoid contamination. The ceramic substrate and components are subjected to the IR reflow process as follows:

IR REFLOW PROCESS

	PREHEAT SOAK	REFLOW
Temperature	150°C to 170°C	215°C to 230°C
Time	60 sec	60 sec

After cooling to room temperature, the component is removed from the ceramic substrate and the component terminals are subjected to visual inspection at 10X magnification.

Test results are acceptable if all terminations exhibit a continuous solder coating free of defects for a minimum 95% of the critical surface area of any individual termination. Causes for rejection include: dewetting, nonwetting, and pin holes. The component leads and the exposed thermal pad were evaluated against this criteria.

SOLDERABILITY TEST RESULTS

Number of Test Units	Failures
22	0

X-ray test

X-ray testing is used to examine and quantify the voiding of the soldered attachment between the thermal pad and the PWB copper trace. Voiding between 20% and 50% was observed on a 49-piece sample.



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

The TPS71Hxx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71Hxx family includes three fixed-output voltage regulators: the TPS71H33 (3.3 V), the TPS71H48 (4.85 V), and the TPS71H50 (5 V). The family also offers an adjustable device, the TPS71H01 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71Hxx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71Hxx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71Hxx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71Hxx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71Hxx family is a 4.85-V regulator, the TPS71H48. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within $\pm 2\%$, allows for operation within the low-end limit of 5-V systems specified to $\pm 5\%$ tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71Hxx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA . If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs .

minimum load requirements

The TPS71Hxx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.



TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μ F) improves load transient response and noise rejection if the TPS71Hxx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS71Hxx family requires an output capacitor for stability. A low-ESR 10- μ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 51). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m Ω (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- μ F devices can be screened for ESR. Figures 34 through 41 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μ F), the output capacitance can be reduced to 4.7 μ F, provided ESR is maintained between 0.7 and 2.5 Ω . Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5- Ω to 1- Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 34 through 41), minimum ESR is not a problem when using 10- μ F or larger output capacitors.

The following is a partial listing of surface-mount capacitors usable with the TPS71Hxx family. This information (along with the ESR graphs, Figures 34 through 41) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF , 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF , 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3

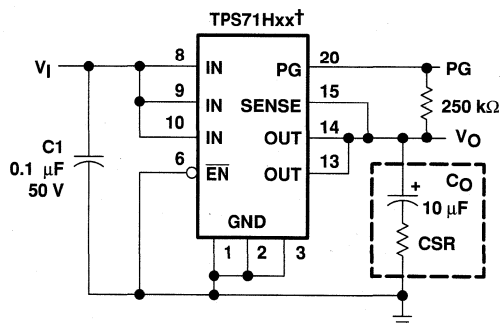
Load < 200 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF , 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF , 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF , 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF , 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF , 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF , 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF , 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF , 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF , 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF , 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.



† TPS71H33, TPS71H48, TPS71H50 (fixed-voltage options)

Figure 51. Typical Application Circuit

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

programming the TPS71H01 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 52. The equation governing the output voltage is:

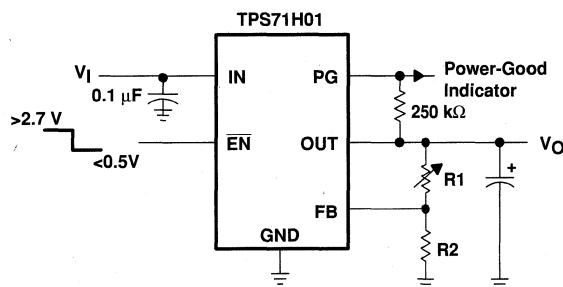
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where

V_{ref} = reference voltage, 1.178 V typ

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. A recommended value for R2 is 169 k Ω with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	k Ω
3.3 V	309	169	k Ω
3.6 V	348	169	k Ω
4 V	402	169	k Ω
5 V	549	169	k Ω
6.4 V	750	169	k Ω

Figure 52. TPS71H01 Adjustable LDO Regulator Programming

power-good indicator

The TPS71Hxx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

TPS71H01Q, TPS71H33Q, TPS71H48Q, TPS71H50Q LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

regulator protection

The TPS71Hxx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71Hxx also features internal current limiting and thermal protection. During normal operation, the TPS71Hxx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.



TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY

MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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- Available in 5-V, 4.85-V, 3.3-V, 3.0-V, 2.75-V[§], and 2.5-V Fixed-Output and Adjustable Versions
- Dropout Voltage <85 mV Max at $I_O = 100$ mA (TPS7250)
- Low Quiescent Current, Independent of Load, 180 μ A Typ
- 8-Pin SOIC and 8-Pin TSSOP Package
- Output Regulated to $\pm 2\%$ Over Full Operating Range for Fixed-Output Versions
- Extremely Low Sleep-State Current, 0.5 μ A Max
- Power-Good (PG) Status Output

description

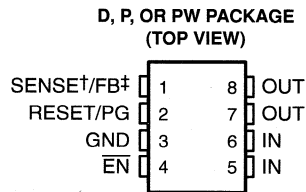
The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation, and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and for designs where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low – maximum of 85 mV at 100 mA of load current (TPS7250) – and is directly proportional to the load current (see Figure 1). Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 μ A maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage and micropower operation result in a significant increase in system battery operating life.

The TPS72xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 0.5 μ A maximum at $T_J = 25^\circ\text{C}$. Other features include a power-good function that reports low output voltage and may be used to implement a power-on reset or a low-battery indicator.

The TPS72xx is offered in 2.5-V, 2.75-V[§], 3-V, 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version).

[§] This device is in the product preview stage of development. Please contact the local TI sales office for availability.



† SENSE – Fixed voltage options only (TPS7225, TPS7228[§], TPS7230, TPS7233, TPS7248, and TPS7250)

‡ FB – Adjustable version only (TPS7201)

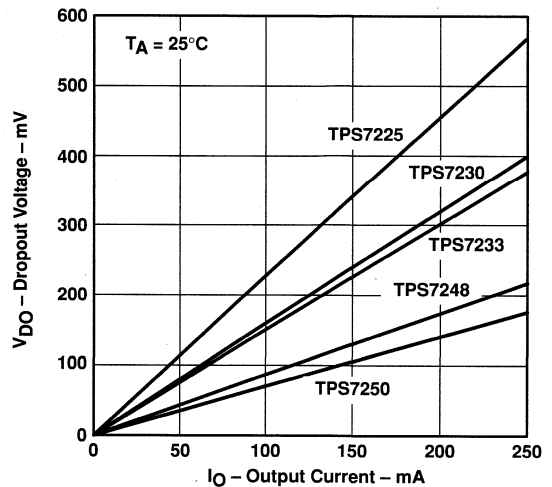


Figure 1. Typical Dropout Voltage Versus Output Current

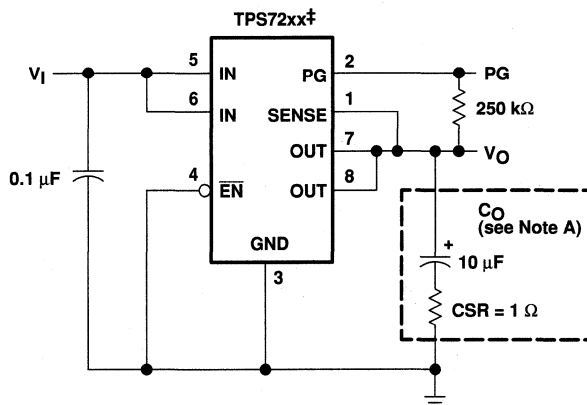
**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	SMALL OUTLINE (D)	PDIP (P)	TSSOP (PW)	
-55°C to 150°C	4.9	5	5.1	TPS7250QD	TPS7250QP	TPS7250QPWR	TPS7250Y
	4.75	4.85	4.95	TPS7248QD	TPS7248QP	TPS7248QPWR	TPS7248Y
	3.23	3.3	3.37	TPS7233QD	TPS7233QP	TPS7233QPWR	TPS7233Y
	2.94	3	3.06	TPS7230QD	TPS7230QP	TPS7230QPWR	TPS7230Y
	2.69	2.75	2.81	TPS7228QD†	TPS7228QP†	TPS7228QPWR†	TPS7228Y†
	2.45	2.5	2.55	TPS7225QD	TPS7225QP	TPS7225QPWR	TPS7225Y
	Adjustable 1.2 V to 9.75 V			TPS7201QD	TPS7201QP	TPS7201QPWR	TPS7201Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7250QDR). The PW package is only available left-end taped and reeled. The TPS7201Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.



‡ TPS7225Q, TPS7228Q†, TPS7230Q, TPS7233Q, TPS7248Q, TPS7250Q
 (fixed-voltage options)

NOTE B. Capacitor selection is nontrivial. See application information section for details.

Figure 2. Typical Application Configuration

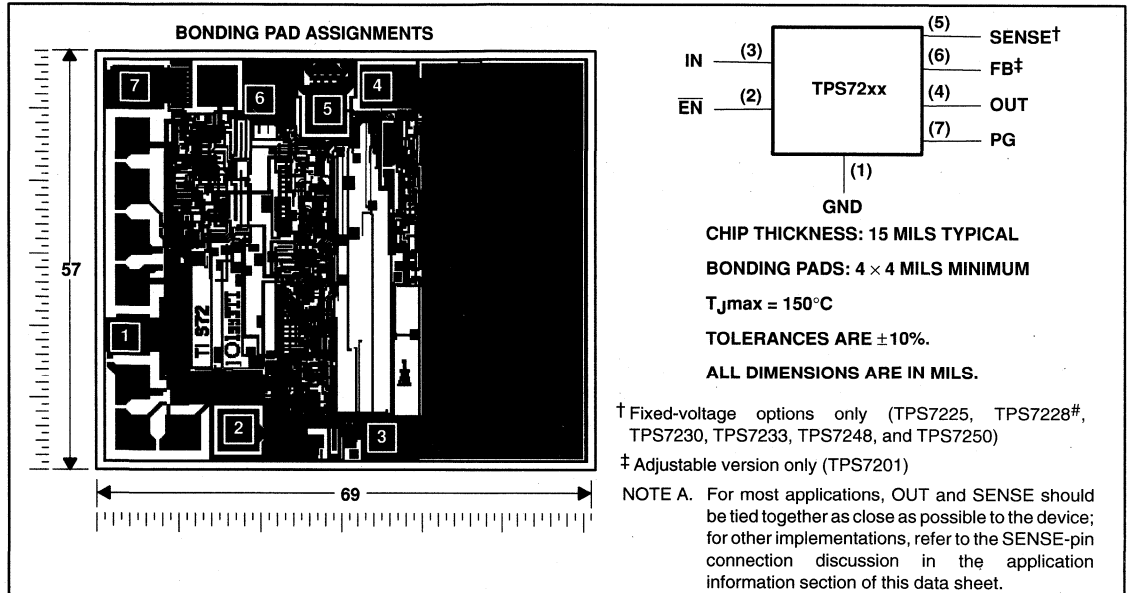
† This device is in the product preview stage of development. Please contact the local TI sales office for availability.

TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

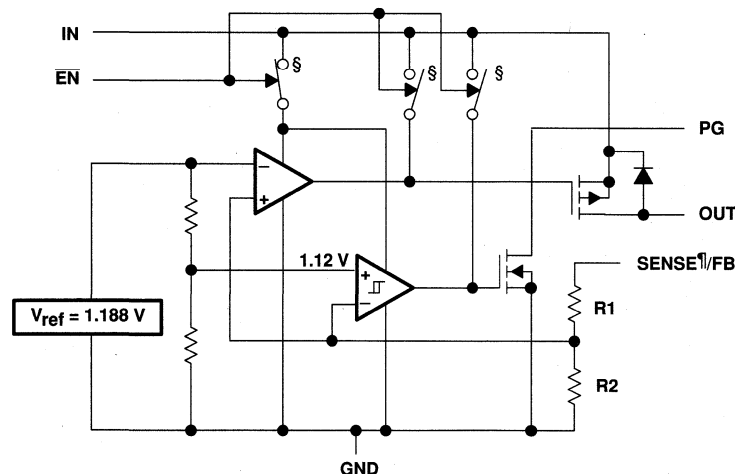
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TPS72xx chip information

These chips, when properly assembled, display characteristics similar to the TPS72xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



functional block diagram



RESISTOR DIVIDER OPTIONS			
DEVICE	R1	R2	UNIT
TPS7201	0	∞	Ω
TPS7225	257	233	kΩ
TPS7228#	306	233	kΩ
TPS7230	357	233	kΩ
TPS7233	420	233	kΩ
TPS7248	726	233	kΩ
TPS7250	756	233	kΩ

NOTE A: Resistors are nominal values only.

COMPONENT COUNT	
MOS transistors	108
Bipolar transistors	41
Diodes	4
Capacitors	15
Resistors	75

§ Switch positions are shown with EN low (active).

¶ For most applications, SENSE should be externally connected to OUT as close as possible to the device.

For other implementations, refer to the SENSE-pin connection discussion in application information section.

This device is in the product preview stage of development. Please contact the local TI sales office for availability.

TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range [‡] , V_I , PG, SENSE, \overline{EN}	-0.3 V to 11 V
Output current, I_O	1.5 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	-55°C to 150°C
Storage temperature range, T_{Stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Note 1 and Figure 3)

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1175 mW	8.74 mW/°C	782 mW	650 mW	301 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Note 1 and Figure 4)

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 85^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
D	2063 mW	16.5 mW/°C	1320 mW	1073 mW	413 mW
P	2738 mW	20.49 mW/°C	1816 mW	1508 mW	689 mW
PW	2900 mW	23.2 mW/°C	1856 mW	1508 mW	580 mW

NOTE 1: Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum of 150°C. For guidelines on maintaining junction temperature within the recommended operating range, see application information section.

MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE

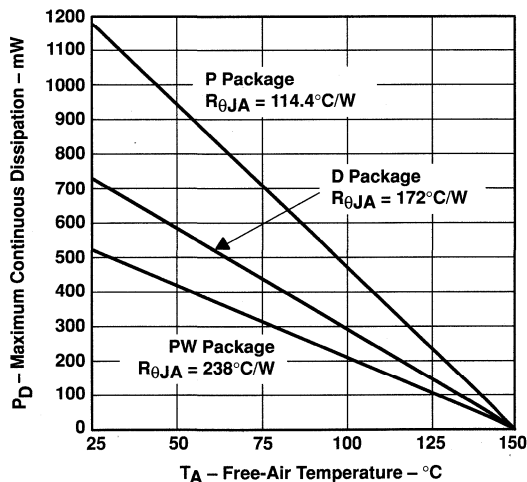


Figure 3

MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE

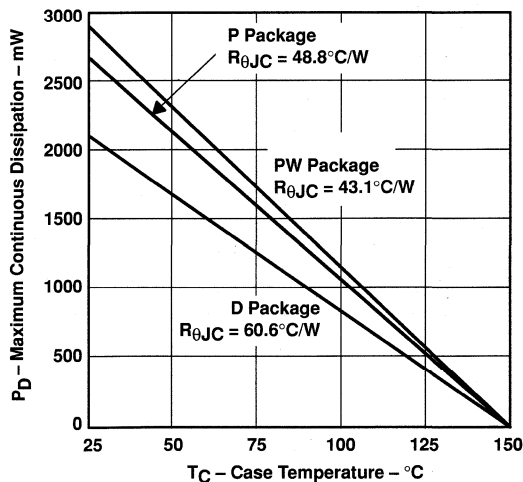


Figure 4

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I †	TPS7201Q	3	10	V
	TPS7225Q	3.65	10	
	TPS7228Q‡	TBD	10	
	TPS7230Q	3.96	10	
	TPS7233Q	3.98	10	
	TPS7248Q	5.24	10	
	TPS7250Q	5.41	10	
High-level input voltage at \overline{EN} , V_{IH}		2		V
Low-level input voltage at \overline{EN} , V_{IL}			0.5	V
Output current, I_O		0	250	mA
Operating virtual junction temperature, T_J		-40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, **the usable range can be extended for lighter loads**. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

Because the TPS7201 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 under the TPS7201 electrical characteristics table. The minimum value of 3 V is the absolute lower limit for the recommended input-voltage range for the TPS7201.

‡ This device is in the product preview stage of development. Please contact the local TI sales office for availability.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	TPS72xxQ			UNIT
			MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5\text{ V}$, $0\text{ mA} \leq I_O \leq 250\text{ mA}$	$V_I = V_O + 1\text{ V}$	25°C	180	225	μA
			-40°C to 125°C		325	
Input current (standby mode)	$\overline{EN} = V_I$	$3\text{ V} \leq V_I \leq 10\text{ V}$	25°C		0.5	μA
			-40°C to 125°C		1	
Output current limit threshold	$V_O = 0\text{ V}$	$V_I = 10\text{ V}$	25°C	0.6	1	A
			-40°C to 125°C		1.5	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$	$3\text{ V} \leq V_I \leq 10\text{ V}$	25°C		0.5	μA
			-40°C to 125°C		1	
PG leakage current	$V_{PG} = 10\text{ V}$	Normal operation	25°C		0.5	μA
			-40°C to 125°C		0.5	
Output voltage temperature coefficient		-40°C to 125°C		31	75	ppm/°C
Thermal shutdown junction temperature				165		°C
\overline{EN} logic high (standby mode)	$3\text{ V} \leq V_I \leq 6\text{ V}$	-40°C to 125°C		2		V
	$6\text{ V} \leq V_I \leq 10\text{ V}$			2.7		
\overline{EN} logic low (active mode)	$3\text{ V} \leq V_I \leq 10\text{ V}$	25°C		0.5	V	
		-40°C to 125°C		0.5		
\overline{EN} hysteresis voltage		25°C		50		mV
\overline{EN} input current	$0\text{ V} \leq V_I \leq 10\text{ V}$	25°C	-0.5	0.5	μA	
		-40°C to 125°C	-0.5	0.5		
Minimum V_I for active pass element		25°C	1.9	2.5	V	
		-40°C to 125°C		2.5		
Minimum V_I for valid PG	$I_{PG} = 300\text{ }\mu\text{A}$	25°C	1.1	1.5	V	
		-40°C to 125°C		1.9		

† CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY**
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TPS7201Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT}^\dagger = 1\text{ }\Omega$), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS7201Q			UNIT
				MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	$V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$		25°C	1.188			V
	$3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2	$5\text{ mA} \leq I_O \leq 250\text{ mA}$	-40°C to 125°C	1.152		1.224	V
Reference voltage temperature coefficient			-40°C to 125°C	31		75	ppm/°C
Pass-element series resistance (see Note 3)	$V_I = 2.4\text{ V}$, §	$50\text{ }\mu\text{A} \leq I_O \leq 100\text{ mA}$	25°C	2.1			Ω
	$V_I = 2.4\text{ V}$, §	$100\text{ mA} \leq I_O \leq 200\text{ mA}$	25°C	2.9			
	$V_I = 2.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	1.6		2.7	
			-40°C to 125°C	4.5			
	$V_I = 3.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	1			
$V_I = 5.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	0.8				
Input regulation	$V_I = 3\text{ V to } 10\text{ V}$, See Note 2	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C			23	mV
			-40°C to 125°C			36	
Output regulation	$I_O = 5\text{ mA to } 250\text{ mA}$, See Note 2	$3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2	25°C	15		25	mV
			-40°C to 125°C			36	
	$I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$, See Note 2	$3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2	25°C	17		27	
			-40°C to 125°C			43	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	49	60	dB	
			-40°C to 125°C	32			
		$I_O = 250\text{ mA}$, See Note 2	25°C	45	50		
			-40°C to 125°C	30			
Output noise spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT}^\dagger = 1\text{ }\Omega$		25°C	235		μV_{rms}	
			25°C	190			
			25°C	125			
PG trip-threshold voltage¶	V_{FB} voltage decreasing from above V_{PG}		-40°C to 125°C	$0.95 \times V_{\text{FB(nom)}}$		V	
PG hysteresis voltage¶	Measured at V_{FB}		25°C	12		mV	
PG output low voltage¶	$I_{\text{PG}} = 400\text{ }\mu\text{A}$, $V_I = 2.13\text{ V}$		25°C	0.1	0.4	V	
			-40°C to 125°C		0.4		
FB input current			25°C	-10	0.1	10	nA
			-40°C to 125°C	-20		20	

† CSRT refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2. When $V_I < 2.9\text{ V}$ and $I_O > 100\text{ mA}$ simultaneously, pass element $r_{\text{DS(on)}}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3. To calculate dropout voltage, use equation:

$$V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$$

$r_{\text{DS(on)}}$ is a function of both output current and input voltage. The parametric table lists $r_{\text{DS(on)}}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TPS7225Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSRT = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T _J	TPS7225Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 3.5\text{ V}$,	$I_O = 10\text{ mA}$	25°C	2.5		2.55	V
	$3.5\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O \leq 250\text{ mA}$	-40°C to 125°C	2.45			
Dropout voltage	$I_O = 250\text{ mA}$,	$V_I = 2.97\text{ V}$	25°C	560	850	1.1	mV
			-40°C to 125°C				
Pass-element series resistance	$(2.97\text{ V} - V_O)/I_O$,	$V_I = 2.97\text{ V}$,	25°C	2.24	3.4	3.84	Ω
			-40°C to 125°C				
Input regulation	$V_I = 3.5\text{ V to }10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	9	27	33	mV
			-40°C to 125°C				
Output regulation	$I_O = 5\text{ mA to }250\text{ mA}$,	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	28	36	60	mV
			-40°C to 125°C				
	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$,	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	24	41	73	
			-40°C to 125°C				
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	47	58	45	dB
			-40°C to 125°C				
		$I_O = 250\text{ mA}$	25°C	40	46	38	
			-40°C to 125°C				
Output noise spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$,	$C_O = 4.7\text{ }\mu\text{F}$	25°C	248		200	μVrms
		$C_O = 10\text{ }\mu\text{F}$	25°C				
		$C_O = 100\text{ }\mu\text{F}$	25°C	130			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	$0.95 \times V_{O(nom)}$		V	
PG hysteresis voltage			25°C	50		mV	
PG output low voltage	$I_{PG} = 1.2\text{ mA}$,	$V_I = 2.13\text{ V}$	25°C	0.3	0.44	0.5	V
			-40°C to 125°C				

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TPS7228Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 3.75\text{ V}$, $\overline{E_N} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT} = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T _J	TPS7228Q			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 3.75\text{ V}$, $I_O = 10\text{ mA}$	25°C		2.75		V
	$3.75\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 250\text{ mA}$	-40°C to 125°C	2.69		2.81	
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 2.69\text{ V}$	25°C		TBD		mV
		-40°C to 125°C			TBD	
	$I_O = 100\text{ mA}$, $V_I = 2.69\text{ V}$	25°C		TBD		
		-40°C to 125°C			TBD	
	$I_O = 250\text{ mA}$, $V_I = 2.69\text{ V}$	25°C		TBD		
		-40°C to 125°C			TBD	
Pass-element series resistance	$(2.69\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$, $V_I = 2.69\text{ V}$	25°C		TBD		Ω
		-40°C to 125°C			TBD	
Input regulation	$V_I = 3.75\text{ V}$ to 10 V , $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C		TBD		mV
		-40°C to 125°C			TBD	
Output regulation	$I_O = 5\text{ mA}$ to 250 mA , $3.75\text{ V} \leq V_I \leq 10\text{ V}$	25°C		TBD		mV
		-40°C to 125°C			TBD	
	$I_O = 50\text{ }\mu\text{A}$ to 250 mA , $3.75\text{ V} \leq V_I \leq 10\text{ V}$	25°C		TBD		
		-40°C to 125°C			TBD	
Ripple rejection	$f = 120\text{ Hz}$, $I_O = 50\text{ }\mu\text{A}$	25°C		TBD		dB
		-40°C to 125°C			TBD	
	$I_O = 250\text{ mA}$	25°C		TBD		
		-40°C to 125°C			TBD	
Output noise spectral density	$f = 120\text{ Hz}$	25°C		TBD		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSRT} = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C		TBD	μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$	25°C		TBD	
		$C_O = 100\text{ }\mu\text{F}$	25°C		TBD	
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}	-40°C to 125°C		TBD		V
PG hysteresis voltage		25°C		TBD		mV
PG output low voltage	$I_{\text{PG}} = 1.2\text{ mA}$, $V_I = 2.34\text{ V}$	25°C			TBD	V
		-40°C to 125°C			TBD	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TPS7230Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 4\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS7230Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4\text{ V}$, $I_O = 10\text{ mA}$		25°C		3		V
	$4\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 250\text{ mA}$		-40°C to 125°C	2.94		3.06	
Dropout voltage	$I_O = 100\text{ mA}$, $V_I = 2.97\text{ V}$		25°C		145	185	mV
			-40°C to 125°C			270	
	$I_O = 250\text{ mA}$, $V_I = 2.97\text{ V}$		25°C		390	502	
			-40°C to 125°C			900	
Pass-element series resistance	$(2.97\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$	$V_I = 2.97\text{ V}$	25°C		1.56	2.01	Ω
			-40°C to 125°C			3.6	
Input regulation	$V_I = 4\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		25°C		9	27	mV
			-40°C to 125°C			33	
Output regulation	$I_O = 5\text{ mA to } 250\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$		25°C		34	45	mV
			-40°C to 125°C			74	
	$I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$		25°C		42	60	
			-40°C to 125°C			98	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	45	56	dB	
			-40°C to 125°C	44			
		$I_O = 250\text{ mA}$	25°C	40	45		
			-40°C to 125°C	38			
Output noise spectral density	$f = 120\text{ Hz}$		25°C		2	$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C		256	μV_{rms}	
		$C_O = 10\text{ }\mu\text{F}$	25°C		206		
		$C_O = 100\text{ }\mu\text{F}$	25°C		132		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C		$0.95 \times V_{O(\text{nom})}$	V	
PG hysteresis voltage			25°C		50	mV	
PG output low voltage	$I_{\text{PG}} = 1.2\text{ mA}$, $V_I = 2.55\text{ V}$		25°C		0.25	0.44	V
			-40°C to 125°C			0.44	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
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TPS7233Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	TPS7233Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$,	$I_O = 10\text{ mA}$	25°C	3.3			V
	$4.3\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O \leq 250\text{ mA}$	-40°C to 125°C	3.23	3.37		
Dropout voltage	$I_O = 10\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	14	20		mV
			-40°C to 125°C	30			
	$I_O = 100\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	140			
			-40°C to 125°C	232			
	$I_O = 250\text{ mA}$,	$V_I = 3.23\text{ V}$	25°C	360			
			-40°C to 125°C	610			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$	$V_I = 3.23\text{ V}$,	25°C	1.5	1.84		Ω
			-40°C to 125°C	2.5			
Input regulation	$V_I = 4.3\text{ V to }10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	8			mV
			-40°C to 125°C	33			
Output regulation	$I_O = 5\text{ mA to }250\text{ mA}$,	$4.3\text{ V} \leq V_I \leq 10\text{ V}$	25°C	32	42		mV
			-40°C to 125°C	71			
	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$,	$4.3\text{ V} \leq V_I \leq 10\text{ V}$	25°C	41			
			-40°C to 125°C	98			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	40	52		dB
			-40°C to 125°C	38			
		$I_O = 250\text{ mA}$	25°C	35	44		
			-40°C to 125°C	33			
Output noise spectral density	$f = 120\text{ Hz}$		25°C	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	265			μVrms
		$C_O = 10\text{ }\mu\text{F}$	25°C	212			
		$C_O = 100\text{ }\mu\text{F}$	25°C	135			
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C	$0.95 \times V_{O(\text{nom})}$			V
PG hysteresis voltage			25°C	32			mV
PG output low voltage	$I_{PG} = 1.2\text{ mA}$,	$V_I = 2.8\text{ V}$	25°C	0.22	0.4		V
			-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
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TPS7248Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 5.85\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS [‡]		T _J	TPS7248Q			UNIT
				MIN	TYP	MAX	
Output voltage	$V_I = 5.85\text{ V}$,	$I_O = 10\text{ mA}$	25°C		4.85		V
	$5.85\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O < 250\text{ mA}$	-40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10\text{ mA}$,	$V_I = 4.75\text{ V}$	25°C		10	19	mV
			-40°C to 125°C			30	
	$I_O = 100\text{ mA}$,	$V_I = 4.75\text{ V}$	25°C		90	100	
			-40°C to 125°C			150	
	$I_O = 250\text{ mA}$,	$V_I = 4.75\text{ V}$	25°C		216	250	
			-40°C to 125°C			285	
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$,	$V_I = 4.75\text{ V}$,	25°C		0.8	1	Ω
			$I_O = 250\text{ mA}$	-40°C to 125°C			
Input regulation	$V_I = 5.85\text{ V}$ to 10 V,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C			34	mV
			-40°C to 125°C				
Output regulation	$I_O = 5\text{ mA}$ to 250 mA,	$5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C		43	55	mV
			-40°C to 125°C				
	$I_O = 50\text{ }\mu\text{A}$ to 250 mA,	$5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C		55	75	
			-40°C to 125°C				
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	42	53	dB	
			-40°C to 125°C	36			
		$I_O = 250\text{ mA}$	25°C	36	46		
			-40°C to 125°C	34			
Output noise spectral density	$f = 120\text{ Hz}$		25°C		2	$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$,	$\text{CSRT}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C		370	μVrms
			$C_O = 10\text{ }\mu\text{F}$	25°C		290	
			$C_O = 100\text{ }\mu\text{F}$	25°C		168	
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		-40°C to 125°C		$0.95 \times V_{O(\text{nom})}$	V	
PG hysteresis voltage			25°C		50	mV	
PG output low voltage	$I_{PG} = 1.2\text{ mA}$,	$V_I = 4.12\text{ V}$	25°C		0.2	0.4	V
			-40°C to 125°C				

[†] CSRT refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
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TPS7250Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	TPS7250Q			UNIT	
			MIN	TYP	MAX		
Output voltage	$V_I = 6\text{ V}$, $I_O = 10\text{ mA}$	25°C	5			V	
	$6\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 250\text{ mA}$	-40°C to 125°C	4.9	5.1			
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	8		12	mV	
		-40°C to 125°C	30				
	$I_O = 100\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	76		85		
		-40°C to 125°C	136				
	$I_O = 250\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	190		206		
		-40°C to 125°C	312				
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$, $V_I = 4.88\text{ V}$	25°C	0.76	0.825		Ω	
		-40°C to 125°C	1.25				
Input regulation	$V_I = 6\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	25°C	28			mV	
		-40°C to 125°C	35				
Output regulation	$I_O = 5\text{ mA to }250\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	46		61	mV	
		-40°C to 125°C	100				
	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	59		79		
		-40°C to 125°C	150				
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	41	52	dB	
			-40°C to 125°C	37			
		$I_O = 250\text{ mA}$	25°C	36	46		
			-40°C to 125°C	32			
Output noise spectral density	$f = 120\text{ Hz}$	25°C	2			$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSR^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	25°C		390	μVrms	
		$C_O = 10\text{ }\mu\text{F}$	25°C		300		
		$C_O = 100\text{ }\mu\text{F}$	25°C		175		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}	-40°C to 125°C	$0.95 \times V_{O(nom)}$			V	
PG hysteresis voltage		25°C	50			mV	
PG output low voltage	$I_{PG} = 1.2\text{ mA}$, $V_I = 4.25\text{ V}$	25°C	0.19		0.4	V	
		-40°C to 125°C	0.4				

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
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electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS72xxY			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN} \leq 0.5\text{ V}$, $0\text{ mA} \leq I_O \leq 250\text{ mA}$		180		μA
Output current limit threshold	$V_O = 0\text{ V}$, $V_I = 10\text{ V}$		0.6		A
Thermal shutdown junction temperature			165		$^\circ\text{C}$
\overline{EN} hysteresis voltage			50		mV
Minimum V_I for active pass element			1.9		V
Minimum V_I for valid PG	$I_{PG} = 300\text{ }\mu\text{A}$		1.1		V

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7201Y			UNIT
		MIN	TYP	MAX	
Reference voltage (measured at FB with OUT connected to FB)	$V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$		1.188		V
Pass-element series resistance (see Note 3)	$V_I = 2.4\text{ V}$, § $50\text{ }\mu\text{A} \leq I_O \leq 100\text{ mA}$		2.1		Ω
	$V_I = 2.4\text{ V}$, § $100\text{ mA} \leq I_O \leq 200\text{ mA}$		2.9		
	$V_I = 2.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		1.6		
	$V_I = 3.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		1		
	$V_I = 5.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		0.8		
Output regulation	$3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2 $I_O = 5\text{ mA}$ to 250 mA ,		15		mV
	$3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2 $I_O = 50\text{ }\mu\text{A}$ to 250 mA ,		17		
Ripple rejection	$V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	60		dB
		$I_O = 250\text{ mA}$, See Note 2	50		
Output noise spectral density	$V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 3.5\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSR^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	235		μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$	190		
		$C_O = 100\text{ }\mu\text{F}$	125		
PG hysteresis voltage¶	$V_I = 3.5\text{ V}$, Measured at V_{FB}		12		mV
PG output low voltage¶	$V_I = 2.13\text{ V}$, $I_{PG} = 400\text{ }\mu\text{A}$		0.1		V
FB input current	$V_I = 3.5\text{ V}$		0.1		nA

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‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2 When $V_I < 2.9\text{ V}$ and $I_O > 100\text{ mA}$ simultaneously, pass element $r_{\text{DS(on)}}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3 To calculate dropout voltage, use equation:

$$V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$$

$r_{\text{DS(on)}}$ is a function of both output current and input voltage. The parametric table lists $r_{\text{DS(on)}}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
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electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7225Y			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 3.5\text{ V}$,	$I_O = 10\text{ mA}$	2.5			V
Dropout voltage	$V_I = 2.97\text{ V}$,	$I_O = 250\text{ mA}$	560			mV
Pass-element series resistance	$(2.97\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$		$V_I = 2.97\text{ V}$, 2.24			Ω
Input regulation	$V_I = 3.5\text{ V to }10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	9			mV
Output regulation	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	$I_O = 5\text{ mA to }250\text{ mA}$	28			mV
	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$	24			
Ripple rejection	$V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	58			dB
		$I_O = 250\text{ mA}$	46			
Output noise spectral density	$V_I = 3.5\text{ V}$,	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 3.5\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	248			μVrms
		$C_O = 10\text{ }\mu\text{F}$	200			
		$C_O = 100\text{ }\mu\text{F}$	130			
PG hysteresis voltage	$V_I = 3.5\text{ V}$		50			mV
PG output low voltage	$V_I = 2.13\text{ V}$	$I_{PG} = 1.2\text{ mA}$	0.3			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
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electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSRT = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†	TPS7228Y			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 3.75\text{ V}$, $I_O = 10\text{ mA}$		2.75		V
Dropout voltage	$V_I = 2.97\text{ V}$, $I_O = 10\text{ mA}$		TBD		mV
	$V_I = 2.97\text{ V}$, $I_O = 100\text{ mA}$		TBD		
	$V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$		TBD		
Pass-element series resistance	$(2.97\text{ V} - V_O)/I_O$, $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$		TBD		Ω
Input regulation	$V_I = 3.75\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		TBD		mV
Output regulation	$3.75\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to }250\text{ mA}$		TBD		mV
	$3.75\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to }250\text{ mA}$		TBD		
Ripple rejection	$V_I = 3.75\text{ V}$, $f = 120\text{ Hz}$, $I_O = 50\text{ }\mu\text{A}$		TBD		dB
	$I_O = 250\text{ mA}$		TBD		
Output noise spectral density	$V_I = 3.75\text{ V}$, $f = 120\text{ Hz}$		TBD		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 3.75\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSRT = 1\text{ }\Omega$, $C_O = 4.7\text{ }\mu\text{F}$		TBD		μVrms
	$C_O = 10\text{ }\mu\text{F}$		TBD		
	$C_O = 100\text{ }\mu\text{F}$		TBD		
PG hysteresis voltage	$V_I = 3.75\text{ V}$		TBD		mV
PG output low voltage	$V_I = 2.34\text{ V}$, $I_{PG} = 1.2\text{ mA}$		TBD		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS†	TPS7230Y			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 4\text{ V}$, $I_O = 10\text{ mA}$		3		V
Dropout voltage	$V_I = 2.97\text{ V}$, $I_O = 100\text{ mA}$		145		mV
	$V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$		390		
Pass-element series resistance	$(2.97\text{ V} - V_O)/I_O$, $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$		1.56		Ω
Input regulation	$V_I = 4\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$		9		mV
Output regulation	$4\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to }250\text{ mA}$		34		mV
	$4\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to }250\text{ mA}$		41		
Ripple rejection	$V_I = 4\text{ V}$, $f = 120\text{ Hz}$, $I_O = 50\text{ }\mu\text{A}$		56		dB
	$I_O = 250\text{ mA}$		45		
Output noise spectral density	$V_I = 4\text{ V}$, $f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 4\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSRT = 1\text{ }\Omega$, $C_O = 4.7\text{ }\mu\text{F}$		256		μVrms
	$C_O = 10\text{ }\mu\text{F}$		206		
	$C_O = 100\text{ }\mu\text{F}$		132		
PG hysteresis voltage	$V_I = 4\text{ V}$		50		mV
PG output low voltage	$V_I = 2.55\text{ V}$, $I_{PG} = 1.2\text{ mA}$		0.25		V

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electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7233Y			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 4.3\text{ V}$,	$I_O = 10\text{ mA}$	3.3			V
Dropout voltage	$V_I = 3.23\text{ V}$,	$I_O = 10\text{ mA}$	14			mV
	$V_I = 3.23\text{ V}$,	$I_O = 100\text{ mA}$	140			
	$V_I = 3.23\text{ V}$,	$I_O = 250\text{ mA}$	360			
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$	$V_I = 3.23\text{ V}$,	1.5			Ω
Input regulation	$V_I = 4.3\text{ V to }10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$	8			mV
Output regulation	$4.3\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 5\text{ mA to }250\text{ mA}$	32			mV
	$4.3\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$	41			
Ripple rejection	$V_I = 4.3\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	52			dB
		$I_O = 250\text{ mA}$	44			
Output noise spectral density	$V_I = 4.3\text{ V}$,	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 4.3\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	265			μVrms
		$C_O = 10\text{ }\mu\text{F}$	212			
		$C_O = 100\text{ }\mu\text{F}$	135			
PG hysteresis voltage	$V_I = 4.3\text{ V}$		32			mV
PG output low voltage	$V_I = 2.8\text{ V}$,	$I_{PG} = 1.2\text{ mA}$	0.22			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER	TEST CONDITIONS‡		TPS7248Y			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 5.85\text{ V}$,	$I_O = 10\text{ mA}$	4.85			V
Dropout voltage	$V_I = 4.75\text{ V}$,	$I_O = 10\text{ mA}$	10			mV
	$V_I = 4.75\text{ V}$,	$I_O = 100\text{ mA}$	90			
	$V_I = 4.75\text{ V}$,	$I_O = 250\text{ mA}$	216			
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$	$V_I = 4.75\text{ V}$,	0.8			Ω
Output regulation	$5.85\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 5\text{ mA to }250\text{ mA}$	43			mV
	$5.85\text{ V} \leq V_I \leq 10\text{ V}$,	$I_O = 50\text{ }\mu\text{A to }250\text{ mA}$	55			
Ripple rejection	$V_I = 5.85\text{ V}$, $f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	53			dB
		$I_O = 250\text{ mA}$	46			
Output noise spectral density	$V_I = 5.85\text{ V}$,	$f = 120\text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 5.85\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$	$C_O = 4.7\text{ }\mu\text{F}$	370			μVrms
		$C_O = 10\text{ }\mu\text{F}$	290			
		$C_O = 100\text{ }\mu\text{F}$	168			
PG hysteresis voltage	$V_I = 5.85\text{ V}$		50			mV
PG output low voltage	$V_I = 4.12\text{ V}$	$I_{PG} = 1.2\text{ mA}$	0.2			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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electrical characteristics, $I_O = 10 \text{ mA}$, $\overline{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ ($\text{CSR}^\dagger = 1 \Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS‡		TPS7250Y			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 6 \text{ V}$,	$I_O = 10 \text{ mA}$	5			V
Dropout voltage	$V_I = 4.88 \text{ V}$	$I_O = 10 \text{ mA}$	8			mV
	$V_I = 4.88 \text{ V}$	$I_O = 100 \text{ mA}$	76			
	$V_I = 4.88 \text{ V}$,	$I_O = 250 \text{ mA}$	190			
Pass-element series resistance	$(4.88 \text{ V} - V_O)/I_O$, $I_O = 250 \text{ mA}$	$V_I = 4.88 \text{ V}$,	0.76			Ω
Input regulation	$V_I = 6 \text{ V to } 10 \text{ V}$,	$50 \mu\text{A} \leq I_O \leq 250 \text{ mA}$				mV
Output regulation	$6 \text{ V} \leq V_I \leq 10 \text{ V}$,	$I_O = 5 \text{ mA to } 250 \text{ mA}$	46			mV
	$6 \text{ V} \leq V_I \leq 10 \text{ V}$,	$I_O = 50 \mu\text{A to } 250 \text{ mA}$	59			
Ripple rejection	$V_I = 6 \text{ V}$, $f = 120 \text{ Hz}$	$I_O = 50 \mu\text{A}$	52			dB
		$I_O = 250 \text{ mA}$	46			
Output noise spectral density	$V_I = 6 \text{ V}$,	$f = 120 \text{ Hz}$	2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$V_I = 6 \text{ V}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$, $\text{CSR}^\dagger = 1 \Omega$	$C_O = 4.7 \mu\text{F}$	390			μVrms
		$C_O = 10 \mu\text{F}$	300			
		$C_O = 100 \mu\text{F}$	175			
PG hysteresis voltage	$V_I = 6 \text{ V}$		50			mV
PG output low voltage	$V_I = 4.25 \text{ V}$,	$I_{PG} = 1.2 \text{ mA}$	0.19			V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	5
		vs Input voltage	6
ΔI_Q^\dagger	Change in quiescent current	vs Free-air temperature	7
V_{DO}	Dropout voltage	vs Output current	8
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	9
V_{DO}	Dropout voltage (TPS7201 only)	vs Output current	10
$r_{DS(on)}$	Pass-element series resistance	vs Input voltage	11
ΔV_O	Change in output voltage	vs Free-air temperature	12
V_O	Output voltage	vs Input voltage	13
		Line regulation	vs Input voltage
	Load regulation (TPS7225, TPS7233, TPS7248, TPS7250)	vs Input voltage	15
$V_O(PG)$	Power-good (PG) voltage	vs Output voltage	16
$r_{DS(on)PG}$	Power-good (PG) on-resistance	vs Input voltage	17
V_I	Minimum input voltage for valid PG	vs Free-air temperature	18
		Output voltage response from enable (EN)	vs Time
	Load transient response (TPS7201/TPS7233)	vs Time	20
	Load transient response (TPS7248/TPS7250)	vs Time	21
	Line transient response (TPS7201)	vs Time	22
	Line transient response (TPS7233)	vs Time	23
	Line transient response (TPS7248/TPS7250)	vs Time	24
	Ripple rejection	vs Frequency	25
	Output Spectral Noise Density	vs Frequency	26
	Compensation series resistance (CSR)	vs Output current ($C_O = 4.7 \mu F$)	27
		vs Added ceramic capacitance ($C_O = 4.7 \mu F$)	28
		vs Output current ($C_O = 10 \mu F$)	29
		vs Added ceramic capacitance ($C_O = 10 \mu F$)	30

† This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
 vs
 OUTPUT CURRENT

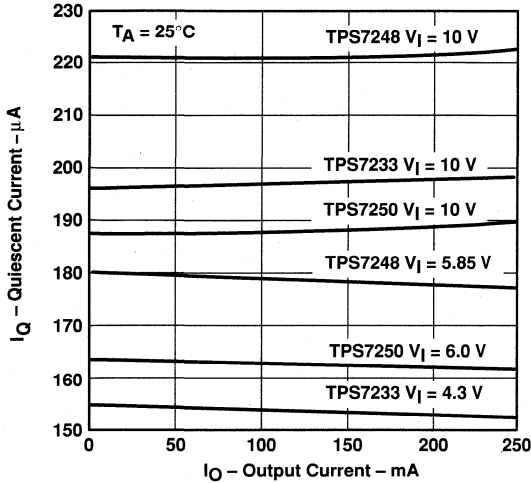


Figure 5

QUIESCENT CURRENT
 vs
 INPUT VOLTAGE

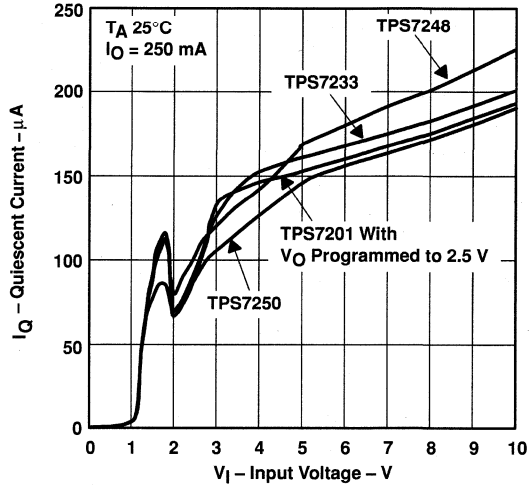


Figure 6

CHANGE IN QUIESCENT CURRENT
 vs
 FREE-AIR TEMPERATURE

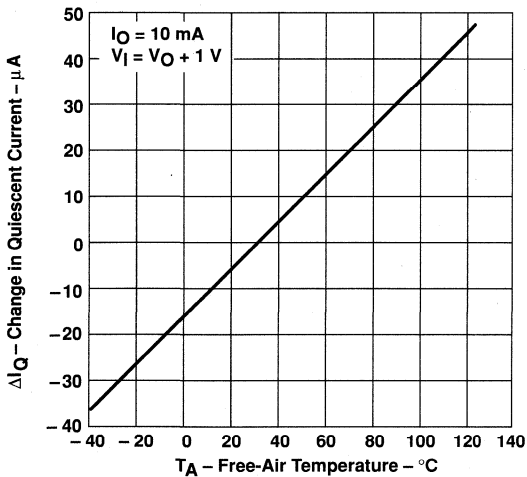


Figure 7

DROPOUT VOLTAGE
 vs
 OUTPUT CURRENT

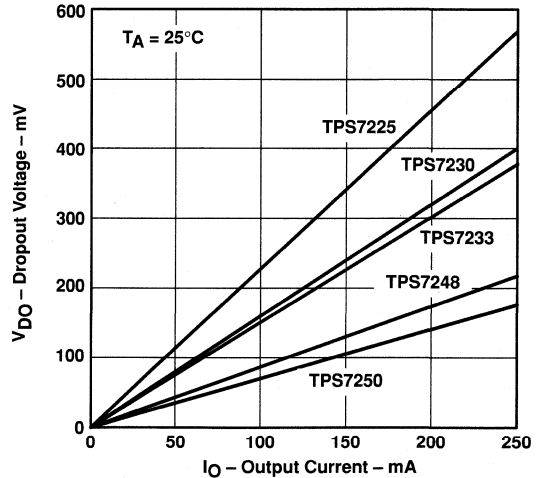


Figure 8

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY**
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

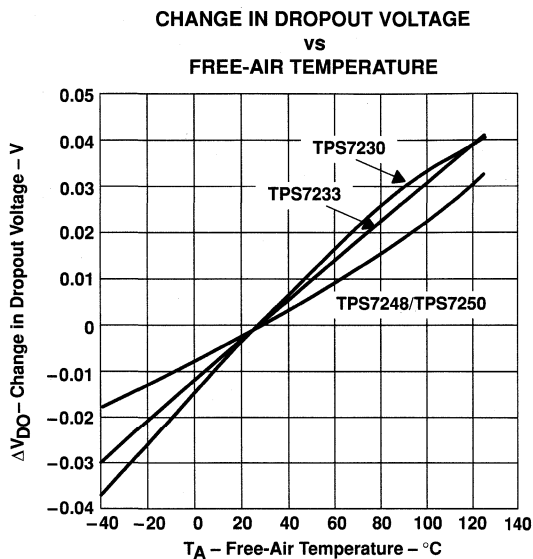
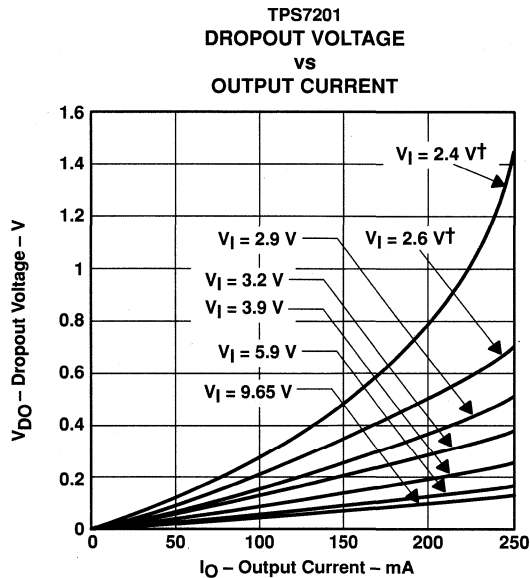


Figure 9



† This voltage is not recommended.

Figure 10

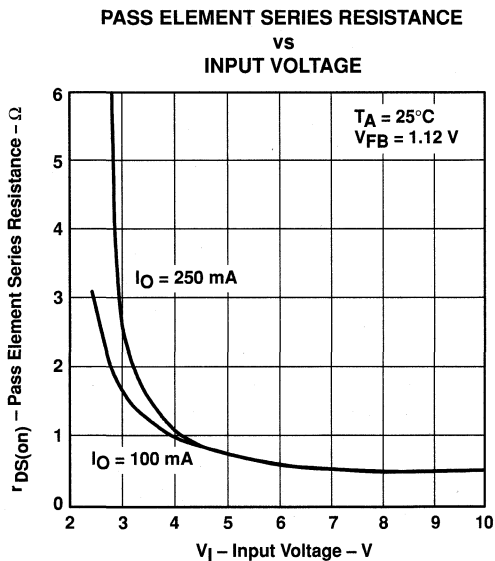


Figure 11

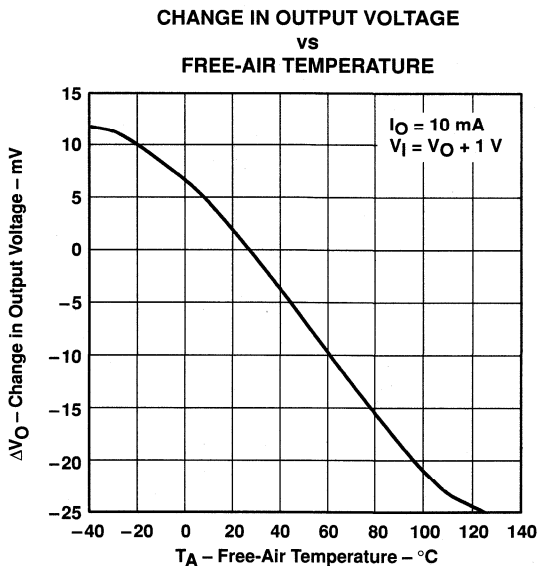


Figure 12

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE**

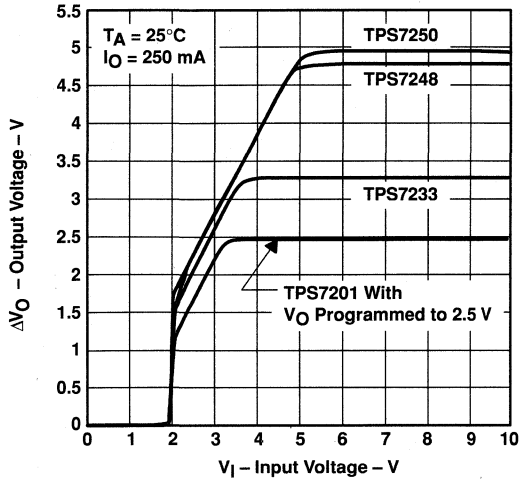


Figure 13

LINE REGULATION

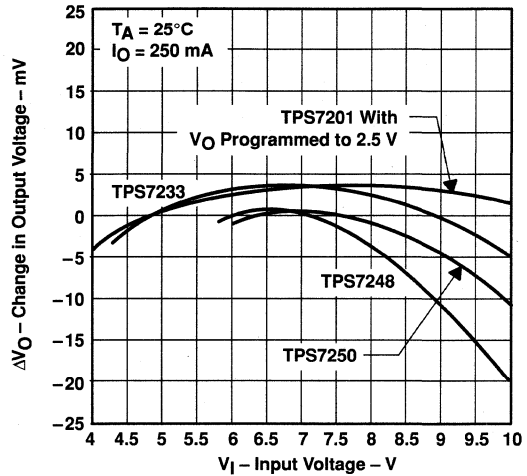


Figure 14

LOAD REGULATION

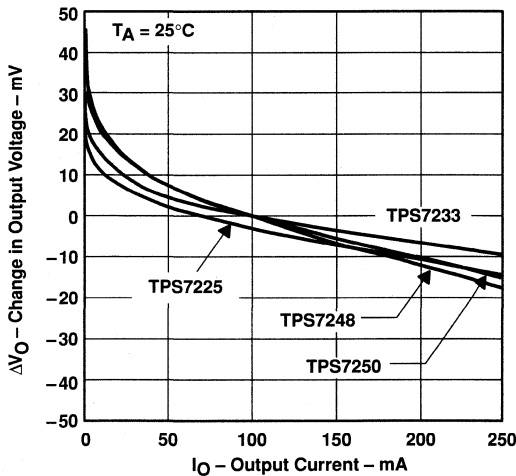
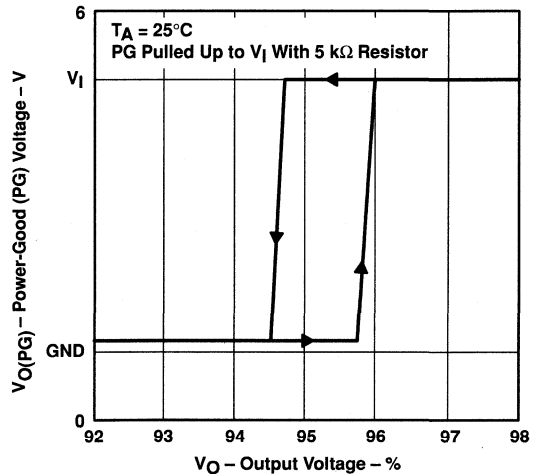


Figure 15

**POWER-GOOD (PG) VOLTAGE
 vs
 OUTPUT VOLTAGE†**



† V_O as a percent of V_Onom.

Figure 16



TYPICAL CHARACTERISTICS

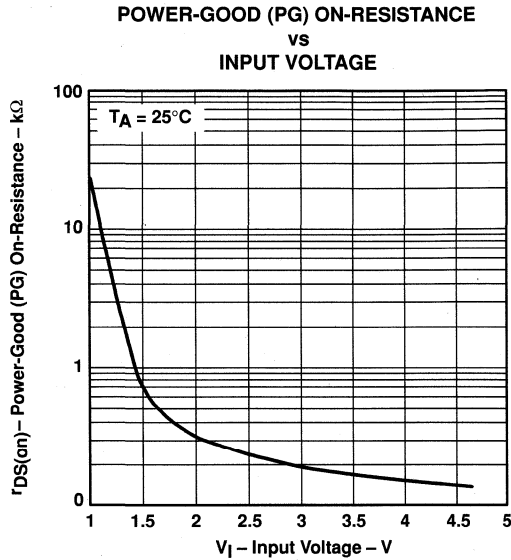


Figure 17

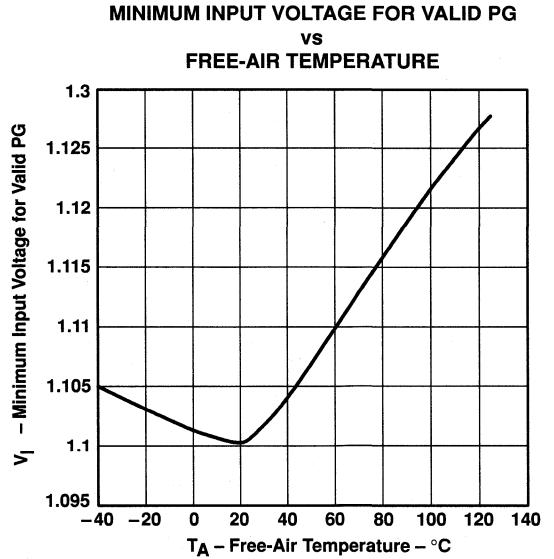


Figure 18

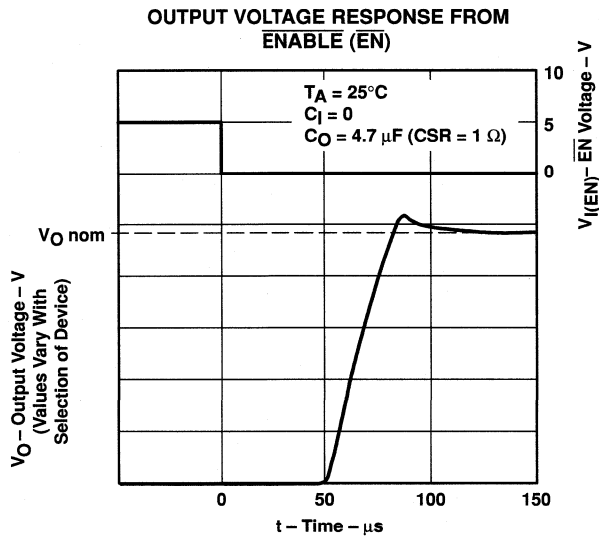


Figure 19

TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TPS7201 (WITH V_O PROGRAMMED TO 2.5 V), TPS7233
LOAD TRANSIENT RESPONSE

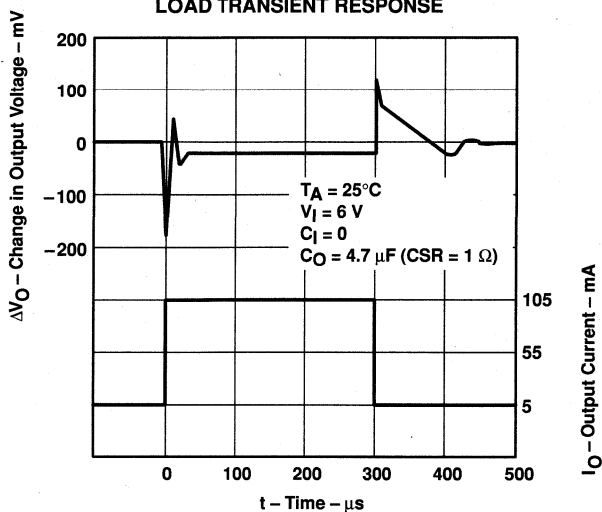


Figure 20

TPS7248/TPS7250
LOAD TRANSIENT RESPONSE

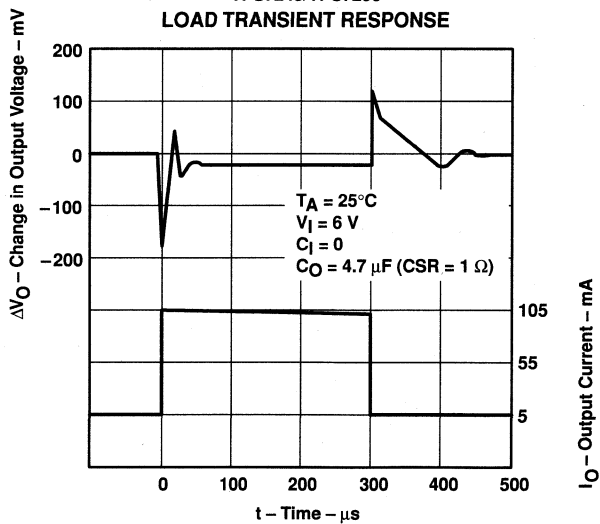


Figure 21

TYPICAL CHARACTERISTICS

TPS7201 WITH V_O PROGRAMMED TO 2.5 V
 LINE TRANSIENT RESPONSE

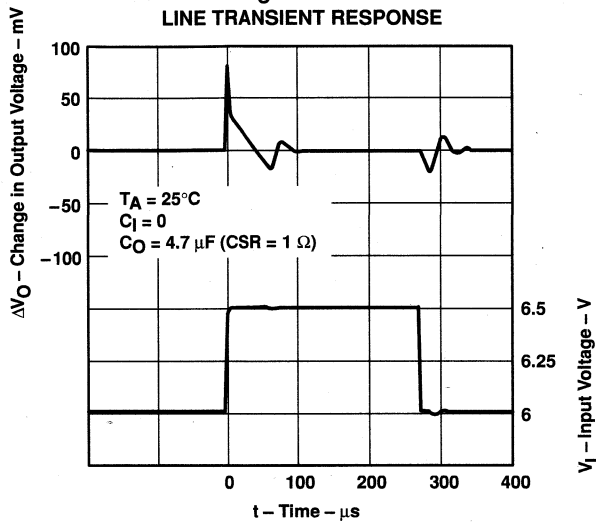


Figure 22

TPS7233
 LINE TRANSIENT RESPONSE

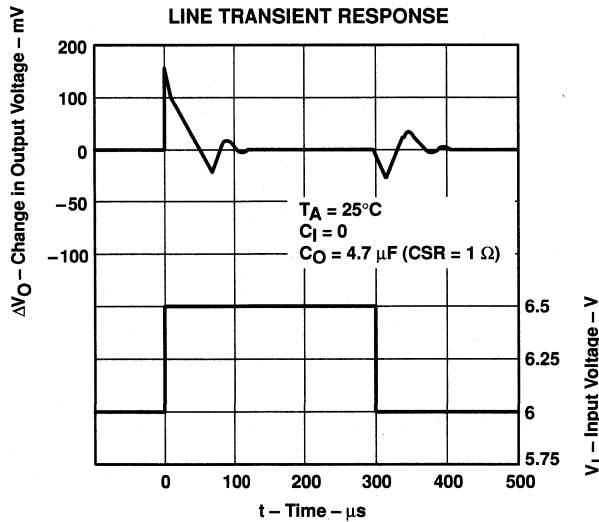


Figure 23

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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TYPICAL CHARACTERISTICS

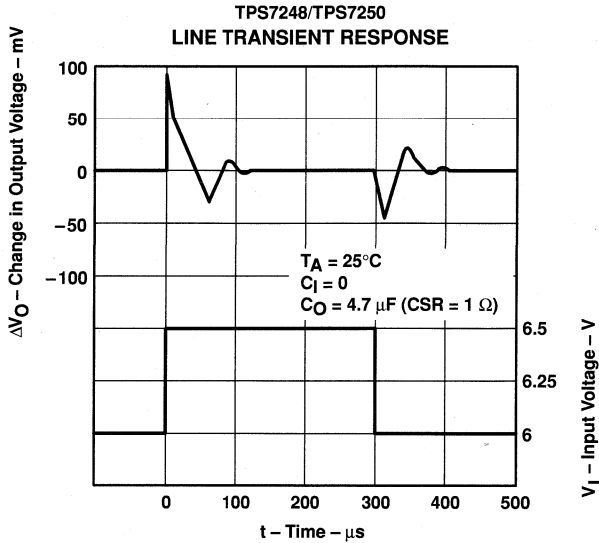


Figure 24

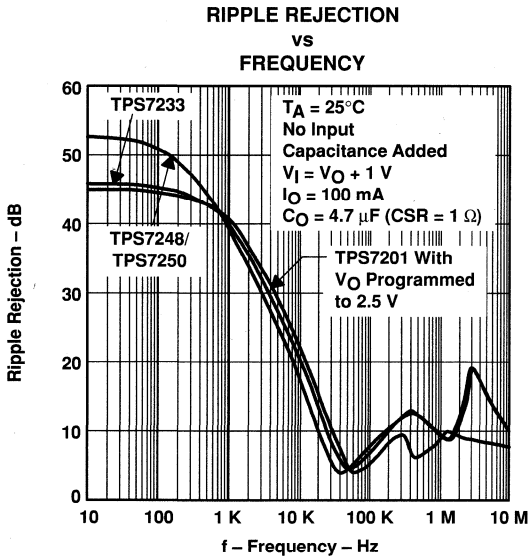


Figure 25

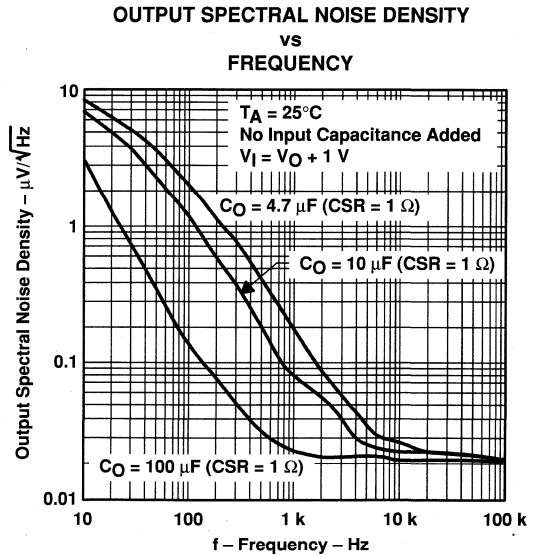


Figure 26



TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

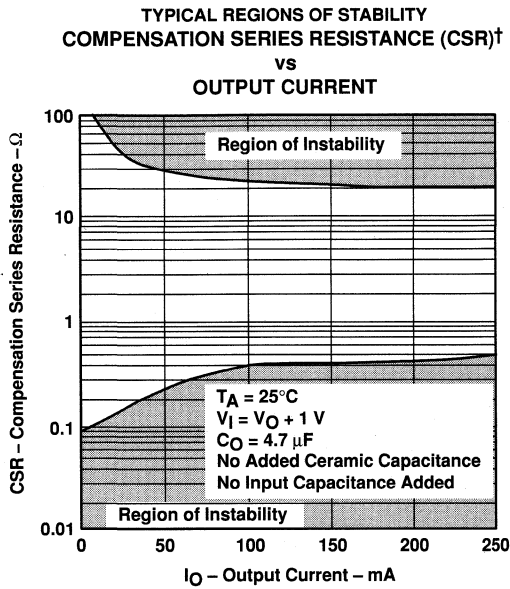


Figure 27

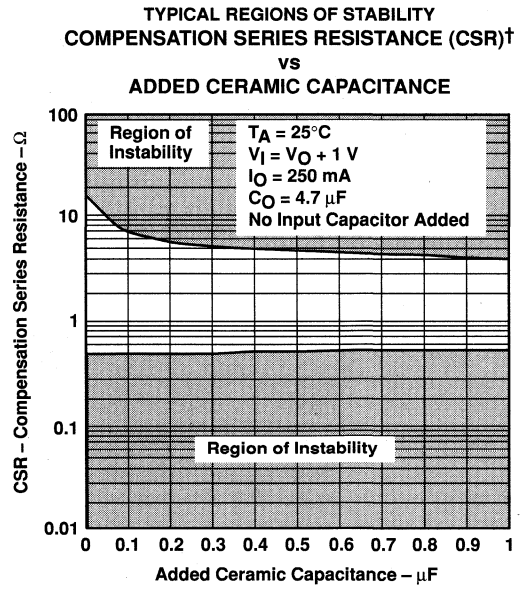


Figure 28

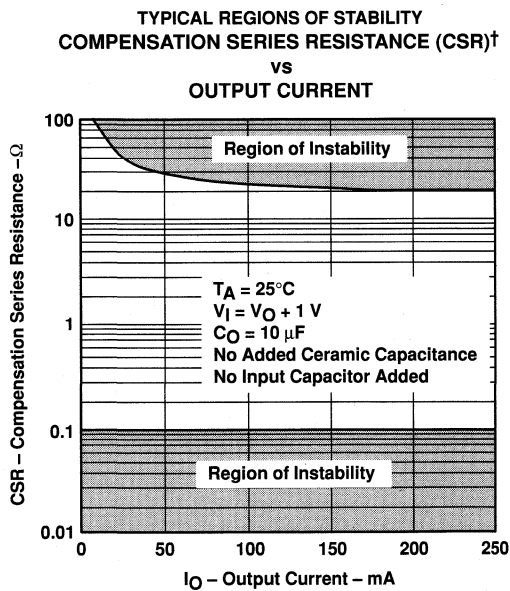


Figure 29

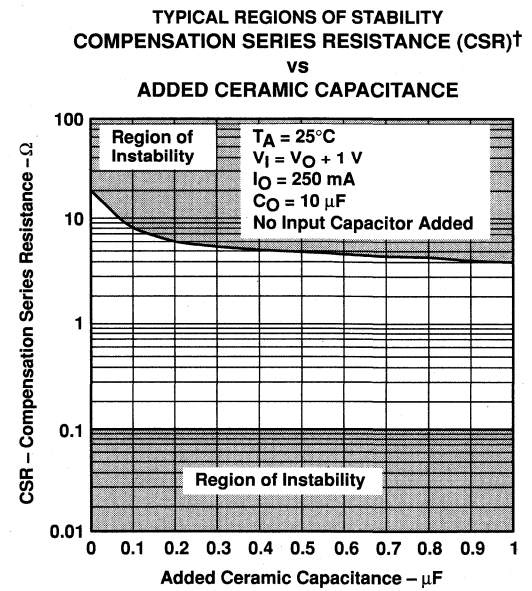


Figure 30

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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APPLICATION INFORMATION

The design of the TPS72xx family of low-dropout (LDO) regulators is based on the higher-current TPS71xx family. These new families of regulators have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low supply currents that remain constant over the full-output-current range of the device, and an enable input to reduce supply currents to less than 0.5 μA when the regulator is turned off.

device operation

The TPS72xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS transistor is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS72xx is essentially constant from no-load to maximum.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load increases reduce the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 5°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

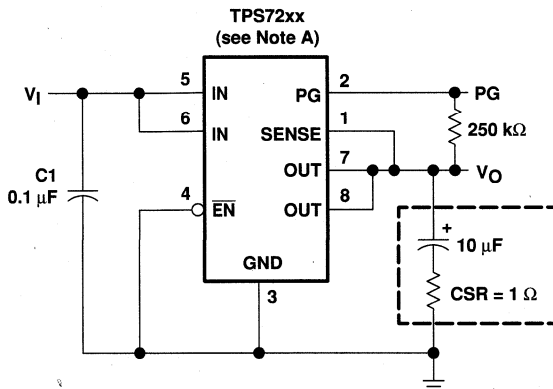
A logic high on the enable input, $\overline{\text{EN}}$, shuts off the output and reduces the supply current to less than 0.5 μA . $\overline{\text{EN}}$ should be grounded in applications where the shutdown feature is not used.

Power good (PG) is an open-drain output signal used to indicate output-voltage status. A comparator circuit continuously monitors the output voltage. When the output drops to approximately 95% of its nominal regulated value, the comparator turns on and pulls PG low.

Transient loads or line pulses can also cause activation of PG if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μs can cause a signal on PG if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1- μs transient causes a PG signal when using an output capacitor with greater than 3.5 Ω of ESR. It is interesting to note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1- μs transient must drop at least 500 mV below the threshold before tripping the PG circuit. A 2- μs transient trips PG at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

A typical application circuit is shown in Figure 31.

APPLICATION INFORMATION



NOTE A. TPS7225, TPS7228†, TPS7230, TPS7233, TPS7248, TPS7250 (fixed-voltage options).

† This device is in the product preview stage of development. Please contact the local TI sales office for availability.

Figure 31. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047- μ F to 0.1- μ F ceramic bypass input capacitor, connected between IN and GND and located close to the TPS72xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

An output capacitor is required to stabilize the internal feedback loop. For most applications, a 10- μ F to 15- μ F solid-tantalum capacitor with a 0.5- Ω resistor (see capacitor selection table) in series is sufficient. The maximum capacitor ESR should be limited to 1.3 Ω to allow for ESR doubling at cold temperatures. Figure 32 shows the transient response of a 5-mA to 85-mA load using a 10- μ F output capacitor with a total ESR of 1.7 Ω .

A 4.7- μ F solid-tantalum capacitor in series with a 1- Ω resistor may also be used (see Figures 27 and 28) provided the ESR of the capacitor does not exceed 1 Ω at room temperature and 2 Ω over the full operating temperature range.

**TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

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APPLICATION INFORMATION

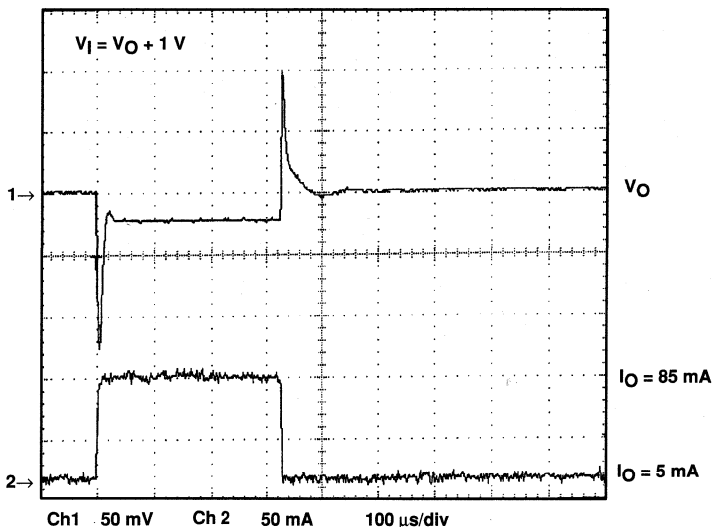


Figure 32. Load Transient Response (CSR total = 1.7 Ω), TPS7248Q

A partial listing of surface-mount capacitors usable with the TPS72xx family is provided below. This information (along with the stability graphs, Figures 27 through 30) is included to assist the designer in selecting suitable capacitors.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.

sense-pin connection

SENSE must be connected to OUT for proper operation of the regulator. Normally this connection should be as short as possible; however, remote sense may be implemented in critical applications when proper care of the circuit path is exercised. SENSE internally connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and any noise pickup on the PCB trace will feed through to the regulator output. SENSE must be routed to minimize noise pickup. Filtering SENSE using an RC network is not recommended because of the possibility of inducing regulator instability.

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS7201 adjustable regulator is programmed using an external resistor divider as shown in Figure 33. The output voltage is calculated using:

$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

$$V_{ref} = 1.188 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 k Ω to set the divider current at 7 μ A and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$

**OUTPUT VOLTAGE
PROGRAMMING GUIDE**

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (k Ω) [†]	
	R1	R2
2.5	191	169
3.3	309	169
3.6	348	169
4	402	169
5	549	169
6.4	750	169

[†] 1% values shown.

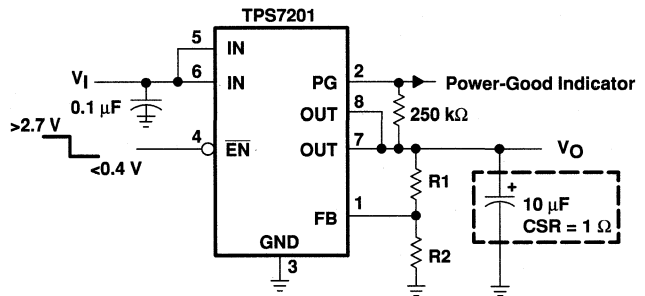


Figure 33. TPS7201 Adjustable LDO Regulator Programming

TPS7201Q, TPS7225Q, TPS7228Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

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APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. These restrictions limit the power dissipation that the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature, i.e., 150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.

regulator protection

The TPS72xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

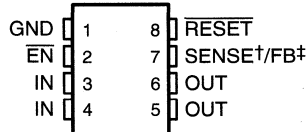
The TPS72xx also features internal current limiting and thermal protection. During normal operation, the TPS72xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

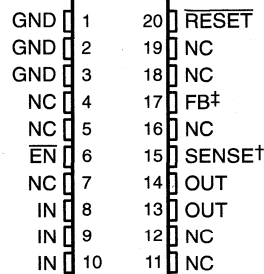
SLVS124F – JUNE 1995 – REVISED JANUARY 1999

- Available in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V Fixed-Output and Adjustable Versions
- Integrated Precision Supply-Voltage Supervisor Monitoring Regulator Output Voltage
- Active-Low Reset Signal with 200-ms Pulse Width
- Very Low Dropout Voltage . . . Maximum of 35 mV at $I_O = 100$ mA (TPS7350)
- Low Quiescent Current – Independent of Load . . . 340 μ A Typ
- Extremely Low Sleep-State Current, 0.5 μ A Max
- 2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions[§]
- Output Current Range of 0 mA to 500 mA
- TSSOP Package Option Offers Reduced Component Height For Critical Applications

**D OR P PACKAGE
(TOP VIEW)**



**PW PACKAGE
(TOP VIEW)**



NC – No internal connection

† SENSE – Fixed voltage options only (TPS7325, TPS7330, TPS7333, TPS7348, and TPS7350)

‡ FB – Adjustable version only (TPS7301)

description

The TPS73xx devices are members of a family of micropower low-dropout (LDO) voltage regulators.

They are differentiated from the TPS71xx and TPS72xx LDOs by their integrated delayed microprocessor-reset function. If the precision delayed reset is not required, the TPS71xx and TPS72xx should be considered.[¶]

AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)			NEGATIVE-GOING RESET THRESHOLD VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
-40°C to 125°C	4.9	5	5.1	4.55	4.65	4.75	TPS7350QD	TPS7350QP	TPS7350QPW	TPS7350Y
	4.75	4.85	4.95	4.5	4.6	4.7	TPS7348QD	TPS7348QP	TPS7348QPW	TPS7348Y
	3.23	3.3	3.37	2.868	2.934	3	TPS7333QD	TPS7333QP	TPS7333QPW	TPS7333Y
	2.94	3	3.06	2.58	2.64	2.7	TPS7330QD	TPS7330QP	TPS7330QPW	TPS7330Y
	2.425	2.5	2.575	2.23	2.32	2.39	TPS7325QD	TPS7325QP	TPS7325QPW	TPS7325Y
	Adjustable 1.2 V to 9.75 V			1.101	1.123	1.145	TPS7301QD	TPS7301QP	TPS7301QPW	TPS7301Y

The D and PW packages are available taped and reeled. Add an R suffix to device type (e.g., TPS7350QDR). The TPS7301Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

[§] The TPS7325 has a tolerance of $\pm 3\%$ over the full temperature range.

[¶] The TPS71xx and the TPS72xx are 500-mA and 250-mA output regulators respectively, offering performance similar to that of the TPS73xx but without the delayed-reset function. The TPS72xx devices are further differentiated by availability in 8-pin thin-shrink small-outline packages (TSSOP) for applications requiring minimum package size.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q

LOW-DROPOUT VOLTAGE REGULATORS

WITH INTEGRATED DELAYED RESET FUNCTION

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description (continued)

The $\overline{\text{RESET}}$ output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

If that occurs, the $\overline{\text{RESET}}$ output (open-drain NMOS) turns on, taking the $\overline{\text{RESET}}$ signal low. $\overline{\text{RESET}}$ stays low for the duration of the undervoltage condition. Once the undervoltage condition ceases, a 200-ms (typ) time-out begins. At the completion of the 200-ms delay, $\overline{\text{RESET}}$ goes high.

An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 35 mV at an output current of 100 mA for the TPS7350) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and remains constant, independent of output loading (typically 340 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The LDO family also features a sleep mode; applying a logic high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at $T_J = 25^\circ\text{C}$.

The TPS73xx is offered in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for the 2.5 V and the adjustable version). The TPS73xx family is available in PDIP (8 pin), SO (8 pin) and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

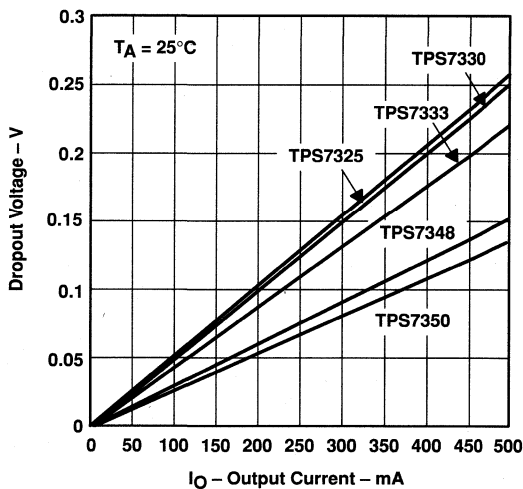
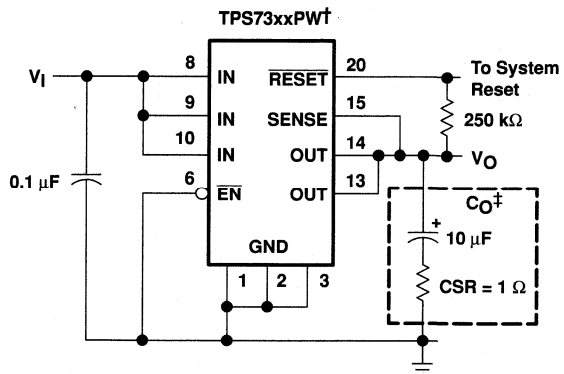


Figure 1. Dropout Voltage Versus Output Current



† TPS7325, TPS7330, TPS7333, TPS7348, TPS7350 (fixed-voltage options)

‡ Capacitor selection is nontrivial. See application information section for details.

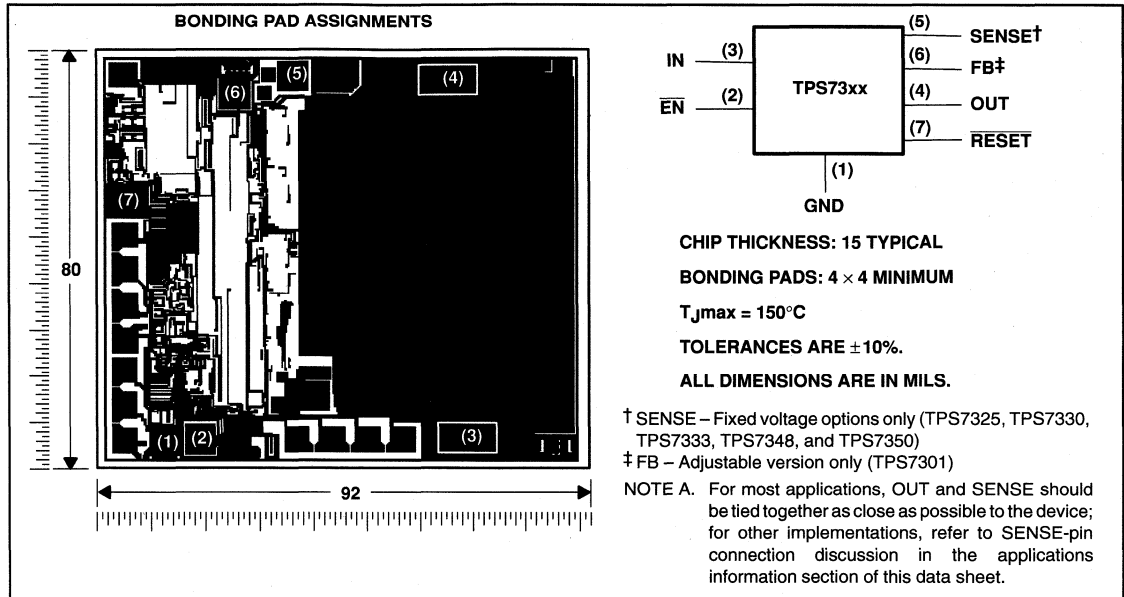
Figure 2. Typical Application Configuration

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

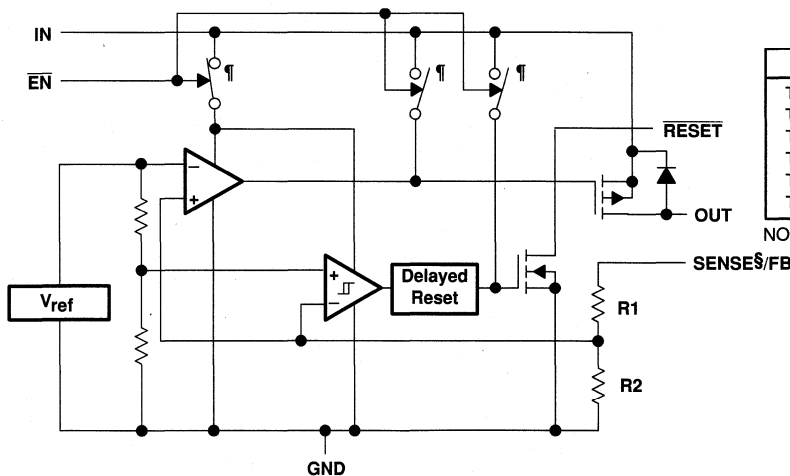
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TPS73xxY chip information

These chips, when properly assembled, display characteristics similar to those of the TPS73xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7301	0	∞	Ω
TPS7325	260	233	k Ω
TPS7330	358	233	k Ω
TPS7333	420	233	k Ω
TPS7348	726	233	k Ω
TPS7350	756	233	k Ω

NOTE A. Resistors are nominal values only.

COMPONENT COUNT

MOS transistors	464
Bipolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

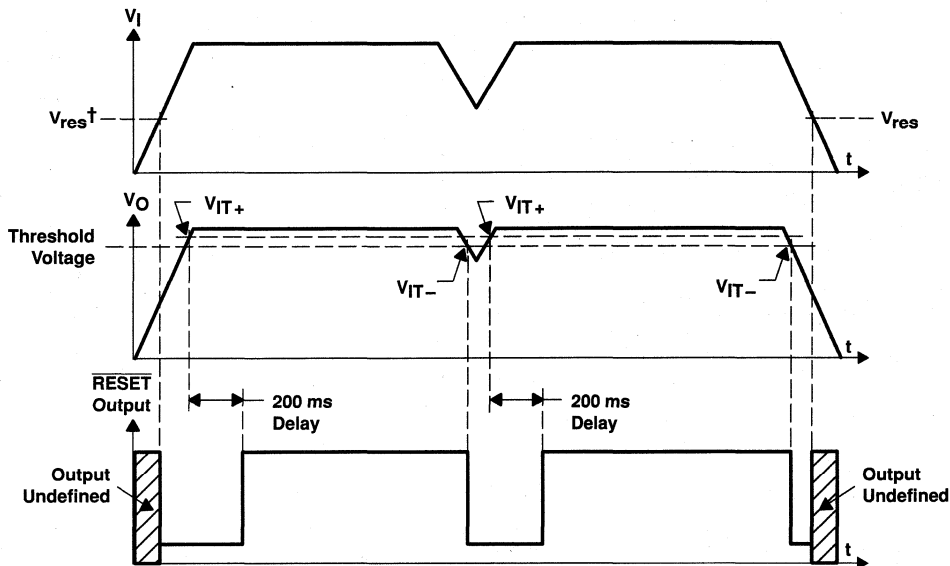
§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

¶ Switch positions are shown with EN low (active).

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
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timing diagram



† V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_i , RESET, SENSE, EN	–0.3 V to 11 V
Output current, I_O	2 A
Continuous total power dissipation	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
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DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (SEE FIGURE 3)

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW†	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (SEE FIGURE 4)

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
D	2188 mW	9.4 mW/°C	1765 mW	1248 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW†	4025 mW	32.2 mW/°C	2576 mW	805 mW

† Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP package.

**MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE**

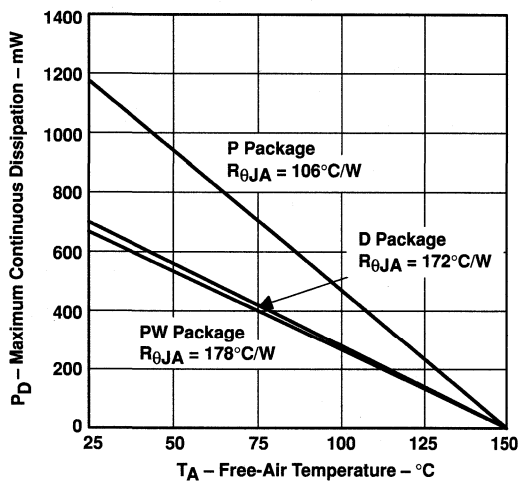


Figure 3

**MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE**

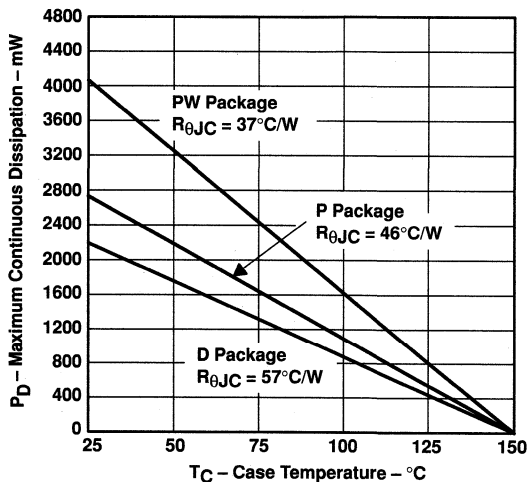


Figure 4

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I^\dagger	TPS7301Q	2.47	10	V
	TPS7325Q	3.1	10	
	TPS7330Q	3.5	10	V
	TPS7333Q	3.77	10	V
	TPS7348Q	5.2	10	
	TPS7350Q	5.33	10	
High-level input voltage at \overline{EN} , V_{IH}		2		V
Low-level input voltage at \overline{EN} , V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		-40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO} , at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

Because the TPS7301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the TPS7301 electrical characteristics table. The minimum value of 2.97 V is the absolute lower limit for the recommended input voltage range for the TPS7301.



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
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electrical characteristics at $I_O = 10 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ ($\text{CSR}^\ddagger = 1 \Omega$), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS [§]	T _J	MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{\text{EN}} \leq 0.5 \text{ V}$, $0 \text{ mA} \leq I_O \leq 500 \text{ mA}$	$V_I = V_O + 1 \text{ V}$, 25°C		340	400	μA
		-40°C to 125°C			550	
Input current (standby mode)	$\overline{\text{EN}} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C		0.01	0.5	μA
		-40°C to 125°C			2	
Output current limit	$V_O = 0 \text{ V}$, $V_I = 10 \text{ V}$	25°C		1.2	2	A
		-40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, $2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C		0.01	0.5	μA
		-40°C to 125°C			1	
$\overline{\text{RESET}}$ leakage current	Normal operation, V at $\overline{\text{RESET}} = 10 \text{ V}$	25°C		0.02	0.5	μA
		-40°C to 125°C			0.5	
Output voltage temperature coefficient		-40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{\text{EN}}$ logic high (standby mode)	$2.5 \text{ V} \leq V_I \leq 6 \text{ V}$ $6 \text{ V} \leq V_I \leq 10 \text{ V}$	-40°C to 125°C		2		V
				2.7		
$\overline{\text{EN}}$ logic low (active mode)	$2.7 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C			0.5	V
		-40°C to 125°C			0.5	
$\overline{\text{EN}}$ hysteresis voltage		25°C		50		mV
$\overline{\text{EN}}$ input current	$0 \text{ V} \leq V_I \leq 10 \text{ V}$	25°C	-0.5	0.001	0.5	μA
		-40°C to 125°C	-0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		-40°C to 125°C			2.5	
Minimum V_I for valid $\overline{\text{RESET}}$	$I_O(\overline{\text{RESET}}) = -300 \mu\text{A}$	25°C		1	1.5	V
		-40°C to 125°C			1.9	

[‡] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[§] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q

**LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION**

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TPS7301Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T _J	MIN	TYP	MAX	UNIT
Reference voltage (measured at FB)			25°C	1.182			V
	2.5 V ≤ V _I ≤ 10 V, See Note 1	5 mA ≤ I _O ≤ 500 mA,	-40°C to 125°C	1.147		1.217	V
Reference voltage temperature coefficient			-40°C to 125°C	61		75	ppm/°C
Pass-element series resistance (See Note 2)	V _I = 2.4 V,	50 μA ≤ I _O ≤ 150 mA	25°C	0.7		1	Ω
			-40°C to 125°C			1	
	V _I = 2.4 V,	150 mA ≤ I _O ≤ 500 mA	25°C	0.83		1.3	
			-40°C to 125°C			1.3	
	V _I = 2.9 V,	50 μA ≤ I _O ≤ 500 mA	25°C	0.52		0.85	
			-40°C to 125°C			0.85	
V _I = 3.9 V,	50 μA ≤ I _O ≤ 500 mA	25°C	0.32				
V _I = 5.9 V,	50 μA ≤ I _O ≤ 500 mA	25°C	0.23				
Input regulation	V _I = 2.5 V to 10 V, See Note 1	50 μA ≤ I _O ≤ 500 mA,	25°C	3		18	mV
			-40°C to 125°C			25	
Output regulation	2.5 V ≤ V _I ≤ 10 V, See Note 1	I _O = 5 mA to 500 mA,	25°C	5		14	mV
			-40°C to 125°C			25	
	2.5 V ≤ V _I ≤ 10 V, See Note 1	I _O = 50 μA to 500 mA,	25°C	7		22	mV
			-40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I _O = 50 μA	25°C	48		59	dB
			-40°C to 125°C			44	
		I _O = 500 mA, See Note 1	25°C	45		54	
			-40°C to 125°C			44	
Output noise-spectral density	f = 120 Hz		25°C	2		μV/√Hz	
Output noise voltage	10 Hz ≤ f ≤ 100 kHz	C _O = 4.7 μF	25°C	95		μV _{rms}	
		C _O = 10 μF	25°C	89			
		C _O = 100 μF	25°C	74			
RESET trip-threshold voltage§	V _{O(FB)} decreasing		-40°C to 125°C	1.101		1.145	V
RESET hysteresis voltage§	Measured at V _{O(FB)}		25°C	12			mV
RESET output low voltage§	V _I = 2.13 V,	I _{O(RESET)} = 400 μA	25°C	0.1		0.4	V
-40°C to 125°C					0.4		
FB input current			25°C	-10	0.1	10	nA
			-40°C to 125°C	-20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element r_{DS(on)} increases (see Figure 33) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation: V_{DO} = I_O · r_{DS(on)}

r_{DS(on)} is a function of both output current and input voltage. This parametric table lists r_{DS(on)} for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 33.



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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TPS7325Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ ($\text{CSRT} = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T _J	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.45	2.5	2.55	V
	3.5 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 500 mA		–40°C to 125°C	2.425		2.575	
Dropout voltage‡	I _O = 10 mA, V _I = 2.97 V		25°C	5			mV
			–40°C to 125°C			14	
	I _O = 100 mA, V _I = 2.97 V		25°C	50		80	
			–40°C to 125°C			150	
	I _O = 500 mA, V _I = 2.97 V		25°C	270		400	
			–40°C to 125°C			600	
Pass-element series resistance§	(2.97 V – V _O)/I _O , I _O = 500 mA	V _I = 2.97 V,	25°C	0.5		0.7	Ω
			–40°C to 125°C			1.4	
Input regulation	V _I = 3.5 V to 10 V, 50 μA ≤ I _O ≤ 500 mA		25°C	6		20	mV
			–40°C to 125°C			25	
Output regulation	I _O = 5 mA to 500 mA, 3.5 V ≤ V _I ≤ 10 V		25°C	20		32	mV
			–40°C to 125°C			50	
	I _O = 50 μA to 500 mA, 3.5 V ≤ V _I ≤ 10 V		25°C	28		60	mV
			–40°C to 125°C			100	
Ripple rejection	f = 120 Hz	I _O = 50 μA	25°C	50	53		dB
			–40°C to 125°C	49			
		I _O = 500 mA	25°C	49	53		
			–40°C to 125°C	32			
Output noise-spectral density	f = 120 Hz		25°C	2		μV/√Hz	
Output noise voltage	10 Hz ≤ f ≤ 100 kHz	C _O = 4.7 μF	25°C	274		μVrms	
		C _O = 10 μF	25°C	228			
		C _O = 100 μF	25°C	159			
RESET trip-threshold voltage	V _O decreasing		–40°C to 125°C	2.23	2.32	2.39	V
RESET output low voltage	V _I = 2.1 V, I _O (RESET) = –0.8 mA		25°C	0.14		0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Dropout test and pass-element series resistance test are not production tested. Test method requires SENSE terminal to be disconnected from output voltage.

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
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TPS7330Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	MIN	TYP	MAX	UNIT
Output voltage		25°C	3			V
	$4\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	2.94		3.06	
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 2.94\text{ V}$	25°C	5.2	7	mV	
		-40°C to 125°C	10			
	$I_O = 100\text{ mA}$, $V_I = 2.94\text{ V}$	25°C	52	75		
		-40°C to 125°C	100			
	$I_O = 500\text{ mA}$, $V_I = 2.94\text{ V}$	25°C	267	450		
		-40°C to 125°C	500			
Pass-element series resistance	$(2.94\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$, $V_I = 2.94\text{ V}$	25°C	0.5	0.7	Ω	
		-40°C to 125°C	1			
Input regulation	$V_I = 4\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	6	23	mV	
		-40°C to 125°C	29			
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$	25°C	20	32	mV	
		-40°C to 125°C	60			
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$	25°C	28	60	mV	
		-40°C to 125°C	120			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	43	53	dB
			-40°C to 125°C	40		
		$I_O = 500\text{ mA}$	25°C	39	53	
			-40°C to 125°C	36		
Output noise-spectral density	$f = 120\text{ Hz}$	25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		μVrms
		$C_O = 10\text{ }\mu\text{F}$	25°C	228		
		$C_O = 100\text{ }\mu\text{F}$	25°C	159		
RESET trip-threshold voltage	V_O decreasing	-40°C to 125°C	2.58	2.64	2.7	V
RESET output low voltage	$V_I = 2.6\text{ V}$, $I_O(\text{RESET}) = -0.8\text{ mA}$	25°C	0.14	0.4	V	
		-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
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TPS7333Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T _J	MIN	TYP	MAX	UNIT
Output voltage	4.3 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 500 mA	25°C		3.3		V
		–40°C to 125°C	3.23		3.37	
Dropout voltage	I _O = 10 mA, V _I = 3.23 V	25°C		4.5	7	mV
		–40°C to 125°C			8	
	I _O = 100 mA, V _I = 3.23 V	25°C		44	60	
		–40°C to 125°C			80	
	I _O = 500 mA, V _I = 3.23 V	25°C		235	300	
		–40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V _O)/I _O , I _O = 500 mA, V _I = 3.23 V	25°C		0.44	0.6	Ω
		–40°C to 125°C			0.8	
Input regulation	V _I = 4.3 V to 10 V, 50 μA ≤ I _O ≤ 500 mA	25°C		6	23	mV
		–40°C to 125°C			29	
Output regulation	I _O = 5 mA to 500 mA, 4.3 V ≤ V _I ≤ 10 V	25°C		21	38	mV
		–40°C to 125°C			75	
	I _O = 50 μA to 500 mA, 4.3 V ≤ V _I ≤ 10 V	25°C		31	60	mV
		–40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I _O = 50 μA	25°C	43	51	dB
			–40°C to 125°C			
		I _O = 500 mA	25°C	39	49	
			–40°C to 125°C			
Output noise-spectral density	f = 120 Hz	25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz	C _O = 4.7 μF	25°C		274	μVrms
		C _O = 10 μF	25°C		228	
		C _O = 100 μF	25°C		159	
$\overline{\text{RESET}}$ trip-threshold voltage	V _O decreasing	–40°C to 125°C	2.868			V
$\overline{\text{RESET}}$ hysteresis voltage		25°C		18		mV
$\overline{\text{RESET}}$ output low voltage	V _I = 2.8 V, I _O (RESET) = –1 mA	25°C		0.17	0.4	V
		–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q

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TPS7348Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 5.85\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS [‡]		T _J	MIN	TYP	MAX	UNIT
Output voltage			25°C		4.85		V
	5.85 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 500 mA		-40°C to 125°C	4.75		4.95	
Dropout voltage	I _O = 10 mA, V _I = 4.75 V		25°C		2.9	6	mV
			-40°C to 125°C			8	
	I _O = 100 mA, V _I = 4.75 V		25°C		28	37	
			-40°C to 125°C			54	
	I _O = 500 mA, V _I = 4.75 V		25°C		150	180	
			-40°C to 125°C			250	
Pass-element series resistance	(4.75 V - V _O)/I _O , I _O = 500 mA		25°C		0.28	0.37	Ω
	V _I = 4.75 V,		-40°C to 125°C			0.52	
Input regulation	V _I = 5.85 V to 10 V, 50 μA ≤ I _O ≤ 500 mA		25°C		9	35	mV
			-40°C to 125°C			37	
Output regulation	I _O = 5 mA to 500 mA, 5.85 V ≤ V _I ≤ 10 V		25°C		28	42	mV
			-40°C to 125°C			80	
	I _O = 50 μA to 500 mA, 5.85 V ≤ V _I ≤ 10 V		25°C		42	65	mV
			-40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I _O = 50 μA	25°C		42	53	dB
			-40°C to 125°C			39	
		I _O = 500 mA	25°C		39	50	
			-40°C to 125°C			35	
Output noise-spectral density	f = 120 Hz		25°C		2	μV/√Hz	
Output noise voltage	10 Hz ≤ f ≤ 100 kHz		25°C		410	μV _{rms}	
			25°C		328		
			25°C		212		
$\overline{\text{RESET}}$ trip-threshold voltage	V _O decreasing		-40°C to 125°C		4.5	4.7	V
$\overline{\text{RESET}}$ hysteresis voltage			25°C		26		mV
$\overline{\text{RESET}}$ output low voltage	I _O ($\overline{\text{RESET}}$) = -1.2 mA, V _I = 4.12 V		25°C		0.2	0.4	V
			-40°C to 125°C			0.4	

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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TPS7350Q electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSRT} = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T _J	MIN	TYP	MAX	UNIT
Output voltage			25°C	5			V
	$6\text{ V} \leq V_I \leq 10\text{ V}$,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	4.9	5.1		
Dropout voltage	$I_O = 10\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	2.9		6	mV
			-40°C to 125°C	8			
	$I_O = 100\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	27		35	
			-40°C to 125°C	50			
	$I_O = 500\text{ mA}$,	$V_I = 4.88\text{ V}$	25°C	146		170	
			-40°C to 125°C	230			
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$,	$V_I = 4.88\text{ V}$,	25°C	0.27	0.35		Ω
			$I_O = 500\text{ mA}$	-40°C to 125°C			
Input regulation	$V_I = 6\text{ V to } 10\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	4		25	mV
			-40°C to 125°C			45	
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	30		45	mV
			-40°C to 125°C			86	
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	45		65	mV
			-40°C to 125°C			140	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	43	53		dB
			-40°C to 125°C			38	
		$I_O = 500\text{ mA}$	25°C	41	51		
			-40°C to 125°C			36	
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	430		μV_{rms}	
		$C_O = 10\text{ }\mu\text{F}$	25°C	345			
		$C_O = 100\text{ }\mu\text{F}$	25°C	220			
RESET trip-threshold voltage	V_O decreasing		-40°C to 125°C	4.55	4.75		V
RESET hysteresis voltage			25°C	28		mV	
RESET output low voltage	$I_O(\text{RESET}) = -1.2\text{ mA}$, $V_I = 4.25\text{ V}$		25°C	0.15	0.4		V
			-40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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switching characteristics

PARAMETER	TEST CONDITIONS	T _J	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q			UNIT
			MIN	TYP	MAX	
$\overline{\text{RESET}}$ time-out delay	See Figure 5	25°C	140	200	260	ms
		-40°C to 125°C	100		300	

electrical characteristics at I_O = 10 mA, $\overline{\text{EN}}$ = 0 V, C_O = 4.7 μF (CSRT = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TPS7301Y, TPS7333Y TPS7348Y, TPS7350Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{\text{EN}} \leq 0.5 \text{ V}$, 0 mA ≤ I _O ≤ 500 mA		340		μA
Input current (standby mode)	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V _I ≤ 10 V		0.01		μA
Output current limit	V _O = 0 V, V _I = 10 V		1.2		A
Pass-element leakage current in standby mode	$\overline{\text{EN}} = V_I$, 2.7 V ≤ V _I ≤ 10 V		0.01		μA
$\overline{\text{RESET}}$ leakage current	Normal operation, V at $\overline{\text{RESET}} = 10 \text{ V}$		0.02		μA
Thermal shutdown junction temperature			165		°C
$\overline{\text{EN}}$ logic low (active mode)	2.7 V ≤ V _I ≤ 10 V			0.5	V
$\overline{\text{EN}}$ hysteresis voltage			50		mV
$\overline{\text{EN}}$ input current	0 V ≤ V _I ≤ 10 V		0.001		μA
Minimum V _I for active pass element			2.05		V
Minimum V _I for valid $\overline{\text{RESET}}$	I _O ($\overline{\text{RESET}}$) = -300 μA		1		V

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

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TPS7301Y electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSRT = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Reference voltage (measured at FB)			1.182			V
Pass-element series resistance (See Note 2)	$V_I = 2.4\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 150\text{ mA}$	0.7			Ω
	$V_I = 2.4\text{ V}$,	$150\text{ mA} \leq I_O \leq 500\text{ mA}$	0.83			
	$V_I = 2.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	0.52			
	$V_I = 3.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	0.32			
	$V_I = 5.9\text{ V}$,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	0.23			
Input regulation	$V_I = 2.5\text{ V to } 10\text{ V}$, See Note 1	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$,	3			mV
Output regulation	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$I_O = 5\text{ mA to } 500\text{ mA}$,	5			mV
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$, See Note 1	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$,	7			mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	59			dB
		$I_O = 500\text{ mA}$, See Note 1	54			
Output noise-spectral density	$f = 120\text{ Hz}$		2			$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	95			μVrms
		$C_O = 10\text{ }\mu\text{F}$	89			
		$C_O = 100\text{ }\mu\text{F}$	74			
$\overline{\text{RESET}}$ hysteresis voltage‡	Measured at $V_O(\text{FB})$		12			mV
$\overline{\text{RESET}}$ output low voltage‡	$V_I = 2.13\text{ V}$,	$I_O(\text{RESET}) = 400\text{ }\mu\text{A}$	0.1			V
FB input current			0.1			nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9\text{ V}$ and $I_O > 150\text{ mA}$ simultaneously, pass element $r_{DS(\text{on})}$ increases (see Figure 33) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation: $V_{DO} = I_O \cdot r_{DS(\text{on})}$

$r_{DS(\text{on})}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(\text{on})}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 33.

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TPS7325Y electrical characteristics at $I_O = 10 \text{ mA}$, $V_I = 3.5 \text{ V}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ ($\text{CSR}^\dagger = 1 \Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS [‡]		MIN	TYP	MAX	UNIT
Output voltage				2.5		V
Dropout voltage [§]	$I_O = 10 \text{ mA}$,	$V_I = 2.97 \text{ V}$		5		mV
	$I_O = 100 \text{ mA}$,	$V_I = 2.97 \text{ V}$		50		
	$I_O = 500 \text{ mA}$,	$V_I = 2.97 \text{ V}$		270		
Pass-element series resistance [§]	$(2.97 \text{ V} - V_O)/I_O$, $I_O = 500 \text{ mA}$	$V_I = 2.97 \text{ V}$,		0.5		Ω
Input regulation	$V_I = 3.5 \text{ V to } 10 \text{ V}$,	$50 \mu\text{A} \leq I_O \leq 500 \text{ mA}$		6		mV
Output regulation	$I_O = 5 \text{ mA to } 500 \text{ mA}$,	$3.5 \text{ V} \leq V_I \leq 10 \text{ V}$		20		mV
	$I_O = 50 \mu\text{A to } 500 \text{ mA}$,	$3.5 \text{ V} \leq V_I \leq 10 \text{ V}$		28		mV
Ripple rejection	$f = 120 \text{ Hz}$	$I_O = 50 \mu\text{A}$		53		dB
		$I_O = 500 \text{ mA}$		53		
Output noise-spectral density	$f = 120 \text{ Hz}$			2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	$C_O = 4.7 \mu\text{F}$		274		μVrms
		$C_O = 10 \mu\text{F}$		228		
		$C_O = 100 \mu\text{F}$		159		
RESET output low voltage	$V_I = 2.1 \text{ V}$,	$I_O(\text{RESET}) = -0.8 \text{ mA}$		0.14		V

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

[§] Dropout test and pass-element series resistance test are not production tested. Test method requires SENSE terminal to be disconnected from output voltage.

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TPS7330Y electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			3		V
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 2.94\text{ V}$		5.2		mV
	$I_O = 100\text{ mA}$, $V_I = 2.94\text{ V}$		52		
	$I_O = 500\text{ mA}$, $V_I = 2.94\text{ V}$		267		
Pass-element series resistance	$(2.94\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$, $V_I = 2.94\text{ V}$		0.5		Ω
Input regulation	$V_I = 4\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		6		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$		20		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$, $4\text{ V} \leq V_I \leq 10\text{ V}$		28		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		53	dB
		$I_O = 500\text{ mA}$		53	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} < f < 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		274	μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$		228	
		$C_O = 100\text{ }\mu\text{F}$		159	
RESET output low voltage	$V_I = 2.6\text{ V}$, $I_O(\text{RESET}) = -0.8\text{ mA}$		0.14		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7333Y electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			3.3		V
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 3.23\text{ V}$		4.5		mV
	$I_O = 100\text{ mA}$, $V_I = 3.23\text{ V}$		44		
	$I_O = 500\text{ mA}$, $V_I = 3.23\text{ V}$		235		
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$, $V_I = 3.23\text{ V}$		0.44		Ω
Input regulation	$V_I = 4.3\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		6		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$, $4.3\text{ V} \leq V_I \leq 10\text{ V}$		21		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$, $4.3\text{ V} \leq V_I \leq 10\text{ V}$		31		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		51	dB
		$I_O = 500\text{ mA}$		49	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		274	μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$		228	
		$C_O = 100\text{ }\mu\text{F}$		159	
RESET hysteresis voltage			18		mV
RESET output low voltage	$V_I = 2.8\text{ V}$, $I_O(\text{RESET}) = -1\text{ mA}$		0.17		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



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WITH INTEGRATED DELAYED RESET FUNCTION

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TPS7348Y electrical characteristics at $I_O = 10 \text{ mA}$, $V_I = 5.85 \text{ V}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ ($\text{CSR}^\dagger = 1 \Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
Output voltage				4.85		V
Dropout voltage	$I_O = 10 \text{ mA}$,	$V_I = 4.75 \text{ V}$		2.9		mV
	$I_O = 100 \text{ mA}$,	$V_I = 4.75 \text{ V}$		28		
	$I_O = 500 \text{ mA}$,	$V_I = 4.75 \text{ V}$		150		
Pass-element series resistance	$(4.75 \text{ V} - V_O)/I_O$, $I_O = 500 \text{ mA}$	$V_I = 4.75 \text{ V}$,		0.28		Ω
Input regulation	$V_I = 5.85 \text{ V}$ to 10 V ,	$50 \mu\text{A} \leq I_O \leq 500 \text{ mA}$		9		mV
Output regulation	$I_O = 5 \text{ mA}$ to 500 mA ,	$5.85 \text{ V} \leq V_I \leq 10 \text{ V}$		28		mV
	$I_O = 50 \mu\text{A}$ to 500 mA ,	$5.85 \text{ V} \leq V_I \leq 10 \text{ V}$		42		mV
Ripple rejection	$f = 120 \text{ Hz}$	$I_O = 50 \mu\text{A}$		53		dB
		$I_O = 500 \text{ mA}$		50		
Output noise-spectral density	$f = 120 \text{ Hz}$			2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10 \text{ Hz} \leq f \leq 100 \text{ kHz}$	$C_O = 4.7 \mu\text{F}$		410		μVrms
		$C_O = 10 \mu\text{F}$		328		
		$C_O = 100 \mu\text{F}$		212		
RESET hysteresis voltage				26		mV
RESET output low voltage	$I_O(\text{RESET}) = -1.2 \text{ mA}$, $V_I = 4.12 \text{ V}$			0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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TPS7350Y electrical characteristics at $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			5		V
Dropout voltage	$I_O = 10\text{ mA}$, $V_I = 4.88\text{ V}$		2.9	6	mV
	$I_O = 100\text{ mA}$, $V_I = 4.88\text{ V}$		27	35	
	$I_O = 500\text{ mA}$, $V_I = 4.88\text{ V}$		146	170	
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$, $I_O = 500\text{ mA}$, $V_I = 4.88\text{ V}$		0.27	0.35	Ω
Input regulation	$V_I = 6\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		4	25	mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$		28	75	mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$, $6\text{ V} \leq V_I \leq 10\text{ V}$		41		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		53	dB
		$I_O = 500\text{ mA}$		51	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		430	μV_{rms}
		$C_O = 10\text{ }\mu\text{F}$		345	
		$C_O = 100\text{ }\mu\text{F}$		220	
RESET hysteresis voltage			28		mV
RESET output low voltage	$I_O(\text{RESET}) = -1.2\text{ mA}$, $V_I = 4.25\text{ V}$		0.15	0.4	V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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PARAMETER MEASUREMENT INFORMATION

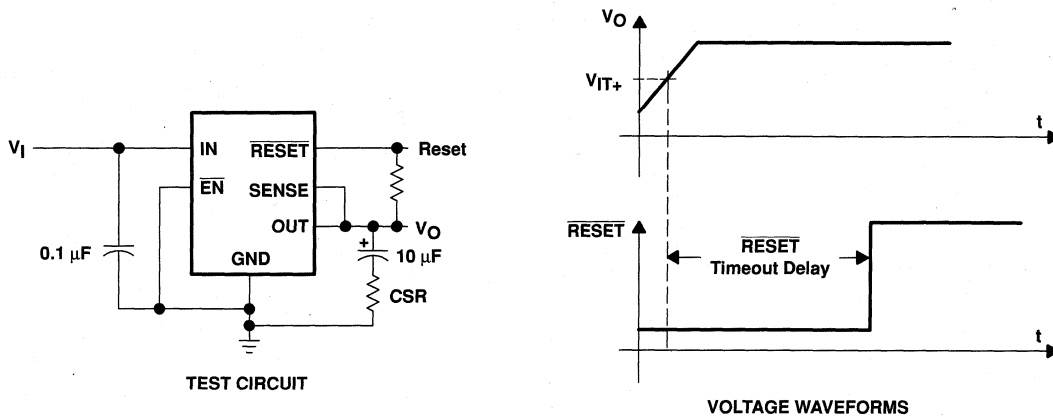
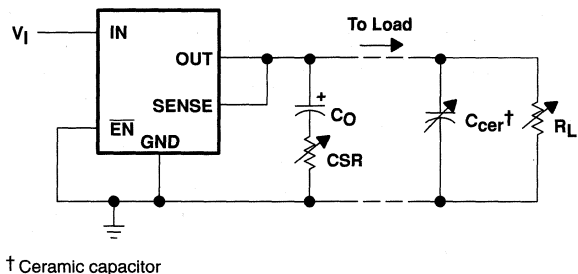


Figure 5. Test Circuit and Voltage Waveforms



† Ceramic capacitor

Figure 6. Test Circuit for Typical Regions of Stability (Refer to Figures 29 through 32)

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS

Table of Graphs

I _Q	Quiescent current		vs Output current	7
			vs Input voltage	8
I _Q	Quiescent current	TPS7348	vs Free-air temperature	9
I _Q	Quiescent current	TPS7325	vs Input voltage	10
			vs Free-air temperature	11
V _{DO}	Dropout voltage		vs Output current	12
ΔV _{DO}	Change in dropout voltage		vs Free-air temperature	13
V _{DO}	Dropout voltage	TPS7301	vs Output current	14
ΔV _O	Change in output voltage		vs Free-air temperature	15
V _O	Output voltage		vs Input voltage	16
V _O	Output voltage	TPS7325	vs Input voltage	17
	Line regulation			18
V _O	Output voltage	TPS7301	vs Output current	19
		TPS7325	vs Output current	20
		TPS7330	vs Output current	21
		TPS7333	vs Output current	22
		TPS7348	vs Output current	23
		TPS7350	vs Output current	24
	Output voltage response from enable (\overline{EN})			25
	Load transient response	TPS7301 or TPS7333		26
		TPS7325		27
		TPS7348 or TPS7350		28
		TPS7301		29
		TPS7333		30
	TPS7348 or TPS7350		31	
	Ripple rejection		vs Frequency	32
	Output spectral noise density		vs Frequency	33
	Compensation series resistance (CSR)	C _O = 4.7 μF	vs Output current	34
			vs Added ceramic capacitance	35
		C _O = 10 μF	vs Output current	36
			vs Added ceramic capacitance	37
r _{DS(on)}	Pass-element resistance		vs Input voltage	38
V _I	Minimum input voltage for valid \overline{RESET}		vs Free-air temperature	39
V _{IT-}	Negative-going reset threshold		vs Free-air temperature	40
I _{OL(RESET)}	\overline{RESET} output current		vs Input voltage	41
t _d	Reset time delay		vs Free-air temperature	42
t _d	Distribution for reset delay			43



TYPICAL CHARACTERISTICS

**QUIESCENT CURRENT
vs
OUTPUT CURRENT**

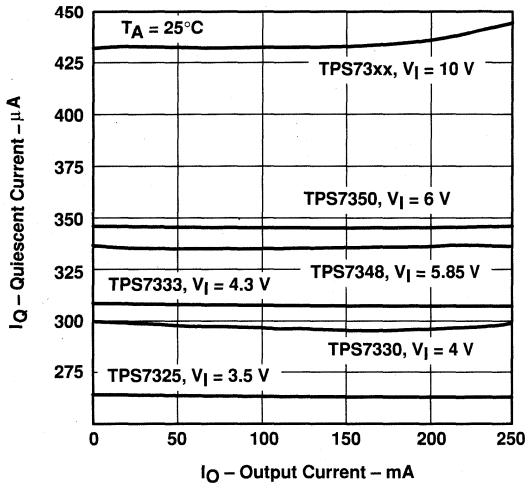


Figure 7

**QUIESCENT CURRENT
vs
INPUT VOLTAGE**

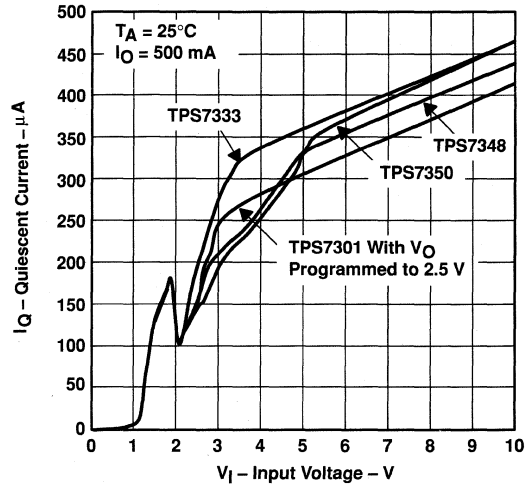


Figure 8

**TPS7348
QUIESCENT CURRENT
vs
FREE-AIR TEMPERATURE**

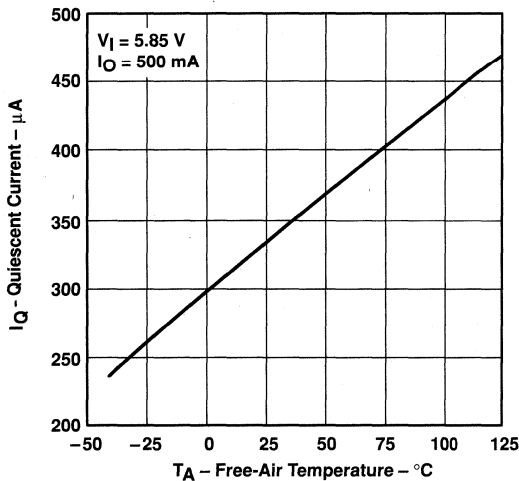


Figure 9

**TPS7325
QUIESCENT CURRENT
vs
INPUT VOLTAGE**

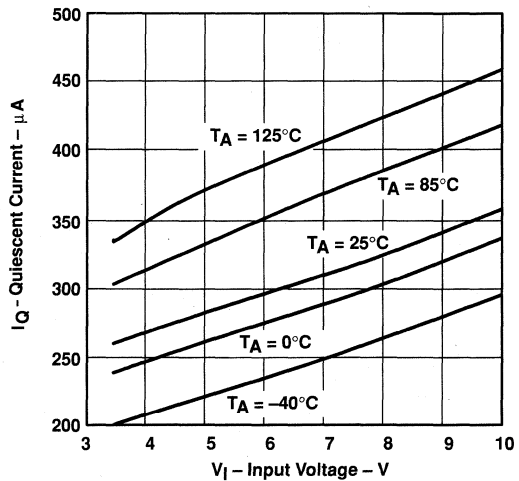


Figure 10

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
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WITH INTEGRATED DELAYED RESET FUNCTION

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TYPICAL CHARACTERISTICS

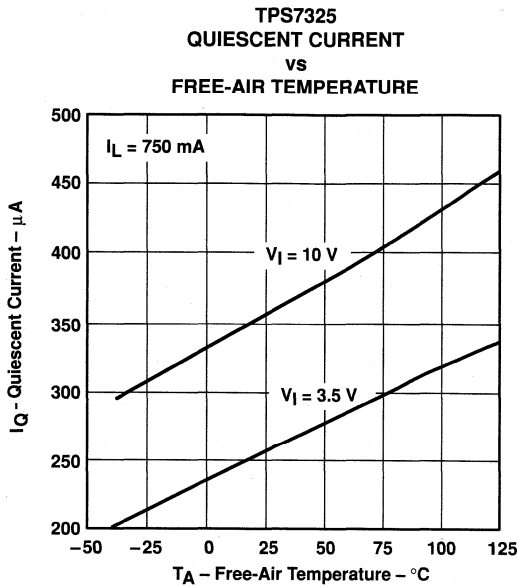


Figure 11

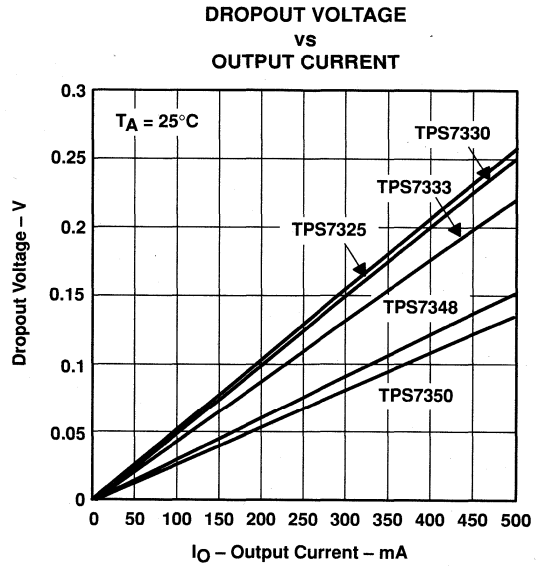


Figure 12

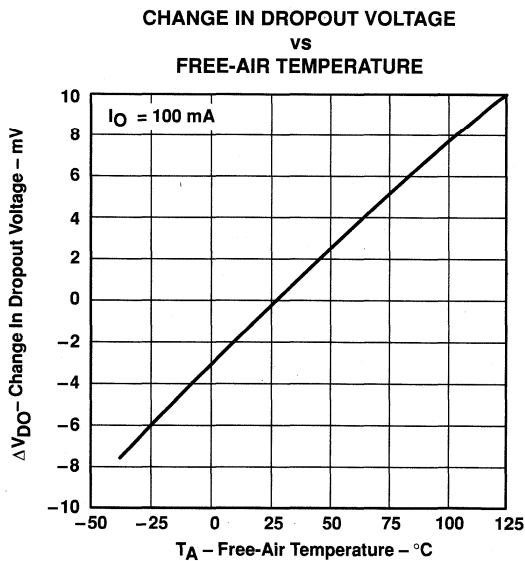


Figure 13

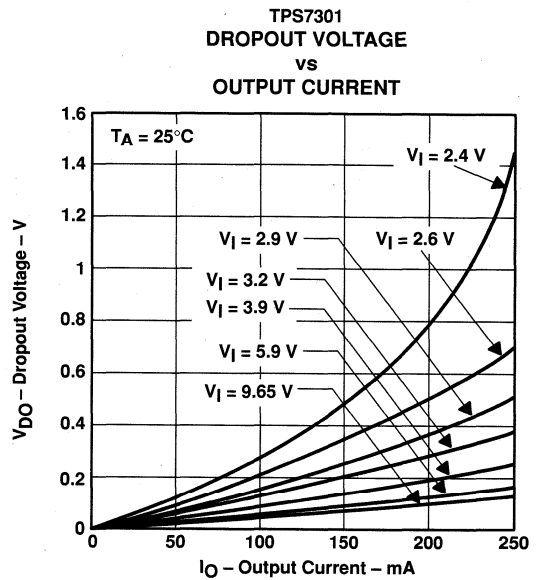


Figure 14

TYPICAL CHARACTERISTICS

**CHANGE IN OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE**

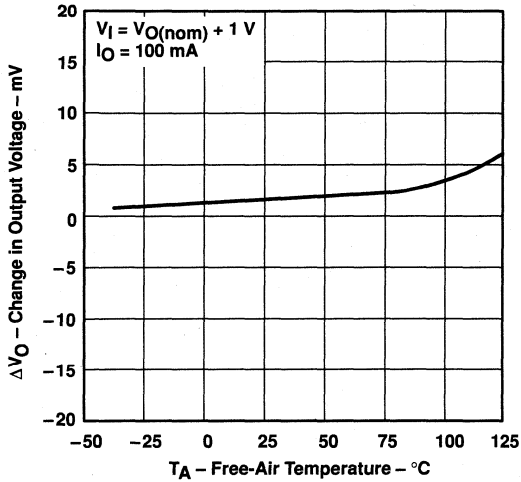


Figure 15

**OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE**

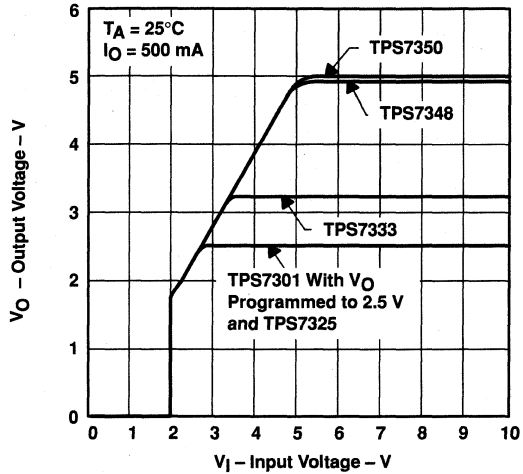


Figure 16

**TPS7325
 OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE**

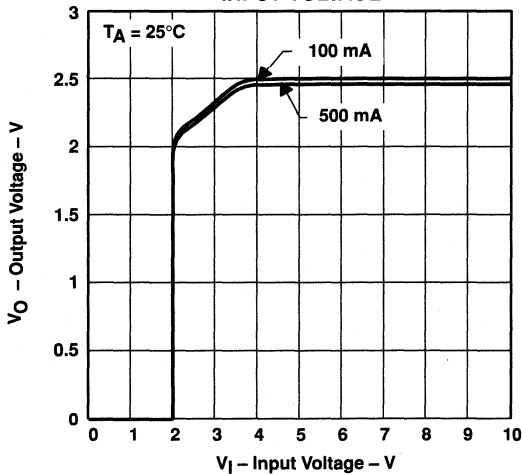


Figure 17

LINE REGULATION

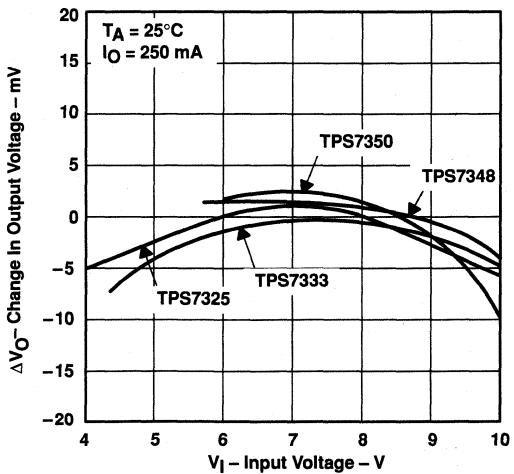
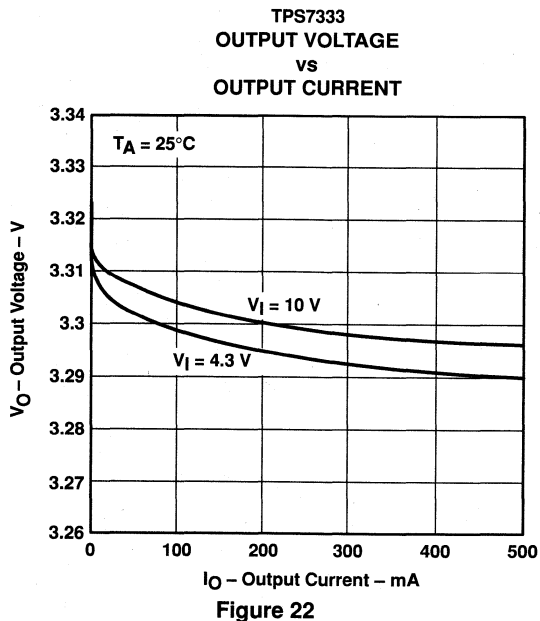
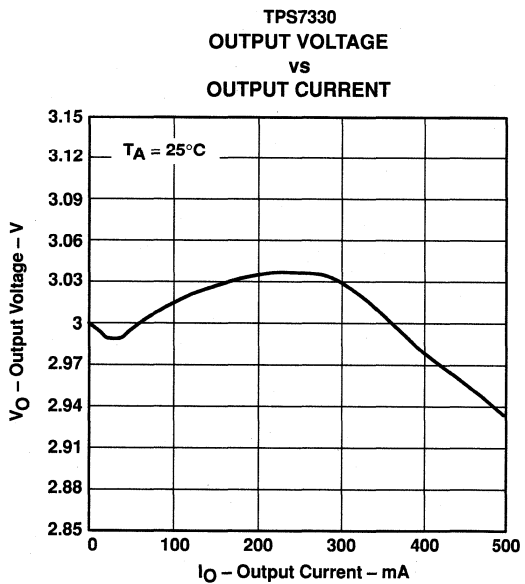
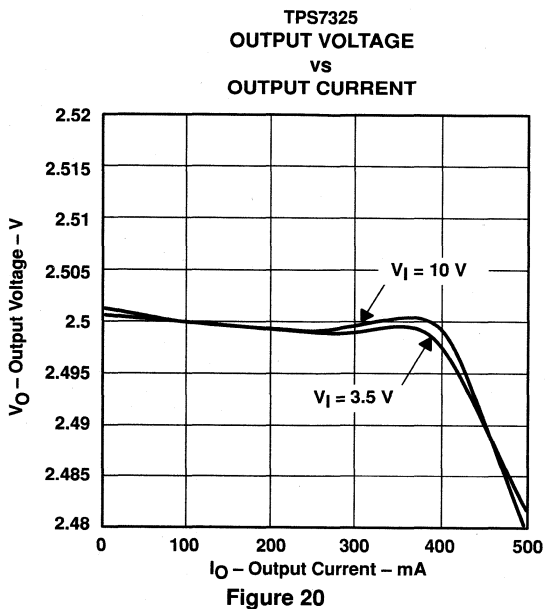
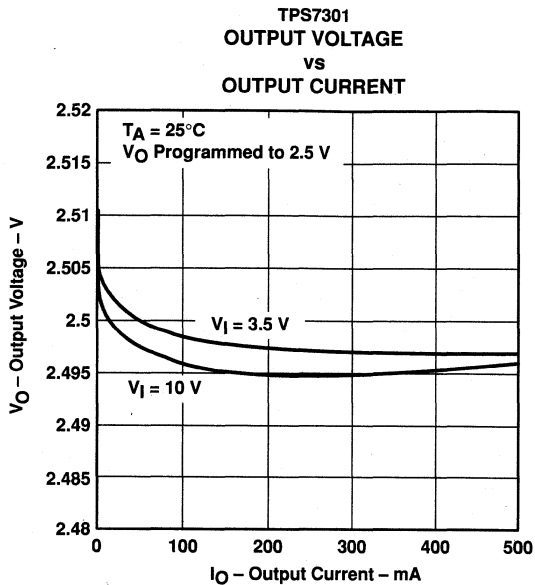


Figure 18

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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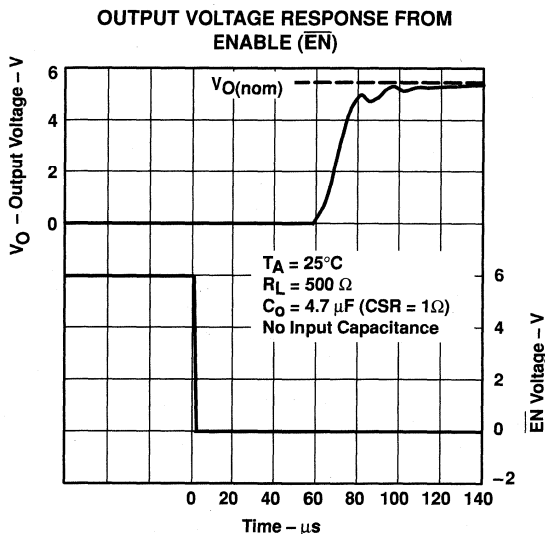
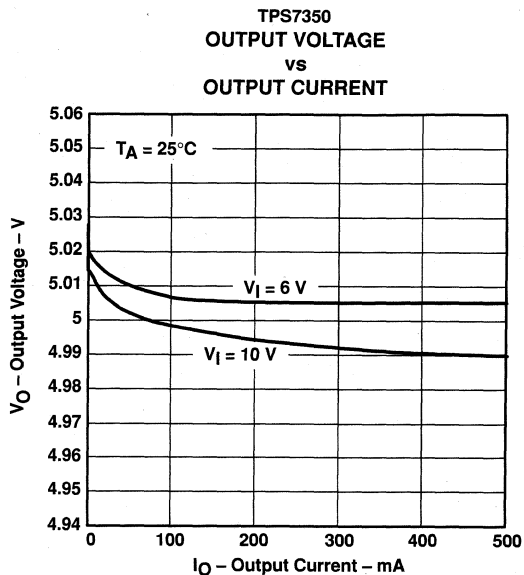
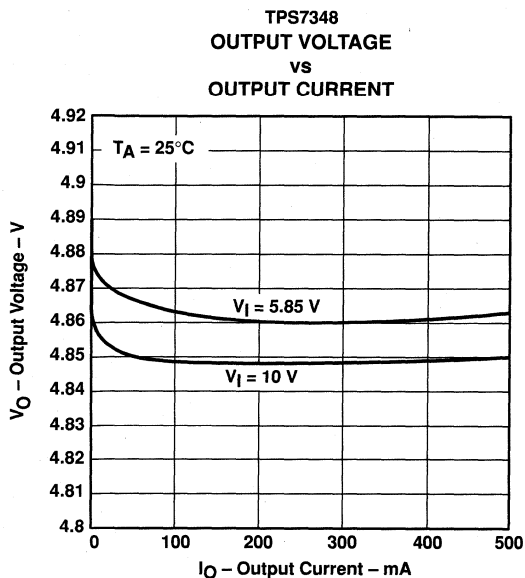
TYPICAL CHARACTERISTICS



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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TYPICAL CHARACTERISTICS



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION
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TYPICAL CHARACTERISTICS

TPS7301 (WITH V_O PROGRAMMED TO 2.5 V) OR TPS7333
LOAD TRANSIENT RESPONSE

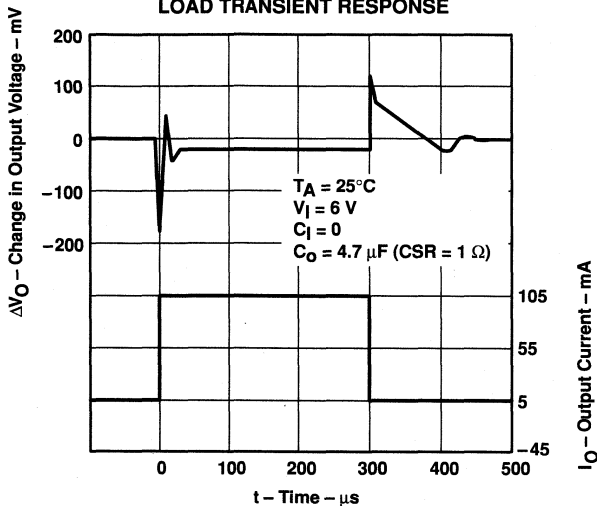


Figure 26

TPS7325
LOAD TRANSIENT RESPONSE

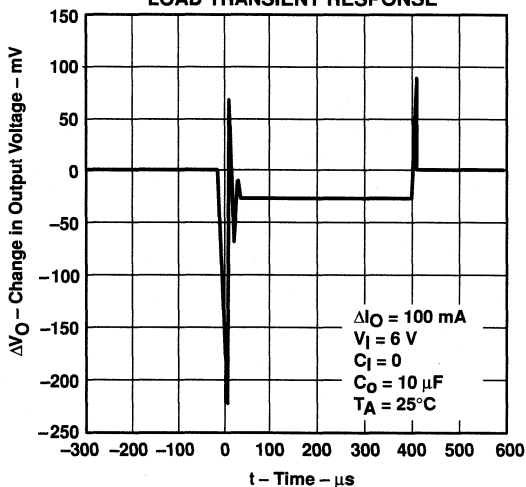


Figure 27

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION
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TYPICAL CHARACTERISTICS

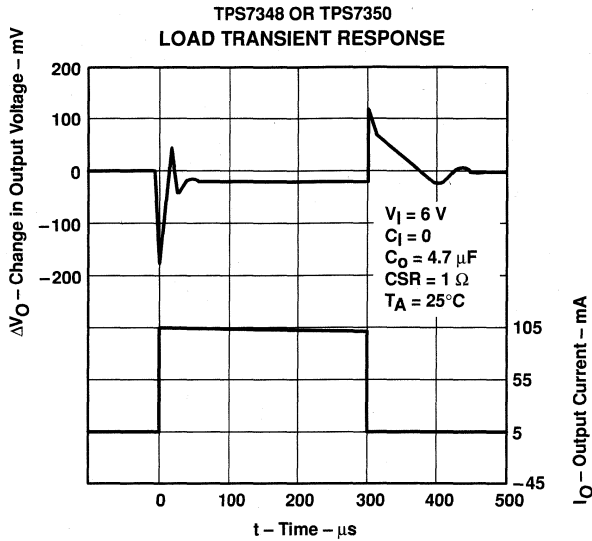


Figure 28

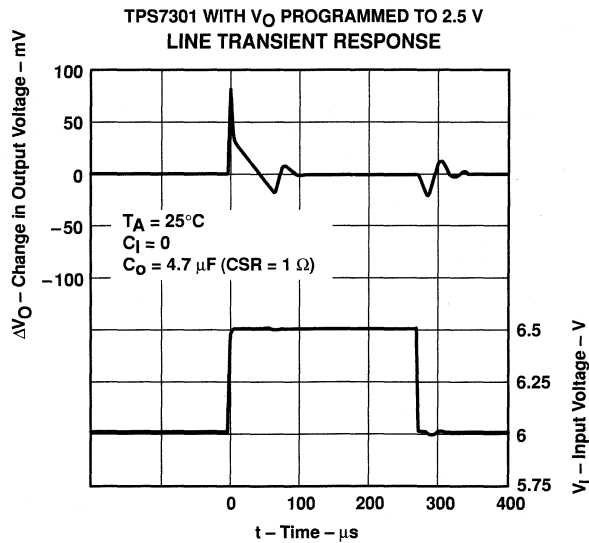


Figure 29

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
 LOW-DROPOUT VOLTAGE REGULATORS
 WITH INTEGRATED DELAYED RESET FUNCTION

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TYPICAL CHARACTERISTICS

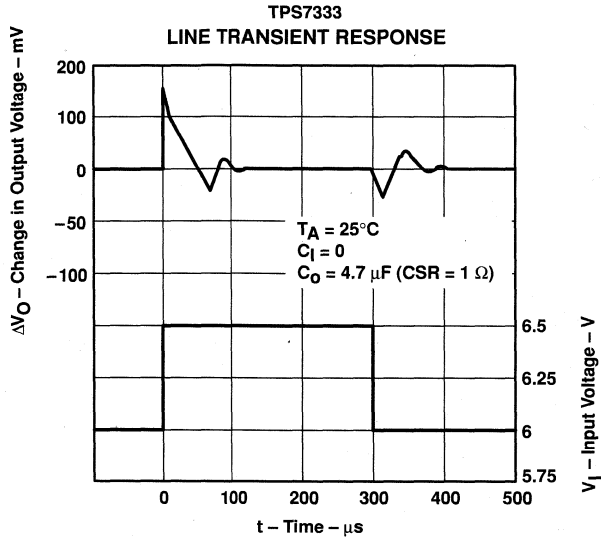


Figure 30

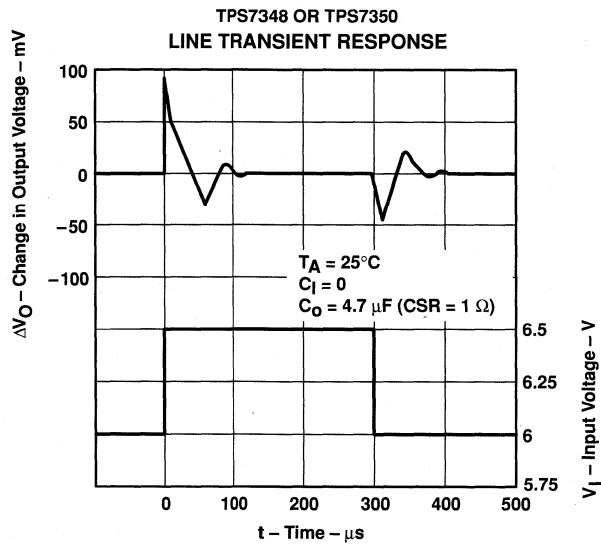


Figure 31

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS

**RIPPLE REJECTION
 vs
 FREQUENCY**

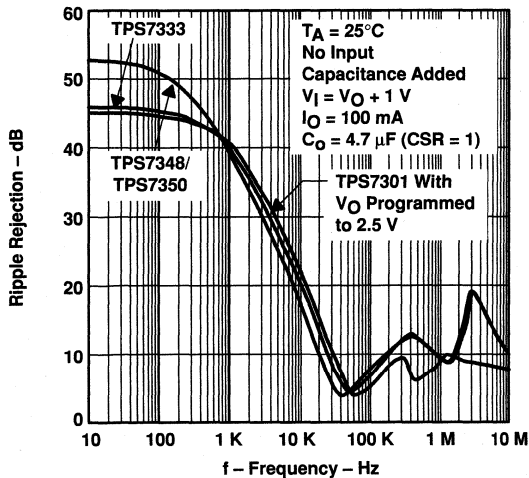


Figure 32

**OUTPUT SPECTRAL-NOISE DENSITY
 vs
 FREQUENCY**

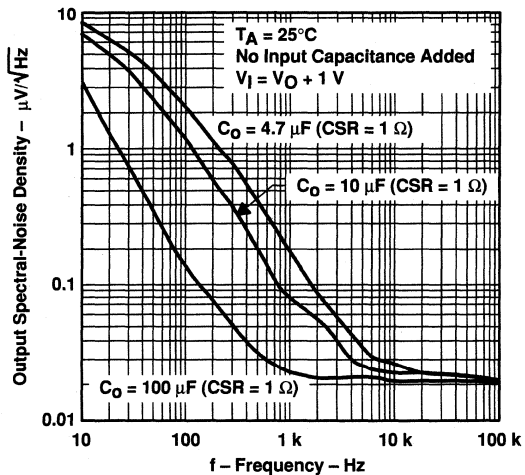


Figure 33

**TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 OUTPUT CURRENT**

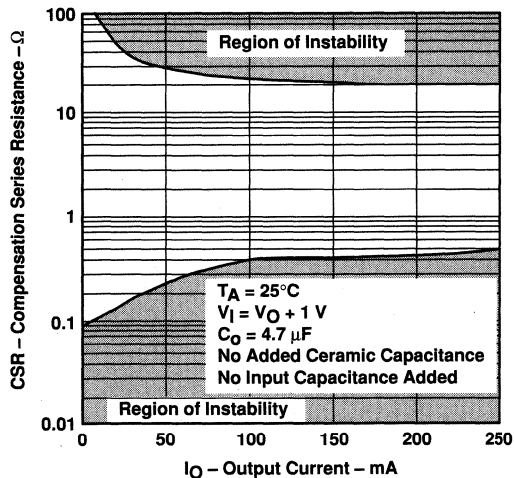


Figure 34

**TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 ADDED CERAMIC CAPACITANCE**

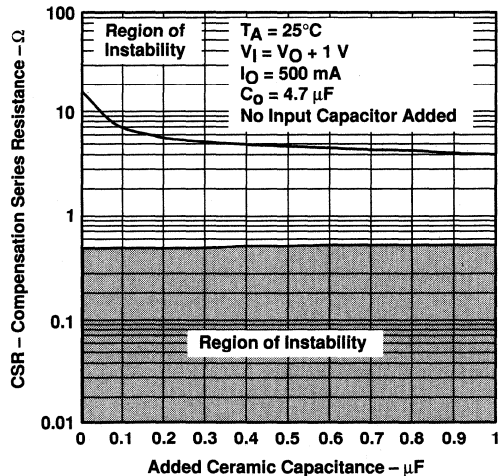


Figure 35



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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TYPICAL CHARACTERISTICS

**TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 OUTPUT CURRENT**

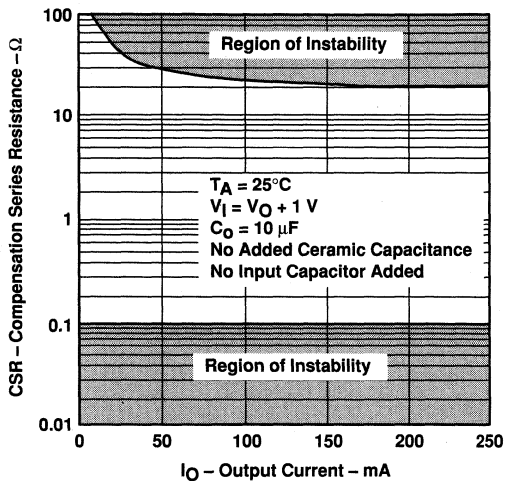


Figure 36

**TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 ADDED CERAMIC CAPACITANCE**

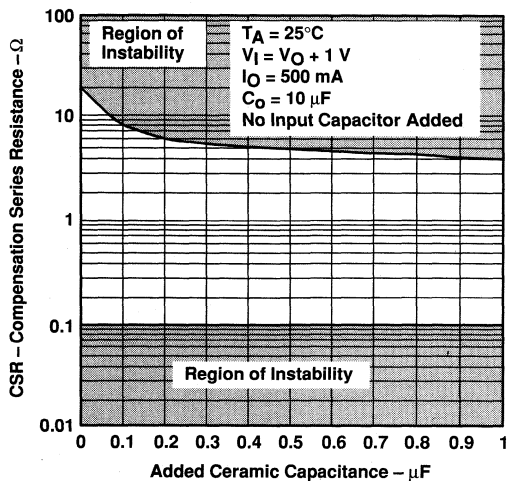


Figure 37

**PASS-ELEMENT RESISTANCE
 vs
 INPUT VOLTAGE**

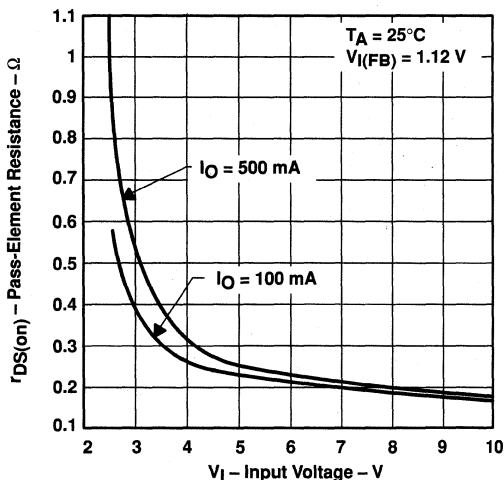


Figure 38

**MINIMUM INPUT VOLTAGE FOR VALID RESET
 vs
 FREE-AIR TEMPERATURE**

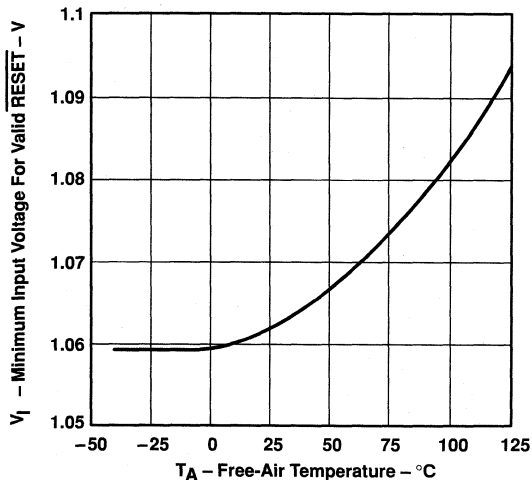


Figure 39



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q
LOW-DROPOUT VOLTAGE REGULATORS
WITH INTEGRATED DELAYED RESET FUNCTION

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TYPICAL CHARACTERISTICS

NEGATIVE-GOING RESET THRESHOLD
vs
FREE-AIR TEMPERATURE

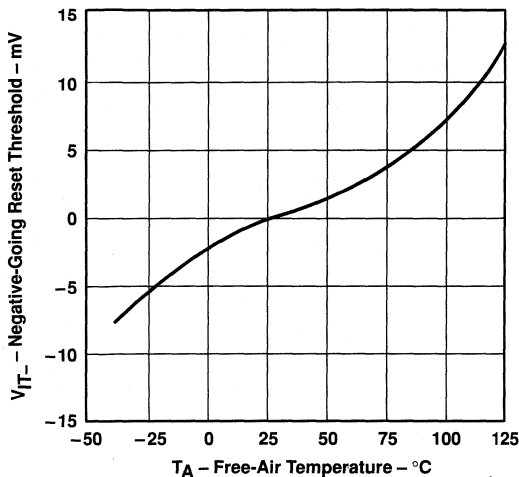


Figure 40

RESET OUTPUT CURRENT
vs
INPUT VOLTAGE

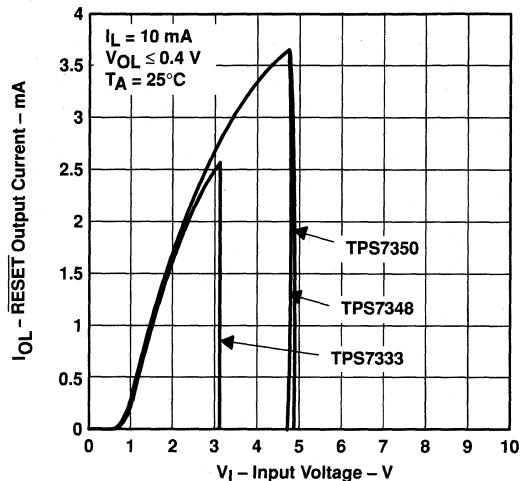


Figure 41

RESET DELAY TIME
vs
FREE-AIR TEMPERATURE

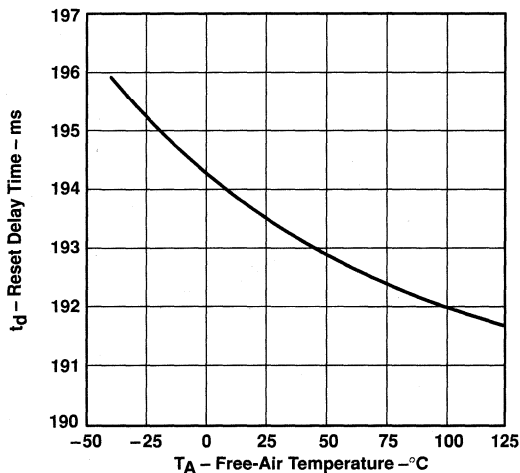


Figure 42

DISTRIBUTION FOR RESET DELAY

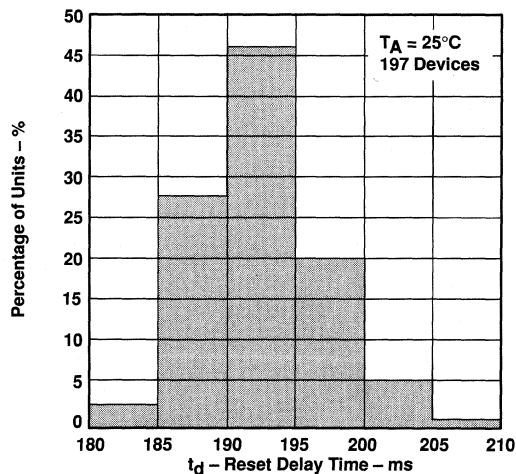


Figure 43

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 44 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ (thermal resistance, junction-to-ambient) for this component/board system is illustrated in Figure 45. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board ($L \times W \times H = 3.2 \text{ inch} \times 3.2 \text{ inch} \times 0.062 \text{ inch}$); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 46 shows the thermal resistance for the same system with the addition of a thermally-conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is $0.815 \text{ W/m} \times ^\circ\text{C}$.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA(\text{system})}}$$

Where

$T_{J(\text{max})}$ is the maximum allowable junction temperature; 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation.

This limit should then be applied to the internal power dissipated by the TPS73xx regulator. The equation for calculating total internal power dissipation of the TPS73xx is:

$$P_{D(\text{total})} = (V_I - V_O) \times I_O + V_I \times I_Q$$

Because the quiescent current of the TPS73xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(\text{total})} = (V_I - V_O) \times I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55^\circ\text{C}$, airflow = 100 ft/min, and copper heat sink area = 1 cm^2 , the maximum power-dissipation limit can be calculated. As indicated in Figure 46, the system $R_{\theta JA}$ is 94°C/W ; therefore, the maximum power-dissipation limit is:

$$P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA(\text{system})}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{94^\circ\text{C/W}} = 745 \text{ mW}$$

If the system implements a TPS7348 regulator where $V_I = 6 \text{ V}$ and $I_O = 150 \text{ mA}$, the internal power dissipation is:

$$P_{D(\text{total})} = (V_I - V_O) \times I_O = (6 - 4.85) \times 0.150 = 173 \text{ mW}$$

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Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing either the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing either the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

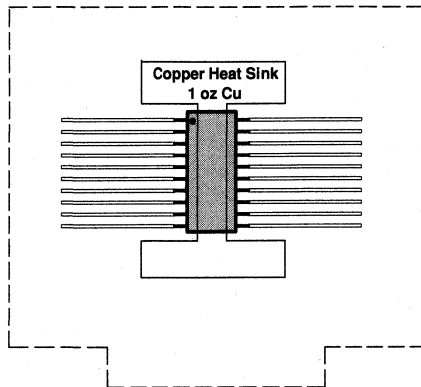
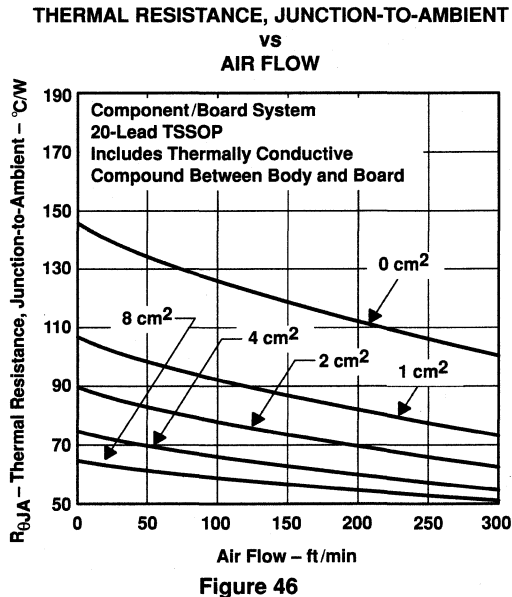
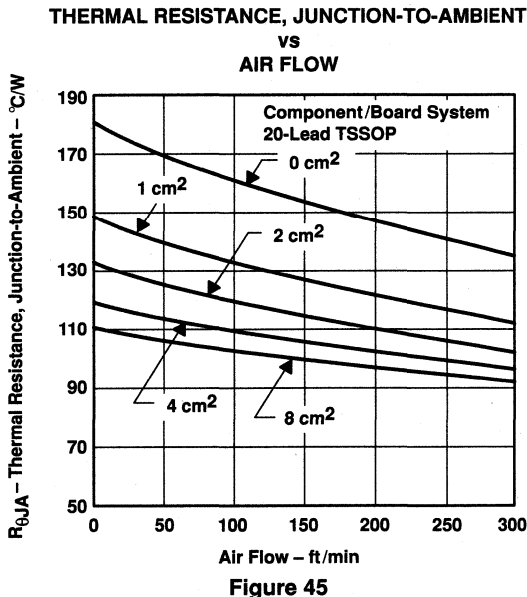


Figure 44. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP



TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

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APPLICATION INFORMATION

The TPS73xx series of low-dropout (LDO) regulators overcome many of the shortcomings of earlier generation LDOs, while adding features such as a power-saving shutdown mode and a supply-voltage supervisor. The TPS73xx family includes five fixed-output voltage regulators: the TPS7325 (2.5 V), TPS7330 (3 V), TPS7333 (3.3 V), the TPS7348 (4.85 V), and the TPS7350 (5 V). The family also offers an adjustable device, the TPS7301 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS73xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that such devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves (see Figure 7). The TPS73xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS73xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power-up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS73xx quiescent current remains low even when the regulator drops out, thus eliminating both problems.

Included in the TPS73xx family is a 4.85-V regulator, the TPS7348. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within $\pm 2\%$, allows for operation within the low-end limit of 5-V systems specified to $\pm 5\%$ tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS73xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under $0.5 \mu\text{A}$. When the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs .

minimum load requirements

The TPS73xx family is stable even at zero load; no minimum load is required for operation.

SENSE connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS73xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.



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external capacitor requirements (continued)

As with most LDO regulators, the TPS73xx family requires an output capacitor for stability. A low-ESR 10- μ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 42). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106M035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m Ω (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- μ F devices can be screened for ESR. Figures 29 through 32 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μ F), the output capacitance can be reduced to 4.7 μ F, provided ESR is maintained between 0.7 and 2.5 Ω . Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5- Ω to 1- Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 29 through 32), minimum ESR is not a problem when using 10- μ F or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73xx family. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 μ F of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μ F, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μ F, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μ F, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μ F, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μ F, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μ F, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μ F, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μ F, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μ F, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μ F, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μ F, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μ F, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μ F, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μ F, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

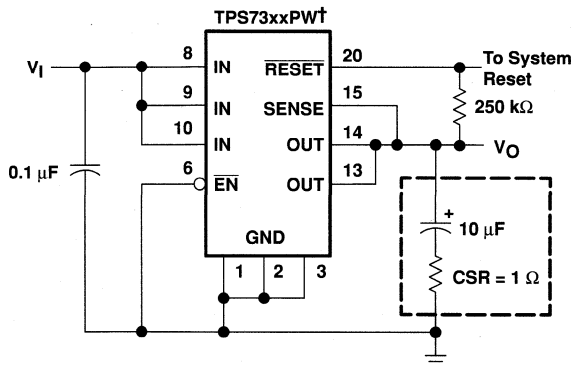


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external capacitor requirements (continued)



† TPS7333, TPS7348, TPS7350 (fixed-voltage options)

Figure 47. Typical Application Circuit

programming the TPS7301 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 43. The equation governing the output voltage is:

$$V_O = V_{\text{ref}} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where

V_{ref} = reference voltage, 1.182 V typ

TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q

LOW-DROPOUT VOLTAGE REGULATORS

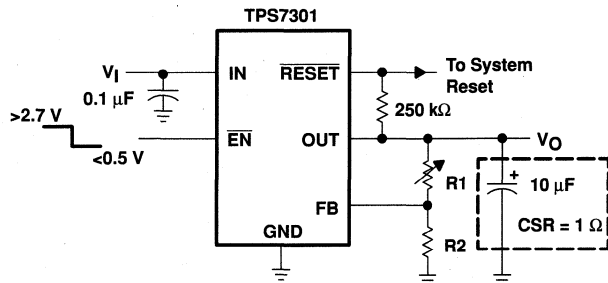
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Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. A recommended value for R2 is 169 k Ω with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \times R2$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	k Ω
3.3 V	309	169	k Ω
3.6 V	348	169	k Ω
4 V	402	169	k Ω
5 V	549	169	k Ω
6.4 V	750	169	k Ω

Figure 48. TPS7301 Adjustable LDO Regulator Programming

undervoltage supervisor function

The $\overline{\text{RESET}}$ output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on taking the $\overline{\text{RESET}}$ signal low.

On power up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typical) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output becomes inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pullup resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power-down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-} . Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typical) timeout period.

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undervoltage supervisor function (continued)

Transient loads or line pulses can also cause a reset to occur if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μ s can cause a reset if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1- μ s transient causes a reset when using an output capacitor with greater than 3.5 Ω of ESR. Note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1- μ s transient must drop at least 500 mV below the threshold before tripping the reset circuit. A 2- μ s transient trips RESET at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

NOTE:

$$V_{IT+} = V_{IT-} + \text{Hysteresis}$$

output noise

The TPS73xx has very low output noise, with a spectral noise density < 2 μ V/ $\sqrt{\text{Hz}}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

regulator protection

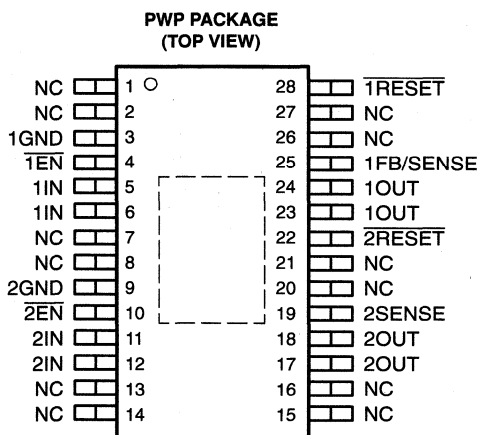
The TPS73xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS73xx also features internal current limiting and thermal protection. During normal operation, the TPS73xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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- Dual Output Voltages for Split-Supply Applications
- 3.3-V/Adjustable Output, 3.3 V/1.8 V, and 3.3 V/2.5
- Dropout Voltage < 80 mV Max at $I_O = 100$ mA (3.3-V option)
- Low Quiescent Current, Independent of Load . . . 340 μ A Typ Per Regulator
- Ultra-Low-Current Sleep State . . . 2 μ A Max
- Dual Active-Low Reset Signals with 200-ms Pulse Width
- Output Current Range of 0 mA to 750 mA Per Regulator
- 28-Pin PowerPAD™ TSSOP Package



description

NC – No internal connection

The TPS73HD3xx family of dual voltage regulators offers very low dropout voltages and dual outputs in a compact package. Designed primarily for DSP applications, these devices can be used in any mixed-output voltage application with each regulator supporting up to 750 mA. Output current can be allocated as desired between the two regulators and used to power many of today's DSPs. Low quiescent current and very low dropout voltage assure maximum power usage in battery-powered applications. Texas Instruments PowerPAD TSSOP package allows use of these devices with any voltage/current combination within the range of the listed specifications without thermal problems, provided proper device mounting procedures are followed. Separate inputs allow the designer to configure the source power as desired. Dual active-low reset signals allow resetting of core-logic and I/O separately. Remote sense/feedback terminals provide regulation at the load. The TPS73HD3xx are available in 28-pin PowerPAD TSSOP. They operate over a free-air temperature range of -40°C to 125°C .

AVAILABLE OPTIONS

T_A	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
-40°C to 125°C	Adj (1.2 – 9.75 V)	3.3 V	TPS73HD301PWPR
	1.8 V	3.3 V	TPS73HD318PWPR
	2.5 V	3.3 V	TPS73HD325PWPR

PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

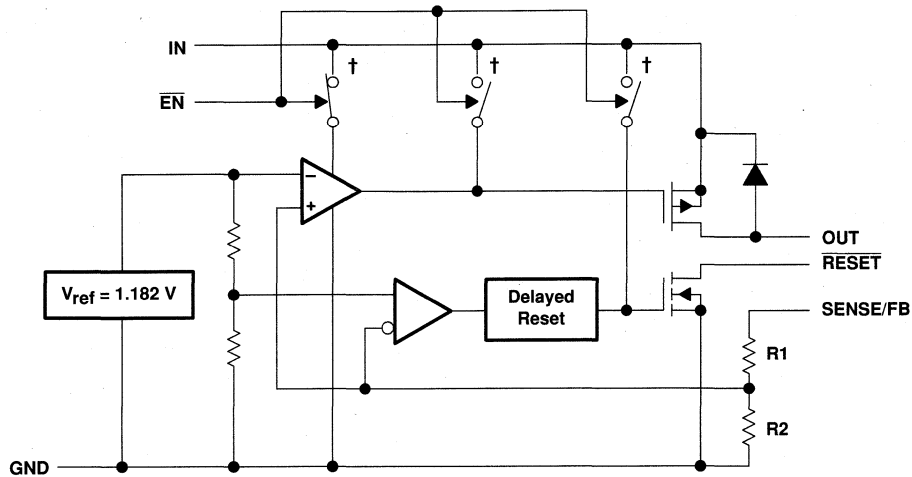


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TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram



† Switch positions shown with \overline{EN} low (active).

OUTPUT VOLTAGE	R1	R2	UNIT
Adjustable	0	∞	Ω
1.8 V	122	233	k Ω
2.5 V	260	233	k Ω
3.3 V	420	233	k Ω

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
NC	1, 2, 7, 8, 13–16, 20, 21, 26, 27		No connection
1GND	3		Regulator #1 ground
$\overline{1EN}$	4	I	Regulator #1 enable, low = enable
1IN	5, 6	I	Regulator #1 input supply voltage
2GND	9		Regulator #2 ground
$\overline{2EN}$	10	I	Regulator #2 enable, low = enable
2IN	11, 12	I	Regulator #2 input supply voltage
2OUT	17, 18	O	Regulator #2 output voltage
2SENSE	19	I	Regulator #2 output voltage sense (fixed output)
$\overline{2RESET}$	22	O	Regulator #2 reset signal, low = reset
1OUT	23, 24	O	Regulator #1 output voltage
1FB/SENSE	25	I	Regulator #1 output voltage feedback (adjustable output)
$\overline{1RESET}$	28	O	Regulator #1 reset signal, low = reset



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, V_I (xIN, \overline{xRESET} , xSENSE, \overline{xEN})	–0.3 V to 11 V
Differential input voltage, V_{ID} (1GND to 2GND)	2 V
Output current, I_O (1OUT, 2OUT)	2 A
Continuous total power dissipation	See Dissipation Rating Tables
Operating free-air temperature range, T_A	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES‡

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP‡	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP§	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

‡ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

§ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²).

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I †	Adjustable output (regulator #1)	2.97	10	V
Input voltage, V_I †	3.3-V output (regulator #2)	3.97	10	V
High-level input voltage at \overline{EN} , V_{IH}		2		V
Low-level input voltage at \overline{EN} , V_{IL}			0.5	V
Total output current range (per regulator), I_O		0	750	mA
Operating virtual junction temperature range, T_J		–40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO} , at the maximum specified load range (750 mA). Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

Because regulator 1 of the TPS373HD301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 in the TPS73HD301 electrical characteristics table. The minimum value of 3.5 V is the absolute lower limit for the recommended input voltage range for the TPS73HD301. With 2.97-V input voltage, the LDO may be in dropout and will not meet the 3% regulator output or 750-mA load current specification.

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electrical characteristics, $V_{I(IN)} = 4.3\text{ V}$, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSR}^\ddagger = 1\text{ }\Omega$,
SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	T _J	MIN	TYP	MAX	UNIT
Quiescent current (active mode), each regulator	EN ≤ 0.5 V, 0 mA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		340	415	μA
		-40°C to 125°C			550	
I _{CC} Supply current (standby mode), each regulator	EN = V _I , NOTE 2	25°C		0.01	0.5	μA
		-40°C to 125°C			2	
I _O Output current limit, each regulator	V _O = 0, V _I = 10 V	25°C	0.8	1.2	2	A
		-40°C to 125°C			2	
I _{lkg} Pass-element leakage current (standby mode)	EN = V _I , See NOTE 2	25°C		0.01	0.5	μA
		-40°C to 125°C			1	
Output voltage temperature coefficient		-40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
Logic high (EN) (standby mode)	2.5 V ≤ V _I ≤ 6 V, 6 V ≤ V _I ≤ 10 V	-40°C to 125°C	2			V
			2.7			
Logic low (EN) (active mode)	See NOTE 2	25°C			0.5	V
		-40°C to 125°C			0.5	
V _{hys} Hysteresis voltage (EN)		25°C		50		mV
I _I Input current (EN)	0 V ≤ V _I ≤ 10 V	25°C	-0.5	0.001	0.5	μA
		-40°C to 125°C	-0.5		0.5	
Minimum input voltage, for active pass element		25°C		2.05	2.5	V
		-40°C to 125°C			2.5	
Minimum input voltage, for valid RESET	I _O (RESET) = -300 μA	25°C		1	1.5	V
		-40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

NOTE 2: Minimum input voltage is 3.5V or V_O(typ) + 1V whichever is greater.

The minimum value of 3.5 V is the absolute lower limit for the recommended input voltage range for the TPS73HD301.

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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**electrical characteristics, $V_{I(IN)} = 4.3\text{ V}$, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSRT} = 1\text{ }\Omega$,
SENSE/FB shorted to OUT (unless otherwise noted) (continued)**

adjustable regulator

PARAMETER	TEST CONDITIONS†	T _J	MIN	TYP	MAX	UNIT	
Reference voltage (1FB)	5 mA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		1.182		V	
		–40°C to 125°C	1.147		1.217		
Reference voltage temperature coefficient		–40°C to 125°C		61	75	ppm/°C	
Pass-element series resistance (see Note 3)	50 μA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		0.52	1	Ω	
		–40°C to 125°C			1		
		V _I = 3.9 V, 50 μA ≤ I _O ≤ 750 mA	25°C		0.32		
	V _I = 5.9 V, 50 μA ≤ I _O ≤ 750 mA	25°C		0.23			
Input regulation	V _I = 3.5 V, 50 μA ≤ I _O ≤ 750 mA	25°C		3		mV	
Output regulation	I _O = 5 mA to 750 mA, See NOTE 2	25°C		7		mV	
	I _O = 50 μA to 750 mA, See NOTE 2	25°C		10		mV	
Ripple rejection	f = 120 Hz, I _O = 50 μA	25°C		59		dB	
	f = 120 Hz, I _O = 500 mA	25°C		54			
Output noise-spectral density	f = 120 Hz	25°C		2		mV/√Hz	
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C _L = 4.7 μF	25°C		95	μV/rms	
		C _L = 10 μF	25°C		89		
		C _L = 100 μF	25°C		74		
V _(TO)	Trip-threshold voltage (RESET)§	V _{O(FB)} decreasing	–40°C to 125°C	1.101	1.145	V	
V _{hys}	Hysteresis voltage (RESET)§	Measured at V _{O(ER)}	25°C	12		mV	
V _{OL}	Low-level output voltage (RESET)§	V _I = 2.13 V, I _{O(RESET)} = 400 μA	25°C	0.1	0.4	V	
			–40°C to 125°C		0.4		
I _I	Input current (1FB)		25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information)

NOTE 3: To calculate dropout voltage, use equation:

$$V_{DO} = I_O \times r_{DS(ON)}$$

r_{DS(ON)} is a function of both output current and input voltage. This parametric table lists r_{DS(ON)} for V_I = 3.9 V and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 4 V and 6 V respectively. For other programmed values, refer to Figure 29.

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electrical characteristics, $V_{I(IN)} = 4.3\text{ V}$, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}/\text{CSR}^\dagger = 1\text{ }\Omega$, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

1.8-V regulator (TPS73HD318)

PARAMETER		TEST CONDITIONS [‡]	T _J	MIN	TYP	MAX	UNIT
V _O	Output voltage	4.3 V ≤ V _I ≤ 10 V	25°C	1.746	1.8	1.854	V
			–40°C to 125°C	1.728		1.872	
Pass-element series resistance		(3.5 V – V _O)/I _O , I _O = 750 mA, V _I = 3.5 V, V _{2SENSE} = 0 V [§]	25°C		0.5	1	Ω
			–40°C to 125°C			1.2	
Input regulation		50 μA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		6		mV
Output regulation		I _O = 5 mA to 750 mA, See NOTE 2 I _O = 50 μA to 750 mA, See NOTE 2	25°C		14		mV
			25°C		18		
Ripple rejection		f = 120 Hz, I _O = 50 μA f = 120 Hz, I _O = 500 mA	25°C		51		dB
			25°C		49		
Output noise-spectral density		f = 120 Hz	25°C		2		mV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C _L = 4.7 μF	25°C		274		μV/rms
		C _L = 10 μF	25°C		228		
		C _L = 100 μF	25°C		159		

[†] CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

[§] Pass-element series resistance measured with sense pin disconnected from output to allow output voltage to rise to full saturation.

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electrical characteristics, $V_{I(IN)} = 4.3\text{ V}$, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F/CSR}\dagger = 1\text{ }\Omega$, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

2.5-V regulator (TPS73HD325)

PARAMETER		TEST CONDITIONS‡	T _J	MIN	TYP	MAX	UNIT
V _O	Output voltage	4.3 V ≤ V _I ≤ 10 V	25°C	2.45	2.5	2.55	V
			–40°C to 125°C	2.425		2.575	
	Dropout voltage	I _O = 750 mA, V _I = 3.5 V	–40°C to 125°C			800	mV
	Input regulation	50 μA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		6		mV
	Output regulation	I _O = 5 mA to 750 mA, See NOTE 2	25°C		20		mV
		I _O = 50 μA to 750 mA, See NOTE 2	25°C		25		mV
	Ripple rejection	f = 120 Hz, I _O = 50 μA	25°C		51		dB
		f = 120 Hz, I _O = 500 mA	25°C		49		
	Output noise-spectral density	f = 120 Hz	25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C _L = 4.7 μF	25°C		274	μV/rms
			C _L = 10 μF	25°C		228	
			C _L = 100 μF	25°C		159	
V _(TO)	Trip-threshold voltage (RESET)	V _O decreasing	–40°C to 125°C	2.172			V
V _{hys}	Hysteresis voltage (RESET)		25°C		18		mV
V _{OL}	Low-level output voltage (RESET)	V _I = 2.8 V, I _O (RESET) = –1 mA	25°C		0.17	0.4	V
			–40°C to 125°C			0.4	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Pass-element series resistance measured with sense pin disconnected from output to allow output voltage to rise to full saturation.

switching characteristics

PARAMETER	TEST CONDITIONS	T _J	MIN	TYP	MAX	UNIT
Time-out delay (RESET)	See Figure 3	25°C	140	200	260	ms
		–40°C to 125°C	100		300	

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electrical characteristics, $V_{I(IN)} = 4.3 \text{ V}$, $I_O = 10 \text{ mA}$, $\overline{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}/\text{CSRT} = 1 \Omega$, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

3.3-V regulator (TPS73HD301)

PARAMETER	TEST CONDITIONS†	T _J	MIN	TYP	MAX	UNIT
V _O Output voltage	4.3 V ≤ V _I ≤ 10 V	25°C		3.3		V
		–40°C to 125°C	3.23		3.37	
Dropout voltage	I _O = 10 mA, V _I = 3.23 V I _O = 100 mA, V _I = 3.23 V I _O = 750 mA, V _I = 3.23 V	25°C		4.5	10	mV
		25°C		44	100	
		25°C		353	750	
		–40°C to 125°C			800	
Pass-element series resistance	(3.23 V – V _O)/I _O , V _I = 3.23 V, I _O = 750 mA	25°C		0.44	1	Ω
		–40°C to 125°C			1.07	
Input regulation	50 μA ≤ I _O ≤ 750 mA, See NOTE 2	25°C		6		mV
Output regulation	I _O = 5 mA to 750 mA, See NOTE 2 I _O = 50 μA to 750 mA, See NOTE 2	25°C		30		mV
		25°C		37		mV
Ripple rejection	f = 120 Hz, I _O = 50 μA f = 120 Hz, I _O = 500 mA	25°C		51		dB
		25°C		49		
Output noise-spectral density	f = 120 Hz	25°C		2		mV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C _L = 4.7 μF	25°C		274	μV/rms
		C _L = 10 μF	25°C		228	
		C _L = 100 μF	25°C		159	
V _(TO) Trip-threshold voltage (RESET)	V _O decreasing	–40°C to 125°C	2.868			V
V _{hys} Hysteresis voltage (RESET)		25°C		18		mV
V _{OL} Low-level output voltage (RESET)	V _I = 2.8 V, I _O (RESET) = –1 mA	25°C		0.17	0.4	V
		–40°C to 125°C			0.4	

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

switching characteristics

PARAMETER	TEST CONDITIONS	T _J	MIN	TYP	MAX	UNIT
Time-out delay (RESET)	See Figure 3	25°C	140	200	260	ms
		–40°C to 125°C	100		300	



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PARAMETER MEASUREMENT INFORMATION

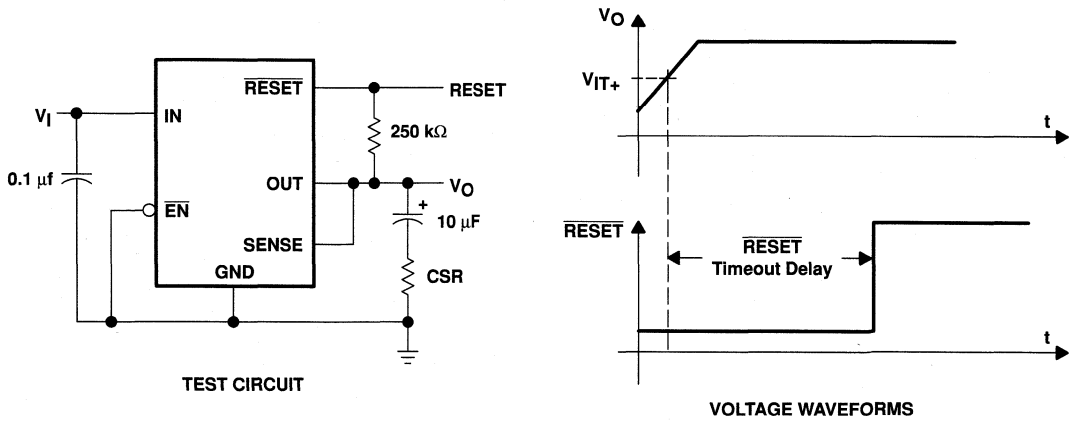


Figure 1. Test Circuit and Voltage Waveforms

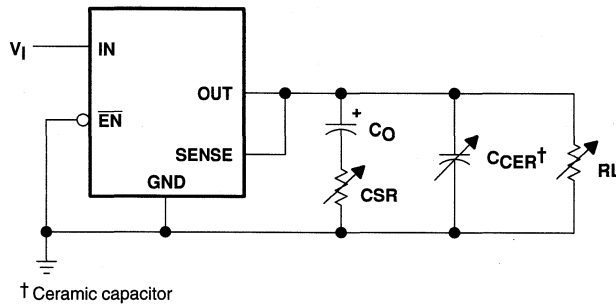


Figure 2. Test Circuit for Typical Regions of Stability (Refer to Figures 29 through 32)

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TYPICAL CHARACTERISTICS

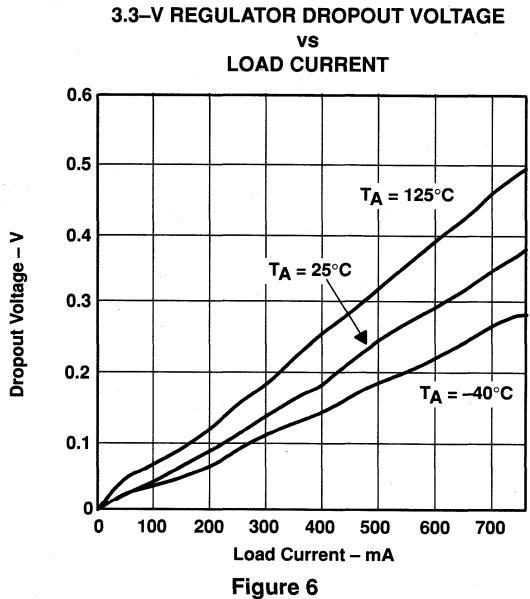
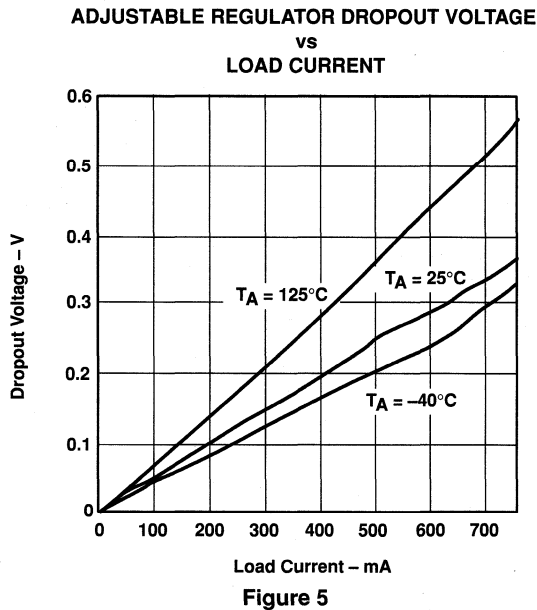
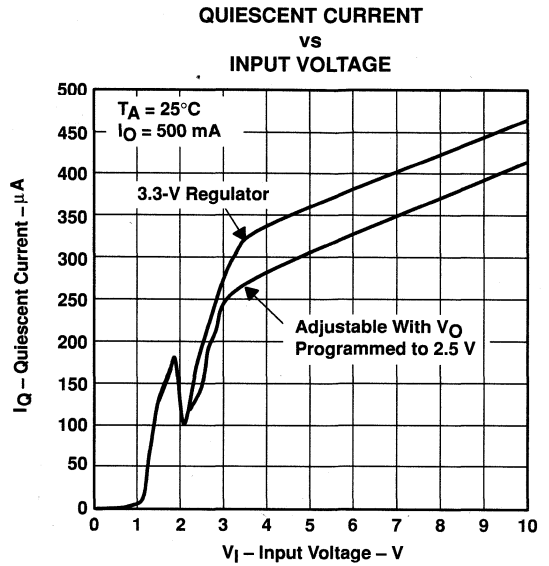
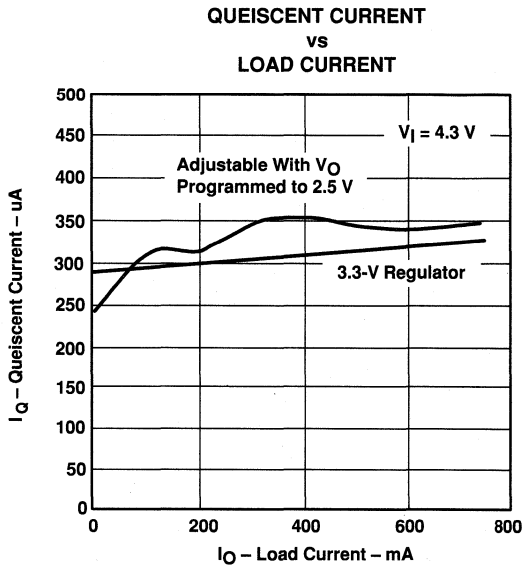
Table of Graphs

I_Q	Quiescent current		vs Load current	5	
			vs Input voltage	6	
V_{DO}	Dropout voltage	Adjustable regulator	vs Load current	7	
		3.3-V regulator	vs Load current	8	
ΔV_{DO}	Change in dropout voltage		vs Free-air temperature	9	
V_{DO}	Dropout voltage		vs Output current	10	
ΔV_O	Change in output voltage		vs Free-air temperature	11	
V_O	Output voltage		vs Input voltage	12	
	Line regulation			13	
V_O	Output voltage		vs Output current	14, 15	
	Output voltage response from enable (\overline{EN})			16	
	Load transient response	Adjustable regulator		17	
		3.3-V regulator		18	
	Line transient response	Adjustable regulator		19	
		3.3-V regulator		20	
	Ripple rejection		vs Frequency	21	
	Output spectral noise density		vs Frequency	22	
	Compensation series resistance (CSR)	Adjustable regulator	vs Output current	23	
			vs Added ceramic capacitance	24	
			vs Output current	25	
		3.3-V regulator	vs Output current	26	
			Adjustable regulator	vs Added ceramic capacitance	27
			3.3-V regulator	vs Added ceramic capacitance	28
$r_{DS(on)}$	Pass-element resistance		vs Input voltage	29	
V_I	Minimum input voltage for valid RESET		vs Free-air temperature	30	
V_{IT-}	Negative-going reset threshold		vs Free-air temperature	31	
$I_{OL(RESET)}$	RESET output current	3.3-V regulator	vs Input voltage	32	
t_d	Reset time delay		vs Free-air temperature	33	
t_d	Distribution for reset delay			34	

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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

**CHANGE IN DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

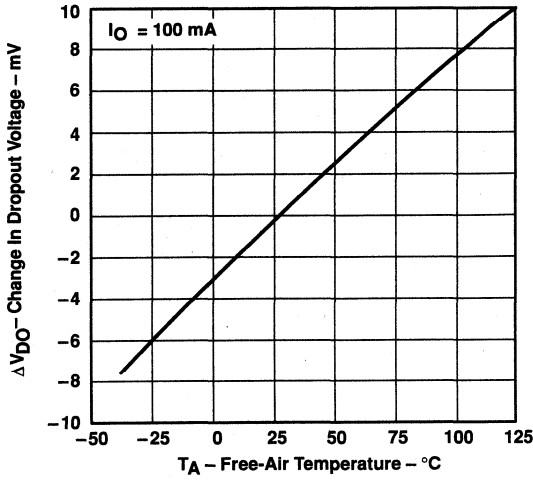


Figure 7

**DROPOUT VOLTAGE
vs
OUTPUT CURRENT**

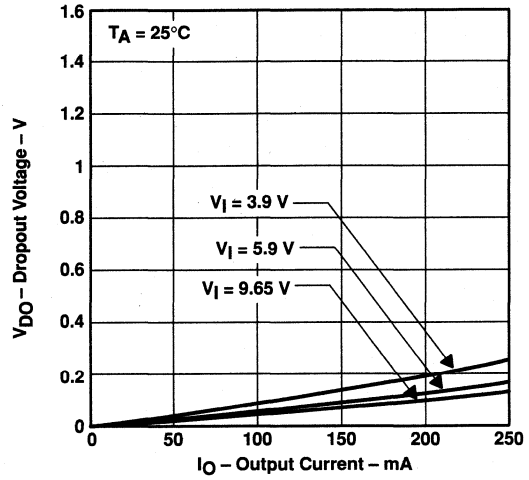


Figure 8

**CHANGE IN OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

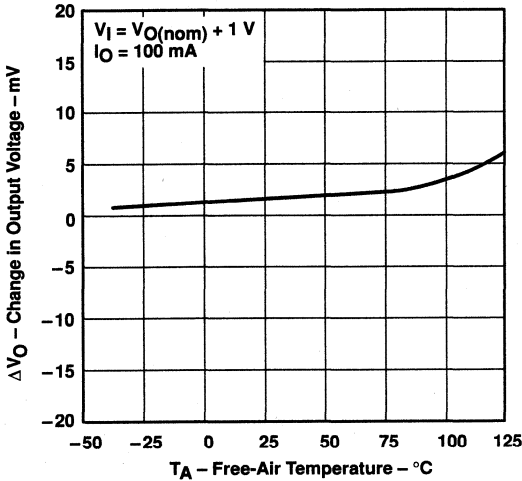


Figure 9

**OUTPUT VOLTAGE
vs
INPUT VOLTAGE**

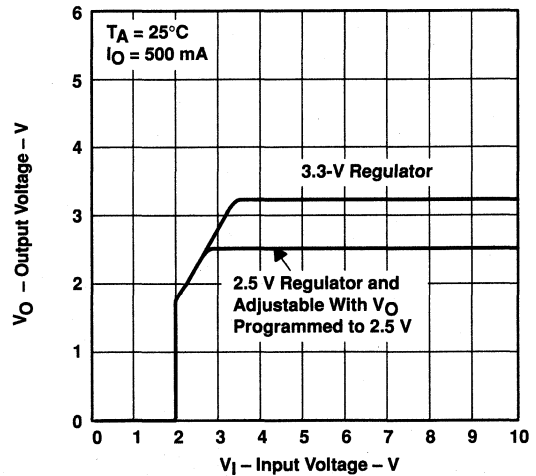
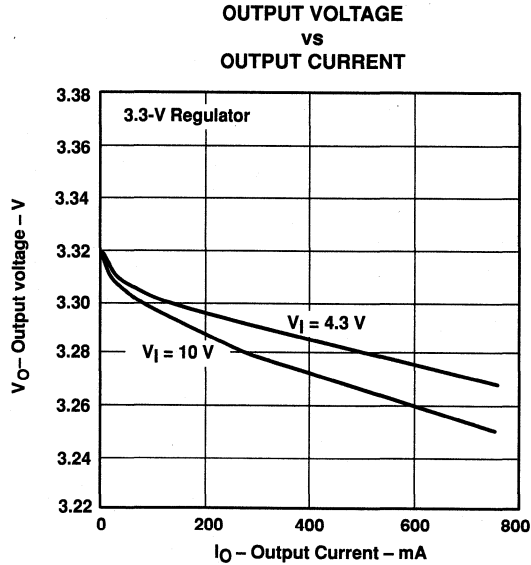
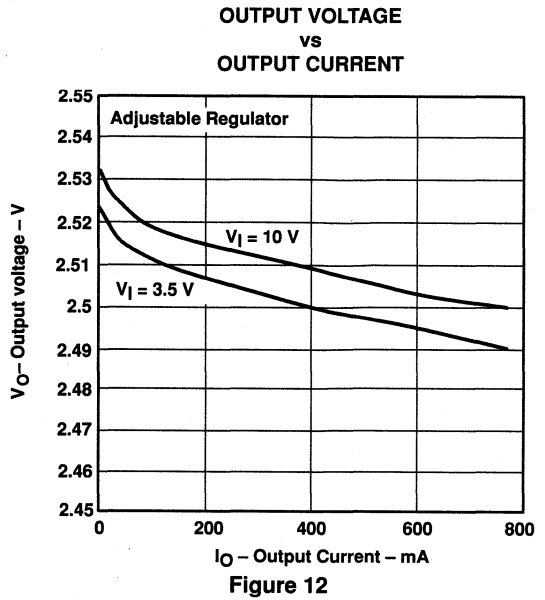
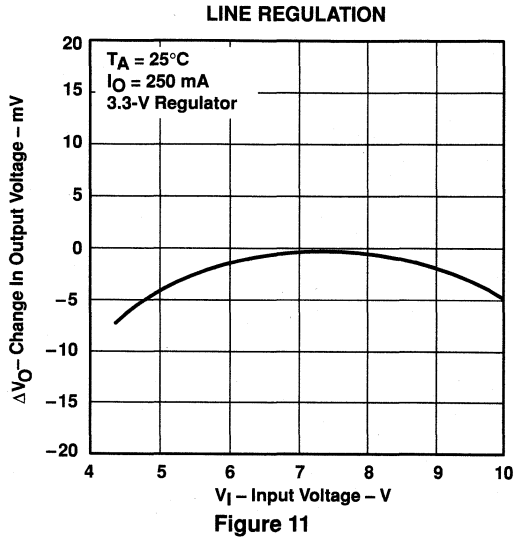


Figure 10

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS



TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE (EN)

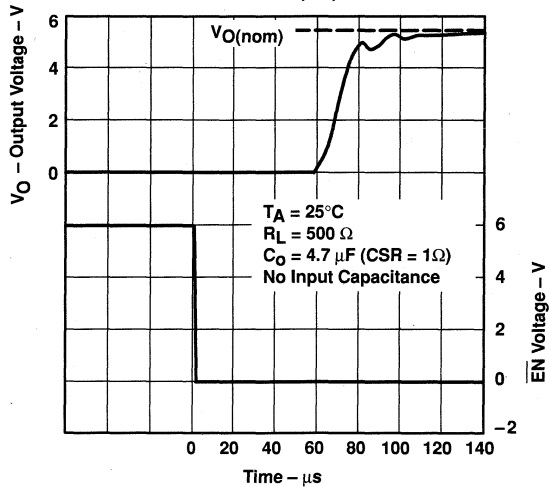


Figure 14

ADJUSTABLE REGULATOR LOAD TRANSIENT RESPONSE

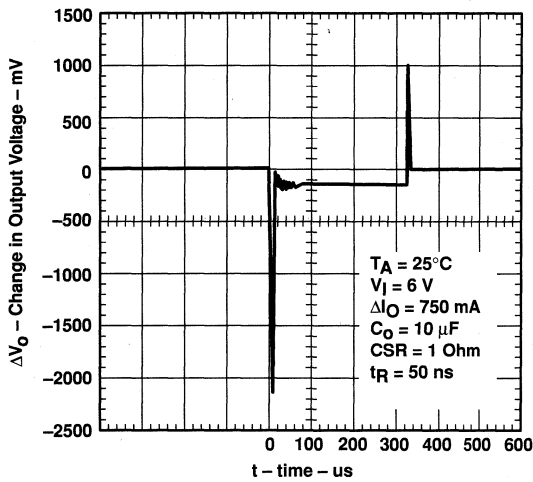


Figure 15

3.3-V REGULATOR LOAD TRANSIENT RESPONSE

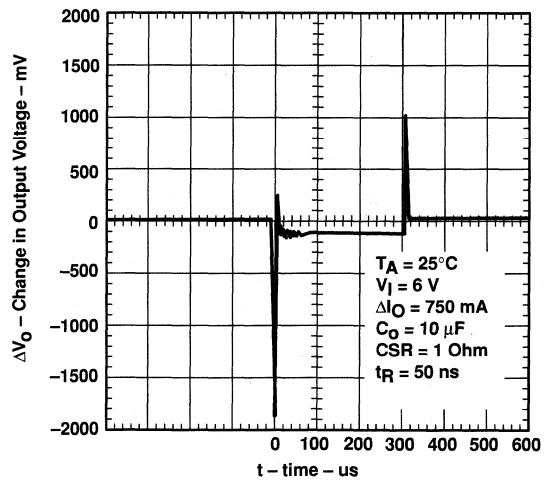


Figure 16



TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

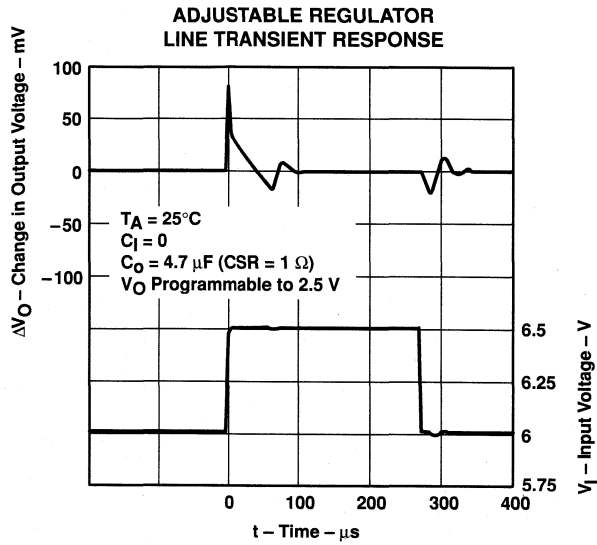


Figure 17

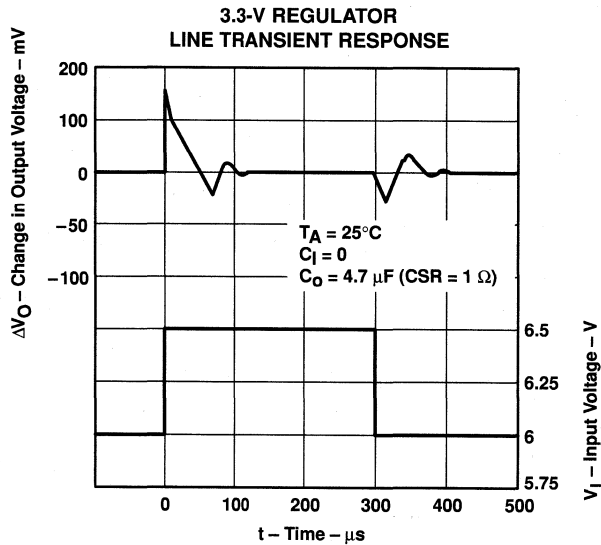


Figure 18

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**RIPPLE REJECTION
vs
FREQUENCY**

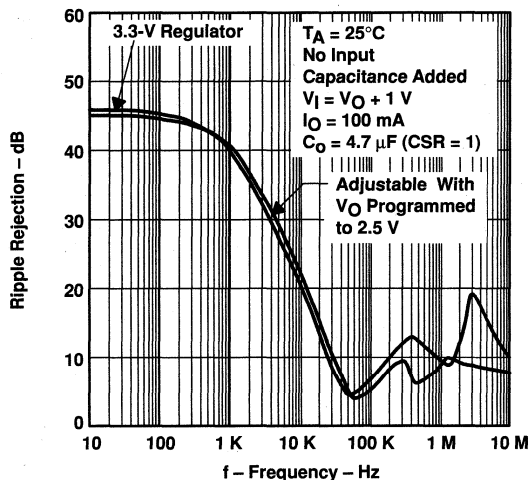


Figure 19

**OUTPUT SPECTRAL-NOISE DENSITY
vs
FREQUENCY**

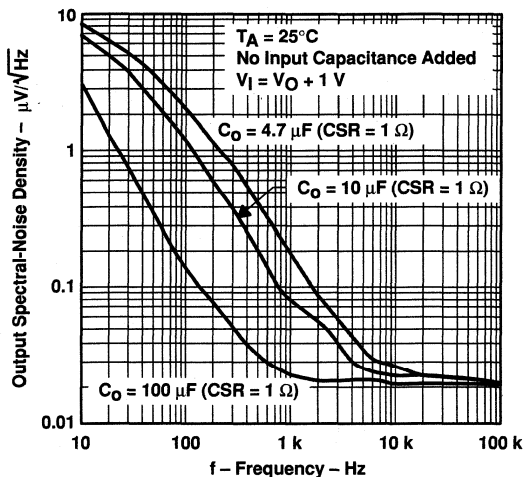


Figure 20

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
OUTPUT CURRENT**

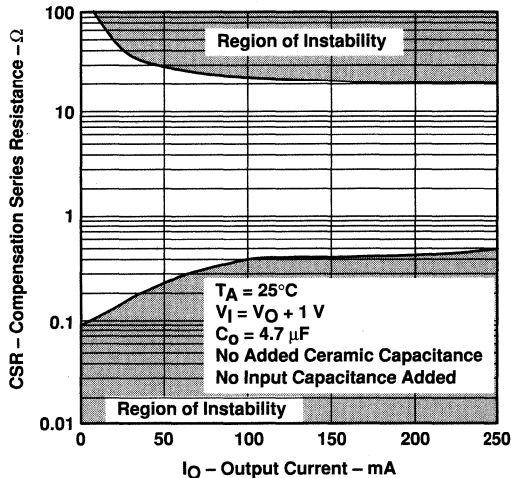


Figure 21

**TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
ADDED CERAMIC CAPACITANCE**

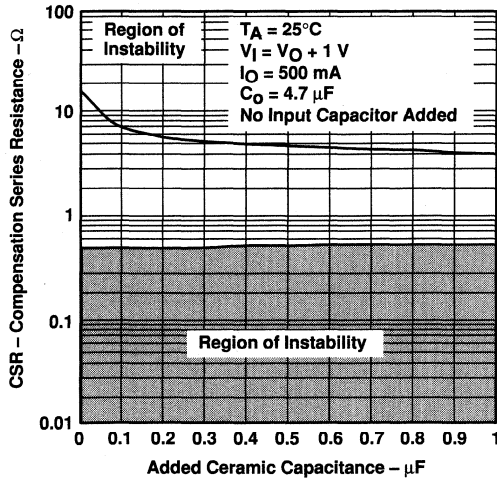


Figure 22



TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE

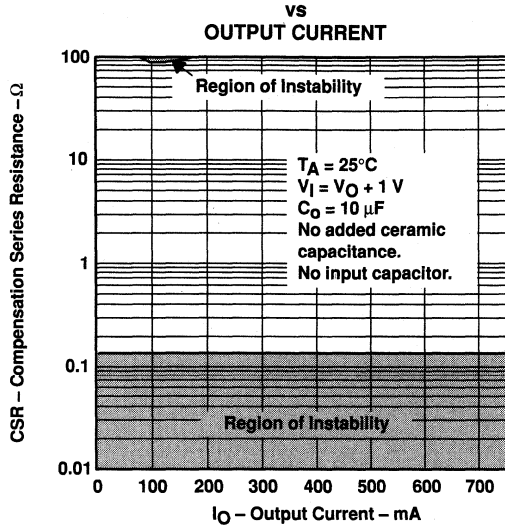


Figure 23

3.3-V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE

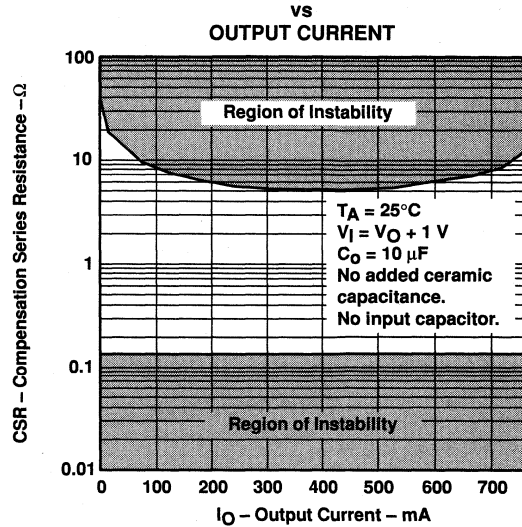


Figure 24

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE

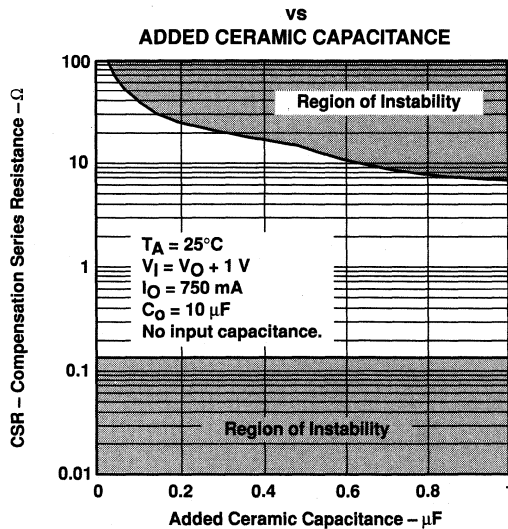


Figure 25

3.3-V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE

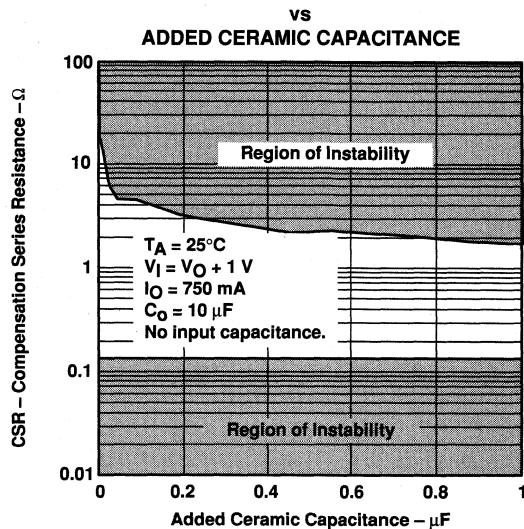


Figure 26

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**PASS-ELEMENT RESISTANCE
vs
INPUT VOLTAGE**

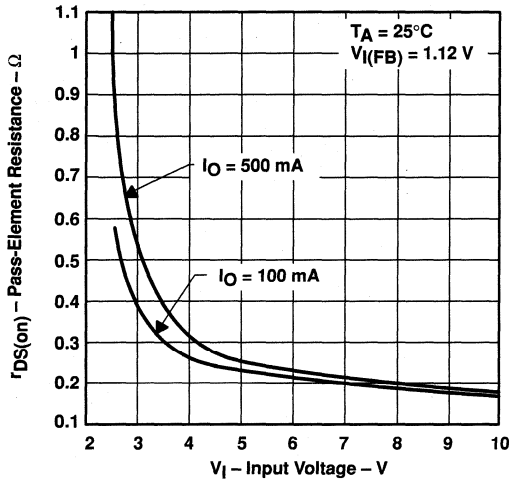


Figure 27

**MINIMUM INPUT VOLTAGE FOR VALID RESET
vs
FREE-AIR TEMPERATURE**

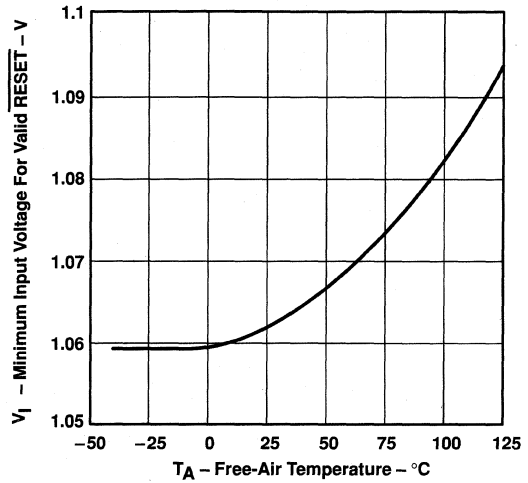


Figure 28

**NEGATIVE-GOING RESET THRESHOLD
vs
FREE-AIR TEMPERATURE**

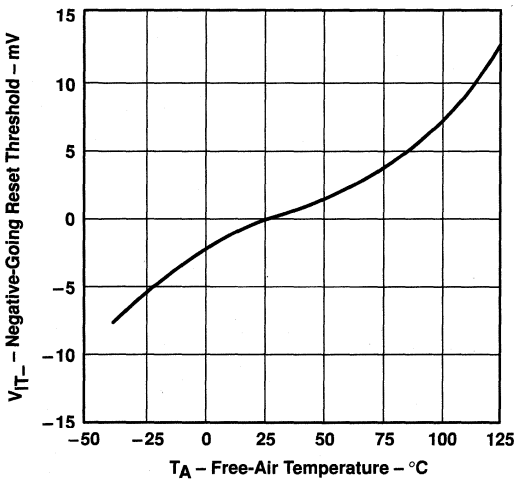


Figure 29

**RESET OUTPUT CURRENT
vs
INPUT VOLTAGE**

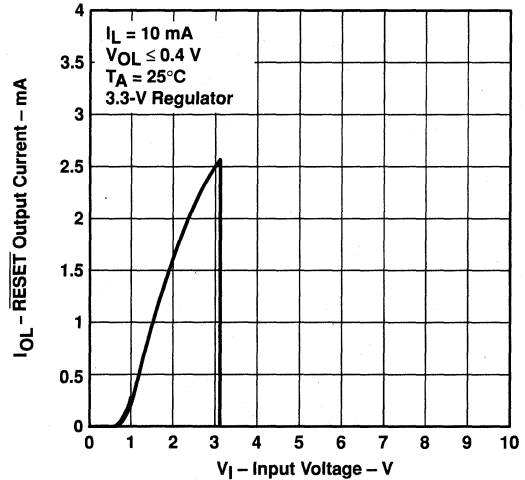


Figure 30



TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

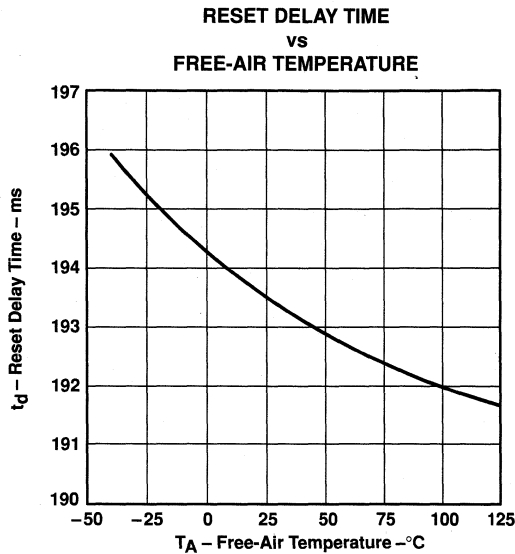


Figure 31

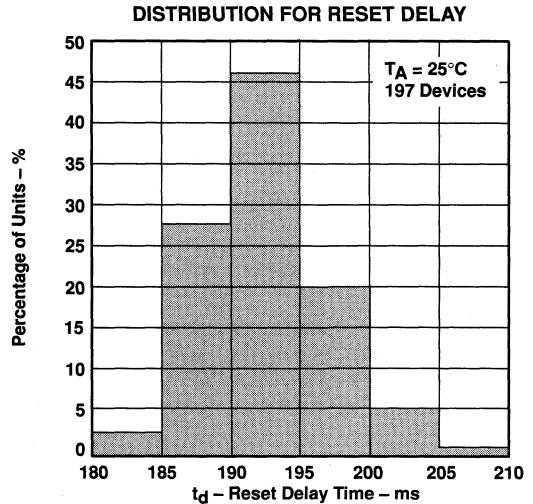


Figure 32

THERMAL INFORMATION

The TPS73HD3xx is packaged in a high-power dissipation downset lead frame for optimal power handling. With proper heat dissipation techniques, the full power output of these devices can be safely handled over the full temperature range. The Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package* (literature number SLMA002), goes into considerable detail into techniques for properly mounting this type of package for maximum thermal performance. A thermal conduction plane of approximately 3" x 3" will give a power dissipation level of 4.5 W.

Power dissipation within the device can be calculated with the following equation:

$$P_D = P_{IN} - P_{OUT} = V_I(I_{O1} + I_{O2}) - (V_{O1} \times I_{O1} + V_{O2} \times I_{O2})$$

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APPLICATION INFORMATION

thermal considerations

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	T _A < 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
PWP†	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWPS	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in² of copper area on a multilayer PCB is 24 mW/°C and 58 mW/°C respectively. Converting this to Θ_{JA} :

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

For 0 CFM :

$$= \frac{1}{0.0235}$$

$$= 42.6^{\circ}\text{C/W}$$

For 300 CFM :

$$= \frac{1}{0.0579}$$

$$= 17.3^{\circ}\text{C/W}$$

Given Θ_{JA} , the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPS73HD3xx is 150 °C.

$$T_{A \text{ Max}} = T_{J \text{ Max}} - (\Theta_{JA} \times P_D)$$

The maximum power dissipation limit is determined using the following equation:

$$T_{D(\text{max})} = \frac{T_{J \text{ max}} - T_A}{R_{\Theta JA}}$$

Where:

$T_{J \text{ max}}$ is the maximum allowable junction temperature

$R_{\Theta JA}$ is the thermal resistance junction-to-free-air for the package (i.e., 285°C/W for the 5-terminal SOT-23 package).

T_A is the free-air temperature

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible.



TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

Capitalizing upon the features of the TPS73xx family (low-dropout voltage, low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package has enabled the integration of the TPS73HD3xx dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 35 shows a typical dual-voltage DSP application.

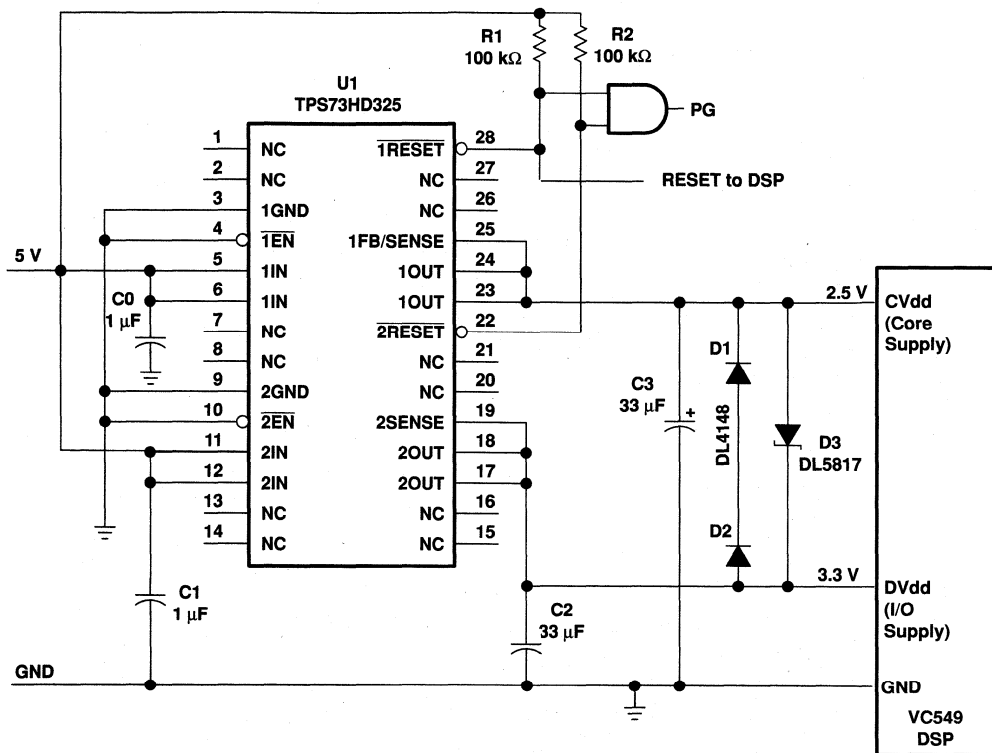


Figure 33. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents. Details of this type of design are shown in the application report, *Designing Power Supplies for TMS320VC549 DSP Systems*.

minimum load requirements

The TPS73HD3xx is stable even at zero load; no minimum load is required for operation.

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

SENSE connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μ F) improves load transient response and noise rejection when the TPS73HD3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS73HD3xx requires an output capacitor for stability. A low-ESR 10- μ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 44). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106M035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m Ω (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- μ F devices can be screened for ESR. Figures 23 through 28 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

Due to the reduced stability range available when using output capacitors smaller than 10 μ F, capacitors in this range are not recommended. Larger capacitors provide a wider range of stability and better load transient response. Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5- Ω to 1- Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 23 through 28), minimum ESR is not a problem when using 10- μ F or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73HD3xx. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF , 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF , 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF , 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF , 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF , 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF , 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF , 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF , full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF , 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF , 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF , 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF , 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF , 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF , 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

programming the adjustable LDO regulator output

Programming the adjustable regulator is done using an external resistor divider as shown in Figure 44. The equation governing the output voltage is:

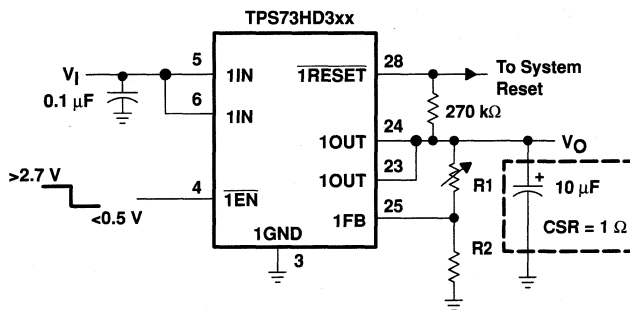
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

Where

V_{ref} = reference voltage, 1.182 V typ

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. A recommended value for R2 is 169 k Ω with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	RESET VOLTAGE	R1	R2	UNIT
1.5 V	-†	45.3	169	k Ω
1.8 V	-†	88.7	169	k Ω
2.5 V	2.37 V	191	169	k Ω
3.3 V	3.13 V	309	169	k Ω
3.6 V	3.42 V	348	169	k Ω
4 V	3.80 V	402	169	k Ω
5 V	4.75 V	549	169	k Ω
6.4 V	6.08 V	750	169	k Ω

† Non-operational below 1.9 V

Figure 34. TPS7301 Adjustable LDO Regulator Programming

TPS73HD301, TPS73HD318, TPS73HD325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

undervoltage supervisor function

The $\overline{\text{RESET}}$ outputs of the TPS73HD3xx initiate a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73HD3xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on, taking the $\overline{\text{RESET}}$ signal low.

At programmed output voltages below 1.9 V (on the adjustable regulator only) and on the 1.8 V regulator the reset function becomes unusable. With a minimum output voltage requirement for a valid $\overline{\text{RESET}}$ signal (over temperature) being 1.9 V, $\overline{\text{RESET}}$ will not operate reliably in this range.

On power up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typical) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output becomes inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pullup resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-} . Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typical) timeout period.

Transient loads or line pulses can also cause a reset to occur if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μs can cause a reset if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1- μs transient causes a reset when using an output capacitor with greater than 3.5 Ω of ESR. Note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1- μs transient must drop at least 500 mV below the threshold before tripping the reset circuit. A 2- μs transient trips $\overline{\text{RESET}}$ at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

NOTE:

$$V_{IT+} = V_{IT-} + \text{Hysteresis}$$

output noise

The TPS73HD3xx has very low output noise, with a spectral noise density $< 2 \mu\text{V}/\sqrt{\text{Hz}}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

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APPLICATION INFORMATION

regulator protection

The TPS73HD3xx PMOS-pass transistors have built-in back diodes that safely conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

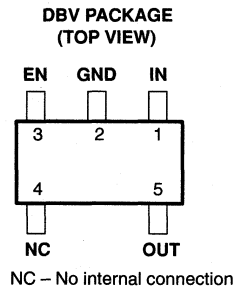
The TPS73HD3xx also features internal current limiting and thermal protection. During normal operation, the TPS73HD3xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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- 50-mA Low-Dropout Regulator
- Fixed Output Voltage Options: 5 V, 3.8 V, 3.3 V, 3.2 V, and 3 V
- Dropout Typically 120 mV at 50 mA
- Thermal Protection
- Less Than 1 μ A Quiescent Current in Shutdown
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 Package
- ESD Protection Verified to 1.5 kV Human Body Model (HBM) per MIL-STD-883C



description

The TPS760xx is a 50mA, low dropout (LDO) voltage regulator designed specifically for battery-powered applications. A proprietary BiCMOS fabrication process allows the TPS760xx to provide outstanding performance in all specifications critical to battery-powered operation.

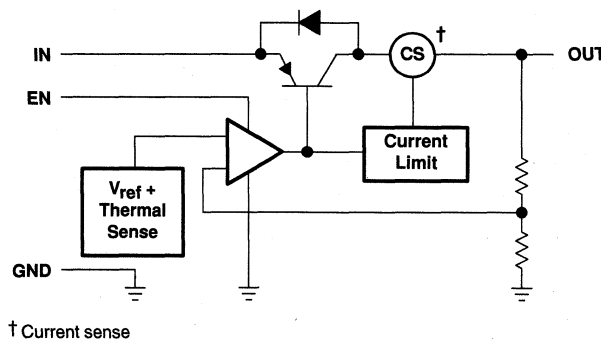
The TPS760xx is available in a space-saving SOT-23 package and operates over a junction temperature range of -40°C to 125°C .

AVAILABLE OPTIONS

T _J	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
-40°C to 125°C	3 V	SOT-23	TPS76030DBVR	PAGI
	3.2 V		TPS76032DBVR	PAOI
	3.3 V		TPS76033DBVR	PAHI
	3.8 V		TPS76038DBVR	PAJI
	5 V		TPS76050DBVR	PANI

NOTE: The DBV package is available taped and reeled only.

functional block diagram



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TPS76030, TPS76032, TPS76033, TPS76038, TPS76050

LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
IN	1	I	Input voltage
GND	2		Ground
EN	3	I	Enable input
NC	4		No connection
OUT	5	O	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I ‡	–0.3 V to 16 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Peak output current	internally limited
Continuous total dissipation	See dissipation table
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	1.5 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to device GND pin.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Input voltage, V_I	TPS76030	3.2		16	V
	TPS76032	3.4		16	V
	TPS76033	3.5		16	V
	TPS76038	4		16	V
	TPS76050	5.2		16	V
Continuous output current, I_O		0		50	mA
Operating junction temperature, T_J		–40		125	°C

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_O(\text{nom}) + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $EN = V_I$, $C_O = 2.2 \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	TPS76030	$T_J = 25^\circ\text{C}$	2.96	3	3.04	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 50 \text{ mA}$	2.92		3.04	V
		$1 \text{ mA} < I_O < 50 \text{ mA}$	2.91		3.07	V
	TPS76032	$T_J = 25^\circ\text{C}$	3.16	3.2	3.24	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 50 \text{ mA}$	3.13		3.24	V
		$1 \text{ mA} < I_O < 50 \text{ mA}$	3.1		3.3	V
	TPS76033	$T_J = 25^\circ\text{C}$	3.26	3.3	3.34	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 50 \text{ mA}$	3.23		3.34	V
		$1 \text{ mA} < I_O < 50 \text{ mA}$	3.2		3.4	V
	TPS76038	$T_J = 25^\circ\text{C}$	3.76	3.8	3.84	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 50 \text{ mA}$	3.73		3.84	V
		$1 \text{ mA} < I_O < 50 \text{ mA}$	3.7		3.9	V
	TPS76050	$T_J = 25^\circ\text{C}$	4.95	5	5.05	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 50 \text{ mA}$	4.91		5.05	V
		$1 \text{ mA} < I_O < 50 \text{ mA}$	4.89		5.1	V
$I_I(\text{standby})$	Standby current	$EN = 0 \text{ V}$			1	μA
Quiescent current (GND current)		$I_O = 0 \text{ mA}$, $T_J = 25^\circ\text{C}$		90	115	μA
		$I_O = 0 \text{ mA}$			130	
		$I_O = 1 \text{ mA}$, $T_J = 25^\circ\text{C}$		100	130	
		$I_O = 1 \text{ mA}$			170	
		$I_O = 10 \text{ mA}$, $T_J = 25^\circ\text{C}$		190	215	
		$I_O = 10 \text{ mA}$			460	
		$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		850	1100	
		$I_O = 50 \text{ mA}$			1200	
Input regulation	TPS76030	$4 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	mV
	TPS76032	$4.2 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
	TPS76033	$4.3 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
	TPS76038	$4.8 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
	TPS76050	$6 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
V_n	Output noise voltage	$BW = 300 \text{ Hz to } 50 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		190		μVrms
Ripple rejection		$f = 1 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		63		dB
Dropout voltage		$I_O = 0 \text{ mA}$, $T_J = 25^\circ\text{C}$		1	3	mV
		$I_O = 0 \text{ mA}$			5	
		$I_O = 1 \text{ mA}$, $T_J = 25^\circ\text{C}$		7	10	
		$I_O = 1 \text{ mA}$			15	
		$I_O = 10 \text{ mA}$, $T_J = 25^\circ\text{C}$		40	60	
		$I_O = 10 \text{ mA}$			90	
		$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		120	150	
Peak output current/current limit		$T_J = 25^\circ\text{C}$	100	125		mA



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050
LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $EN = V_I$, $C_O = 1\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High level enable input			2			V
Low level enable input					0.8	V
I_I	Input current (EN)	$EN = 0\text{ V}$	-1	0	1	μA
		$EN = V_I$		2.5	5	μA

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1, 2, 3
		vs Free-air temperature	4, 5, 6
	Ground current	vs Free-air temperature	7, 8, 9
	Output noise	vs Frequency	10
Z_O	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Free-air temperature	12
	Line transient response		13, 15
	Load transient response		14, 16



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050
 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

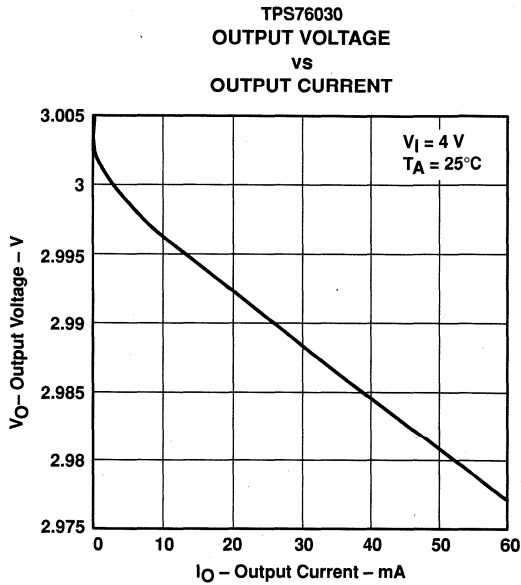


Figure 1

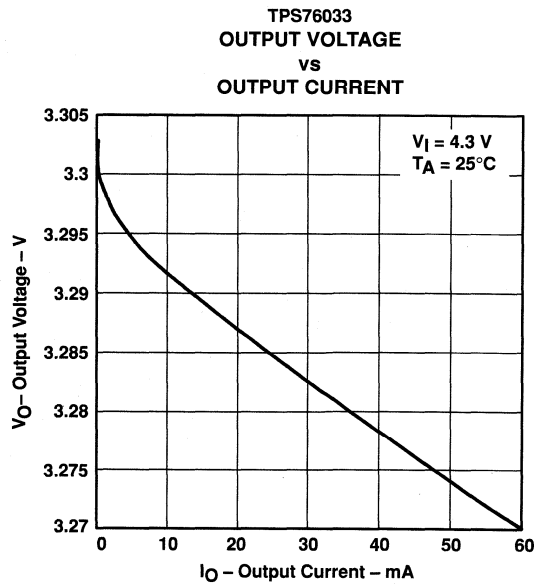


Figure 2

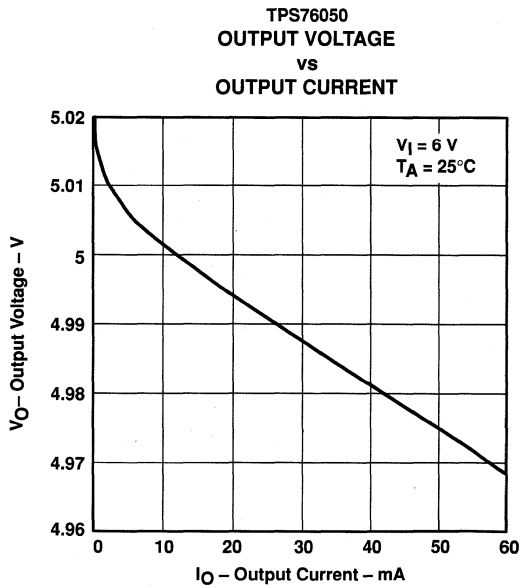


Figure 3

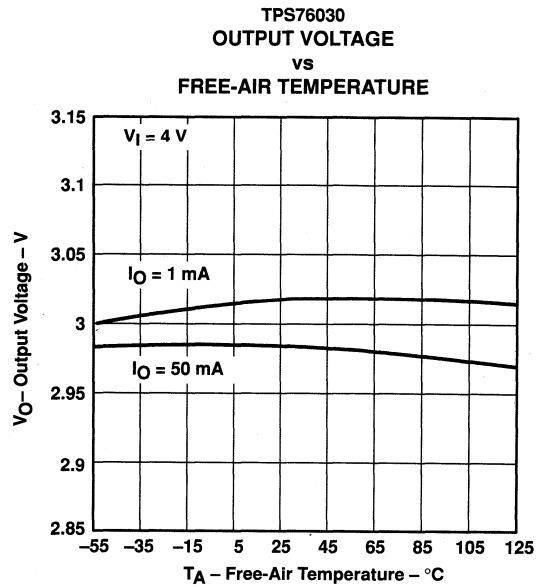


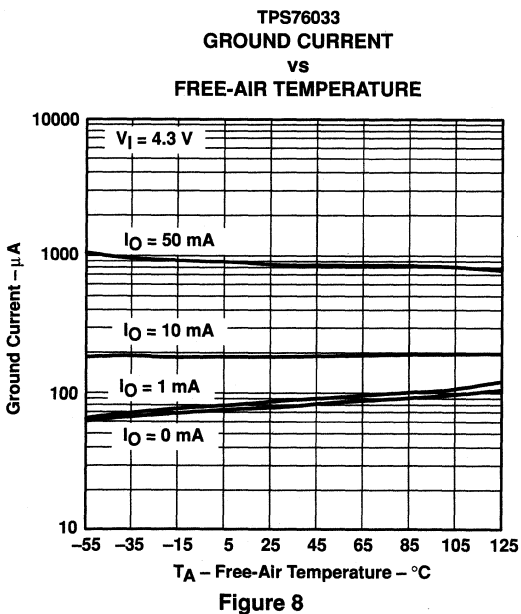
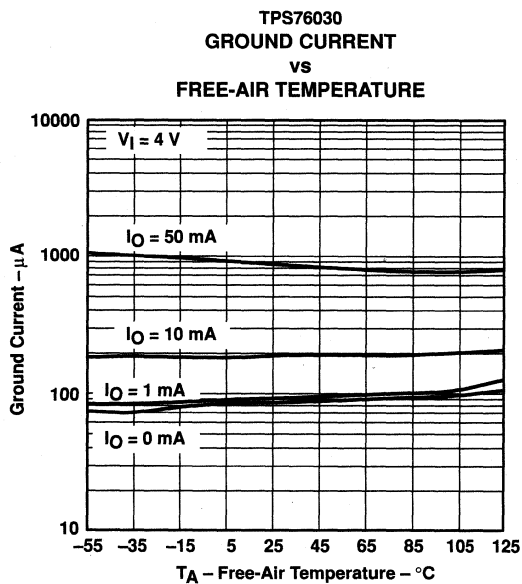
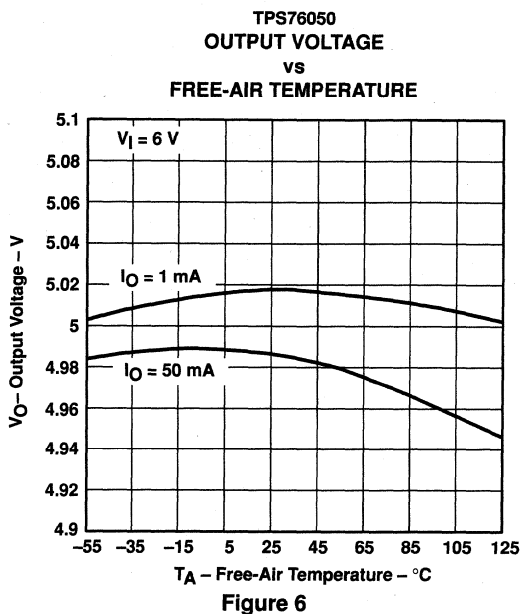
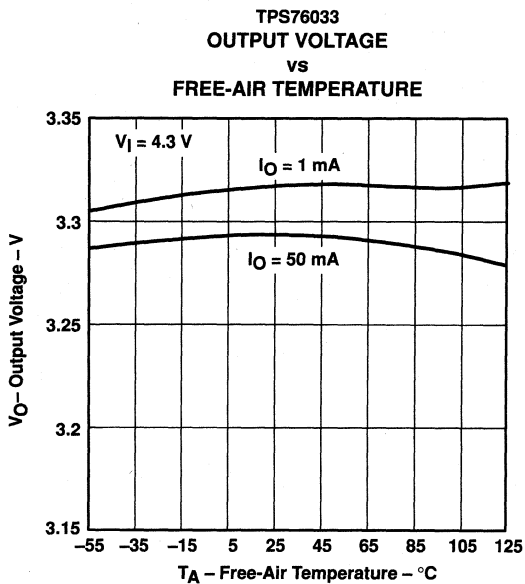
Figure 4

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050

LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050
 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

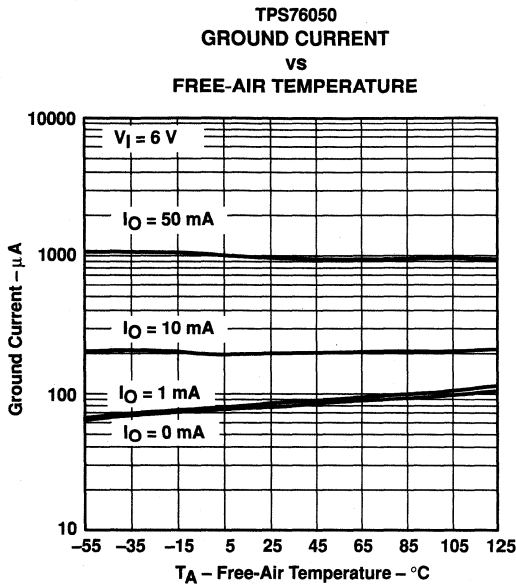


Figure 9

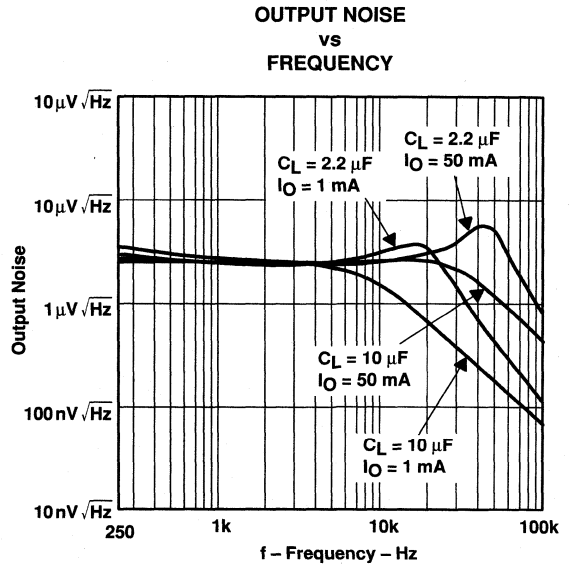


Figure 10

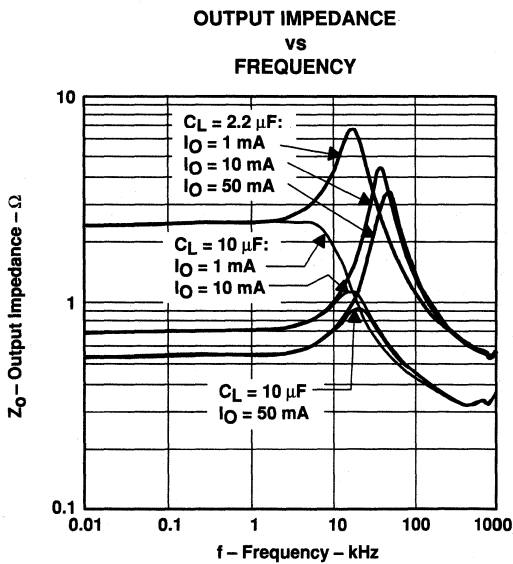


Figure 11

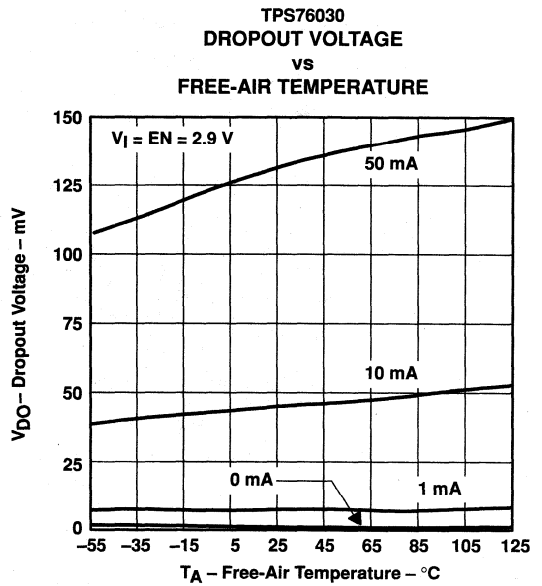


Figure 12

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050

LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

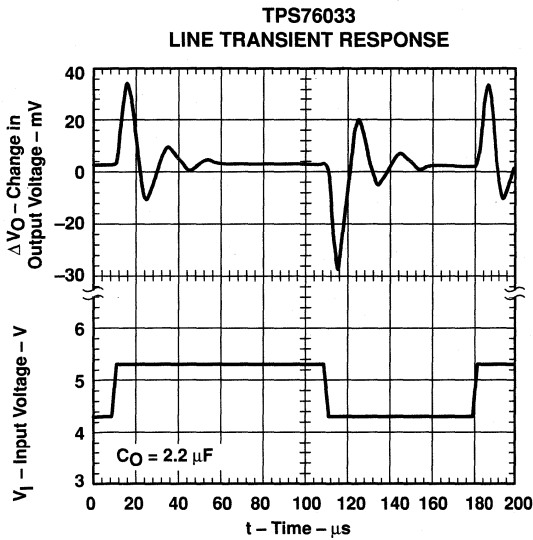


Figure 13

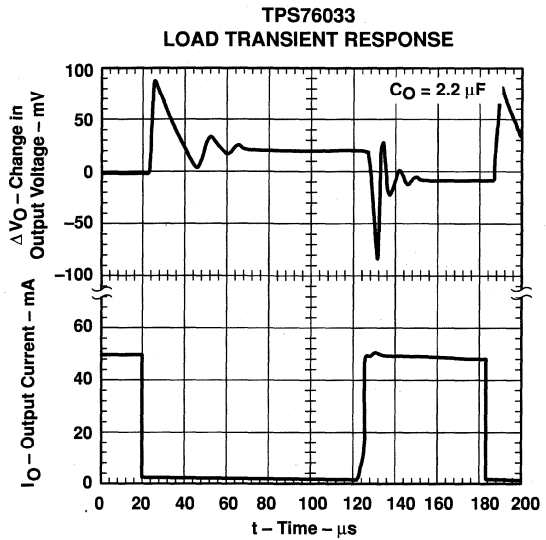


Figure 14

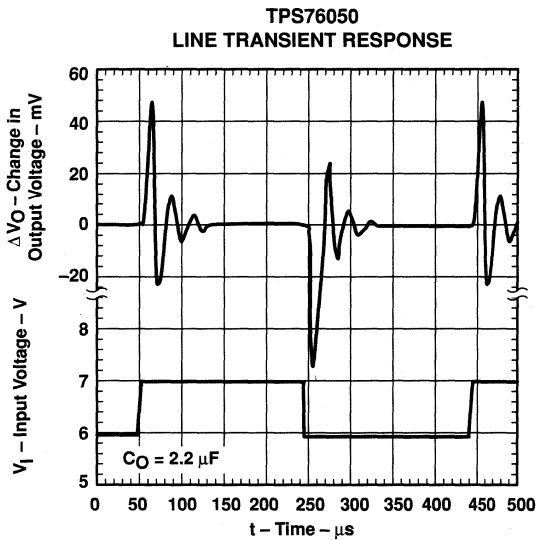


Figure 15

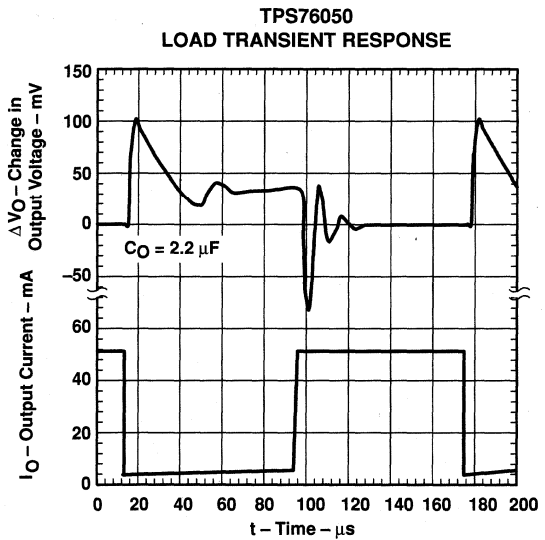


Figure 16

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

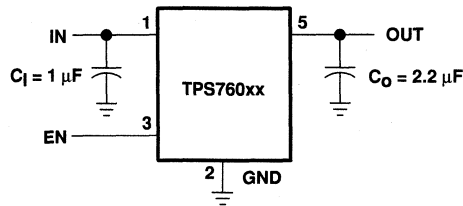


Figure 17. TPS760xx Typical Application

over current protection

The over current protection circuit forces the TPS760xx into a constant current output mode when the load is excessive or the output is shorted to ground. Normal operation resumes when the fault condition is removed. An overload or short circuit may also activate the over temperature protection if the fault condition persists.

over temperature protection

The thermal protection system shuts the TPS760xx down when the junction temperature exceeds 160°C. The device recovers and operates normally when the temperature drops below 150°C.

input capacitor

A 0.047 µF or larger ceramic decoupling capacitor with short leads connected between IN and GND is recommended. The decoupling capacitor may be omitted if there is a 1 µF or larger electrolytic capacitor connected between IN and GND and located reasonably close to the TPS760xx. However, the small ceramic device is desirable even when the larger capacitor is present, if there is a lot of high frequency noise present in the system.

output capacitor

Like all low dropout regulators, the TPS760xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 2.2 µF and the ESR (equivalent series resistance) must be between 0.1 Ω and 20 Ω. Capacitor values of 2.5-µF or larger are acceptable, provided the ESR is less than 20 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 2.2-µF surface-mount solid-tantalum capacitors, including devices from Sprague, Kemet, and Nichicon, meet the ESR requirements stated above. Multilayer ceramic capacitors should have minimum values of 2.5 µF over the full operating temperature range of the equipment.

enable (EN)

A logic zero on the enable input shuts the TPS760xx off and reduces the supply current to less than 1 µA. Pulling the enable input high causes normal operation to resume. If the enable feature is not used, EN should be connected to IN to keep the regulator on all of the time. The EN input must not be left floating.

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

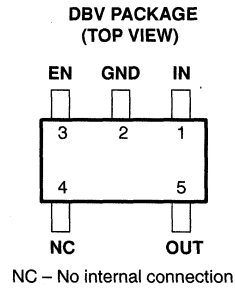
reverse current path

The power transistor used in the TPS760xx has an inherent diode connected between IN and OUT as shown in the functional block diagram. This diode conducts current from the OUT terminal to the IN terminal whenever IN is lower than OUT by a diode drop. This condition does not damage the TPS760xx, provided the current is limited to 100mA.

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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- 100-mA Low-Dropout Regulator
- Fixed Output Voltage Options: 5 V, 3.8 V, 3.3 V, 3.2 V, and 3 V
- Dropout Typically 170 mV at 100-mA
- Thermal Protection
- Less Than 1 μ A Quiescent Current in Shutdown
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package
- ESD Protection Verified to 1.5 KV Human Body Model (HBM) per MIL-STD-883C



description

The TPS761xx is a 100 mA, low dropout (LDO) voltage regulator designed specifically for battery-powered applications. A proprietary BiCMOS fabrication process allows the TPS761xx to provide outstanding performance in all specifications critical to battery-powered operation.

The TPS761xx is available in a space-saving SOT-23 (DBV) package and operates over a junction temperature range of -40°C to 125°C .

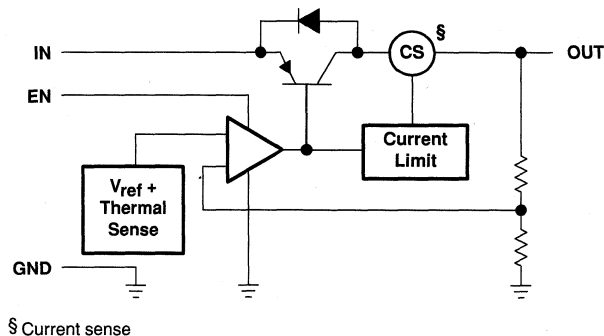
AVAILABLE OPTIONS

T _J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	3 V	SOT-23 (DBV)	TPS76130DBVR†	TPS76130DBVT‡	PAEI
	3.2 V		TPS76132DBVR†	TPS76132DBVT‡	PAFI
	3.3 V		TPS76133DBVR†	TPS76133DBVT‡	PAII
	3.8 V		TPS76138DBVR†	TPS76138DBVT‡	PAKI
	5 V		TPS76150DBVR†	TPS76150DBVT‡	PALI

† The DBVR passive indicates tape and reel of 3000 parts.

‡ The DBVT passive indicates tape and reel of 250 parts.

functional block diagram



TPS76130, TPS76132, TPS76133, TPS76138, TPS76150

LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	3	I	Enable input
GND	2		Ground
IN	1	I	Input voltage
NC	4		No connection
OUT	5	O	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1)	–0.3 V to 16 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Peak output current	internally limited
Continuous total dissipation	See Dissipation Rating Table
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	1.5 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to device GND pin.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Input voltage, V_I	TPS76130	3.35		16	V
	TPS76132	3.58		16	
	TPS76133	3.68		16	
	TPS76138	4.18		16	
	TPS76150	5.38		16	
Continuous output current, I_O		0		100	mA
Operating junction temperature, T_J		–40		125	°C

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $EN = V_I$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	TPS76130	$T_J = 25^\circ\text{C}$		2.96	3	3.04	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 100 \text{ mA}$		2.9		3.04	
		$1 \text{ mA} < I_O < 100 \text{ mA}$		2.89		3.07	
	TPS76132	$T_J = 25^\circ\text{C}$		3.16	3.2	3.24	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 100 \text{ mA}$		3.11		3.24	
		$1 \text{ mA} < I_O < 100 \text{ mA}$		3.08		3.3	
	TPS76133	$T_J = 25^\circ\text{C}$		3.26	3.3	3.34	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 100 \text{ mA}$		3.21		3.34	
		$1 \text{ mA} < I_O < 100 \text{ mA}$		3.18		3.4	
	TPS76138	$T_J = 25^\circ\text{C}$		3.76	3.8	3.84	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 100 \text{ mA}$		3.71		3.84	
		$1 \text{ mA} < I_O < 100 \text{ mA}$		3.68		3.9	
	TPS76150	$T_J = 25^\circ\text{C}$		4.95	5	5.05	V
		$T_J = 25^\circ\text{C}$, $1 \text{ mA} < I_O < 100 \text{ mA}$		4.88		5.05	
		$1 \text{ mA} < I_O < 100 \text{ mA}$		4.86		5.1	
$I_I(\text{standby})$	Standby current	$EN = 0 \text{ V}$				1	μA
	Quiescent current (GND current)	$I_O = 0 \text{ mA}$, $T_J = 25^\circ\text{C}$			90	115	μA
		$I_O = 0 \text{ mA}$				130	
		$I_O = 1 \text{ mA}$, $T_J = 25^\circ\text{C}$			100	130	
		$I_O = 1 \text{ mA}$				170	
		$I_O = 10 \text{ mA}$, $T_J = 25^\circ\text{C}$			190	220	
		$I_O = 10 \text{ mA}$				260	
		$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$			850	1100	
		$I_O = 50 \text{ mA}$				1200	
		$I_O = 100 \text{ mA}$, $T_J = 25^\circ\text{C}$			2600	3600	
		$I_O = 100 \text{ mA}$				4000	
	Input regulation	TPS76130	$4 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	mV
		TPS76132	$4.2 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
		TPS76133	$4.3 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
		TPS76138	$4.8 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
		TPS76150	$6 \text{ V} < V_I < 16$, $I_O = 1 \text{ mA}$		3	10	
V_n	Output noise voltage	$BW = 300 \text{ Hz to } 50 \text{ kHz}$	$C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	190			μVrms
	Ripple rejection	$f = 1 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		63			dB



TPS76130, TPS76132, TPS76133, TPS76138, TPS76150
LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(typ)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $EN = V_I$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage	$I_O = 0\text{ mA}$, $T_J = 25^\circ\text{C}$		1	3	mV
	$I_O = 0\text{ mA}$			5	
	$I_O = 1\text{ mA}$, $T_J = 25^\circ\text{C}$		7	10	
	$I_O = 1\text{ mA}$			15	
	$I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$		40	60	
	$I_O = 10\text{ mA}$			90	
	$I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$		120	150	
	$I_O = 50\text{ mA}$			180	
	$I_O = 100\text{ mA}$, $T_J = 25^\circ\text{C}$		170	240	
	$I_O = 100\text{ mA}$			280	
Peak output current/current limit	$T_J = 25^\circ\text{C}$	100	150		mA
High level enable input		2			V
Low level enable input				0.8	V
I_I Input current (EN)	$EN = 0\text{ V}$	-1	0	1	μA
	$EN = V_I$		2.5	5	

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1, 2, 3
		vs Free-air temperature	4, 5, 6
	Ground current	vs Free-air temperature	7, 8, 9
	Output noise	vs Frequency	10
Z_O	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Free-air temperature	12
		Line transient response	13, 15
		Load transient response	14, 16

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

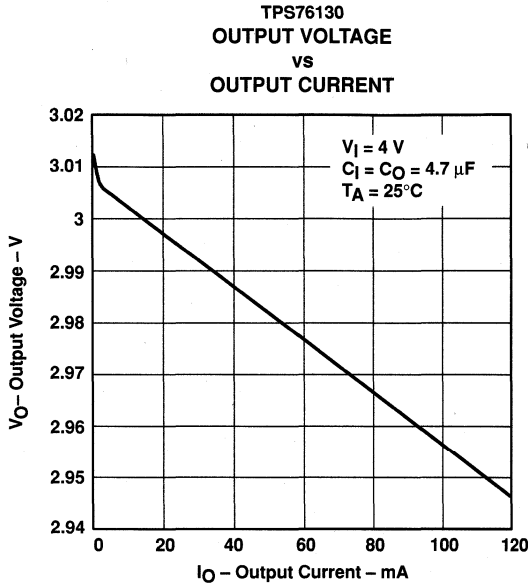


Figure 1

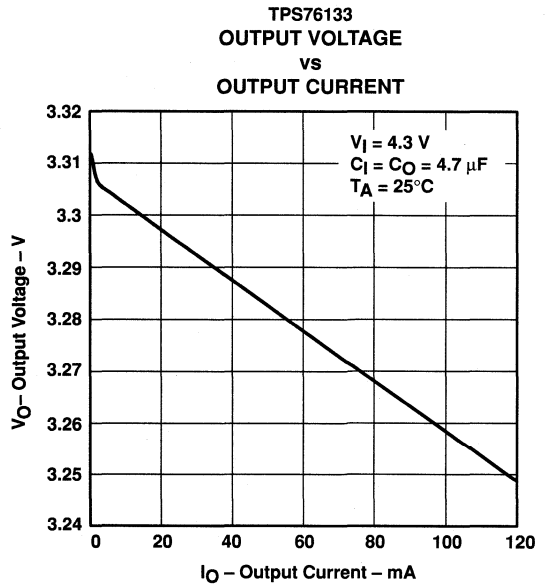


Figure 2

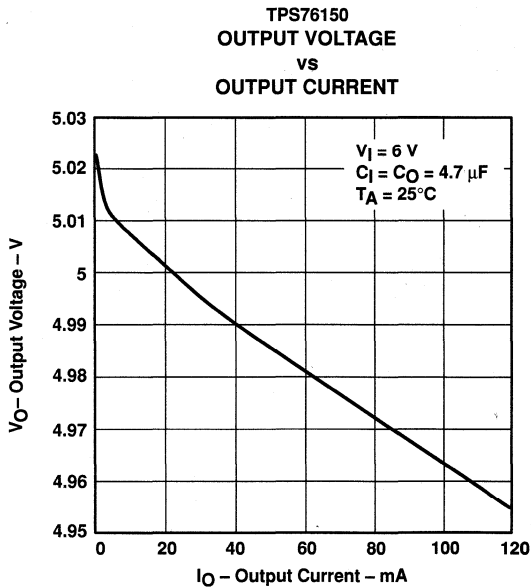


Figure 3

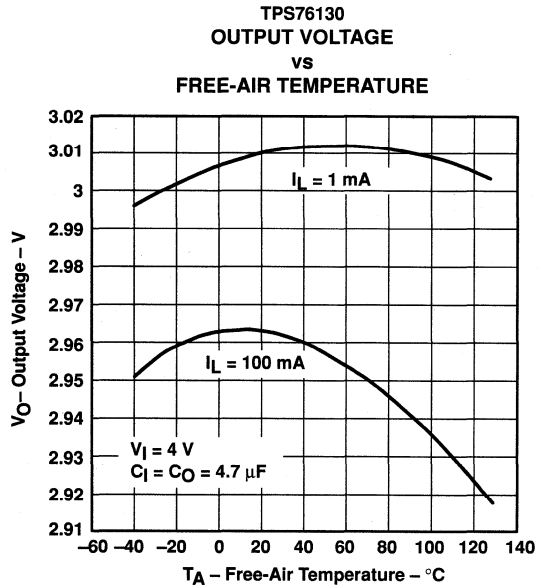


Figure 4

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

TPS76133
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

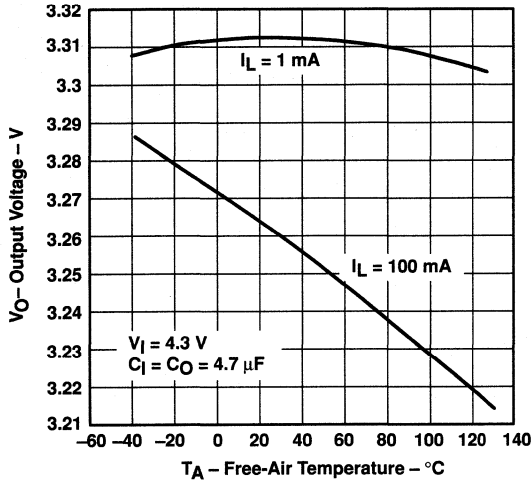


Figure 5

TPS76150
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

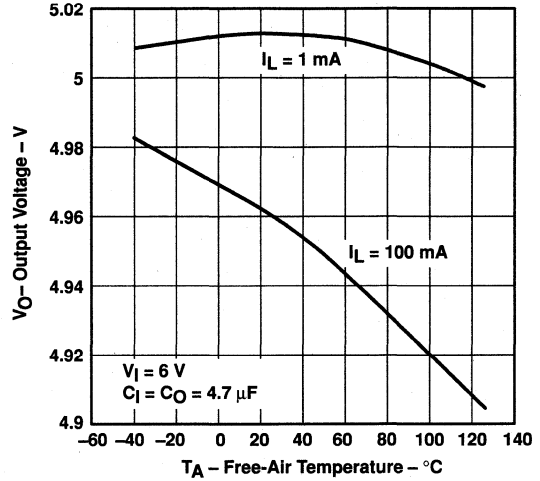


Figure 6

TPS76130
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

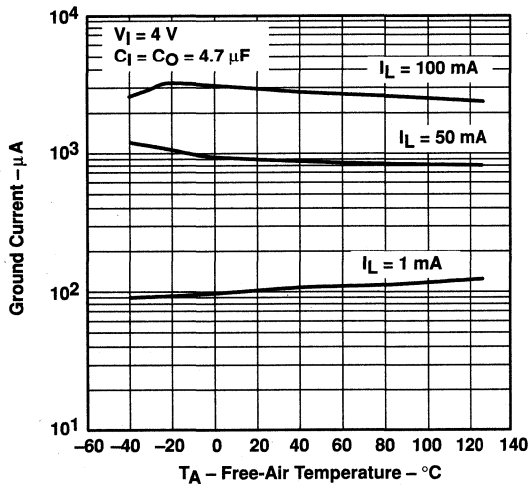


Figure 7

TPS76133
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

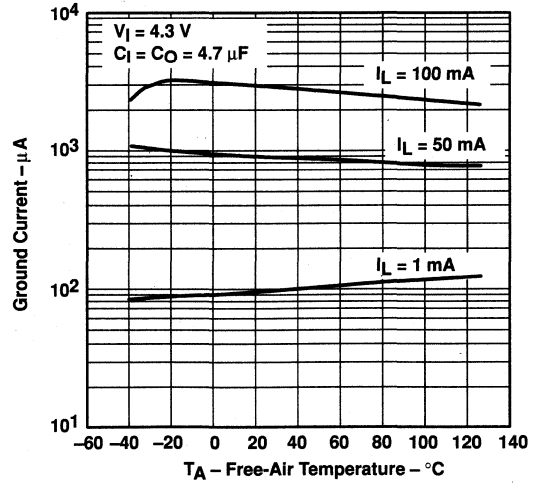


Figure 8

TYPICAL CHARACTERISTICS

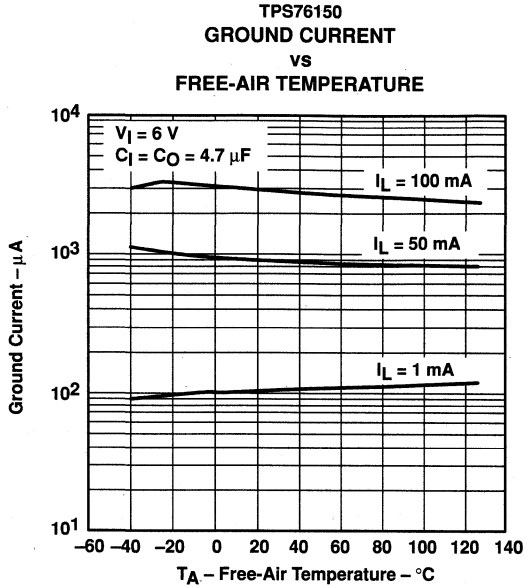


Figure 9

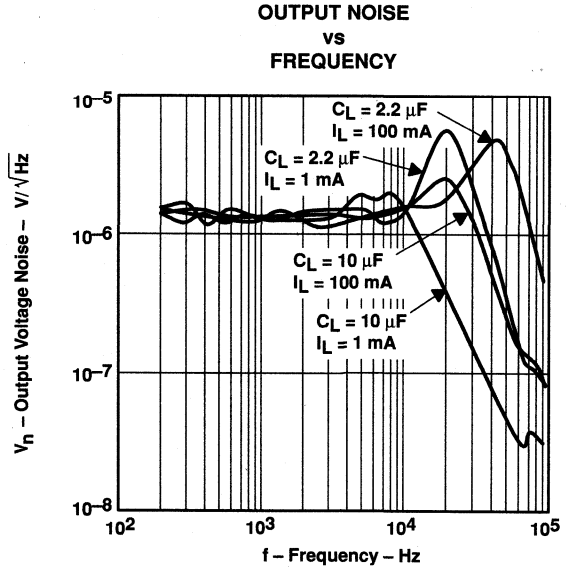


Figure 10

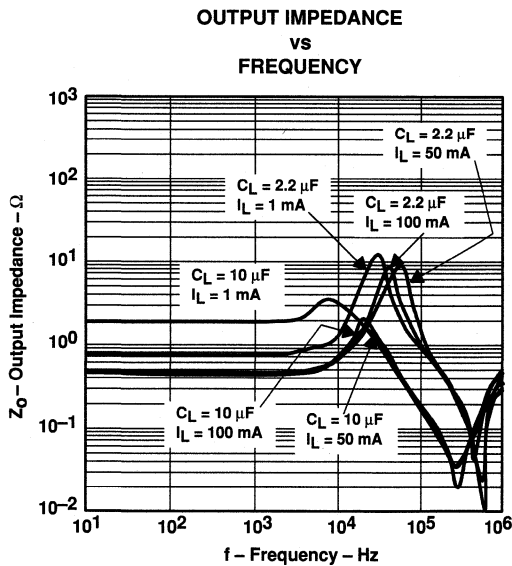


Figure 11

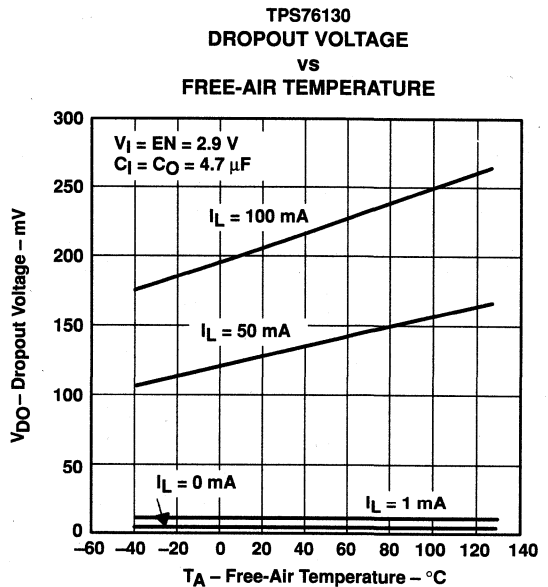


Figure 12

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

SLVS178A – DECEMBER 1998 – REVISED FEBRUARY 1999

TYPICAL CHARACTERISTICS

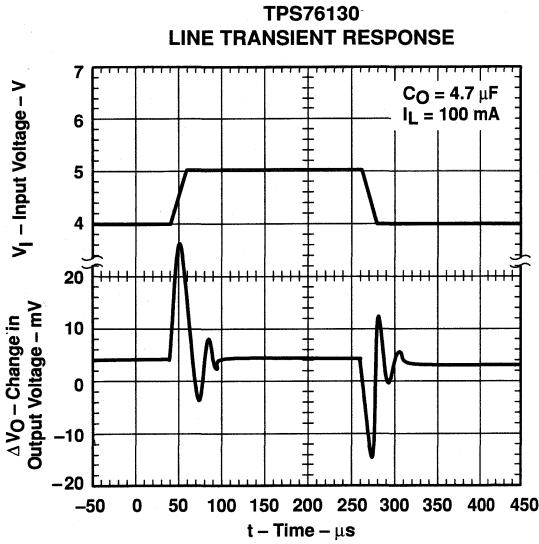


Figure 13

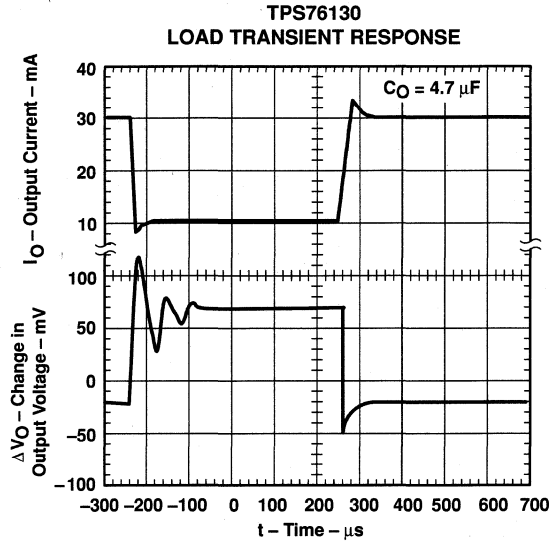


Figure 14

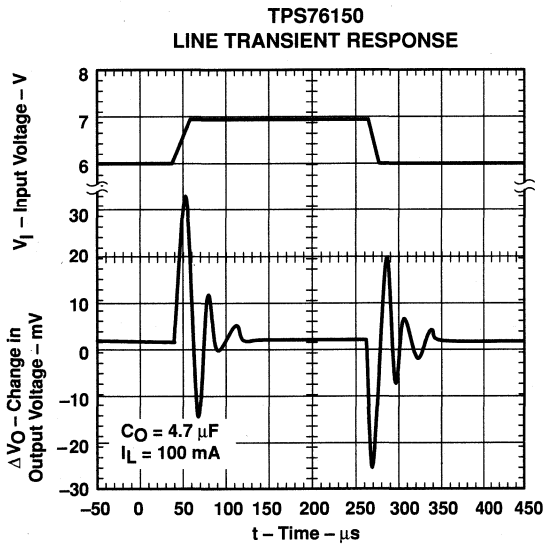


Figure 15

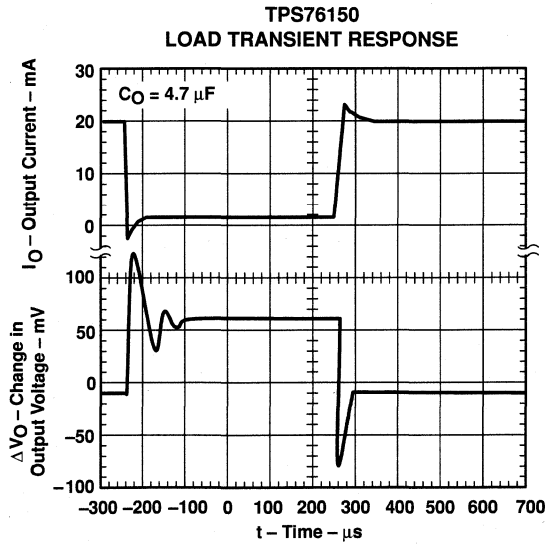


Figure 16

TPS76130, TPS76132, TPS76133, TPS76138, TPS76150 LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

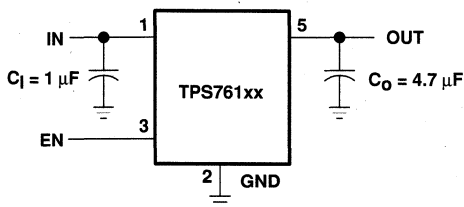


Figure 17. TPS761xx Typical Application

over current protection

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NOTE:

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The thermal protection system shuts the TPS761xx down when the junction temperature exceeds 160°C. The device recovers and operates normally when the temperature drops below 150°C.

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A 1- μ F or larger ceramic decoupling capacitor with short leads connected between IN and GND is recommended. The decoupling capacitor may be omitted if there is a 1 μ F or larger electrolytic capacitor connected between IN and GND and located reasonably close to the TPS761xx. However, the small ceramic device is desirable even when the larger capacitor is present, if there is a lot of high frequency noise present in the system.

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Like all low dropout regulators, the TPS761xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 μ F and the ESR (equivalent series resistance) must be between 0.1 Ω and 10 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7- μ F surface-mount solid-tantalum capacitors, including devices from Sprague, Kemet, and Nichicon, meet the ESR requirements stated above. Multilayer ceramic capacitors should have minimum values of 4.7 μ F over the full operating temperature range of the equipment.

enable (EN)

A logic zero on the enable input shuts the TPS761xx off and reduces the supply current to less than 1 μ A. Pulling the enable input high causes normal operation to resume. If the enable feature is not used, EN should be connected to IN to keep the regulator on all of the time. The EN input must not be left floating.

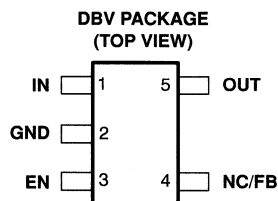
reverse current path

The power transistor used in the TPS761xx has an inherent diode connected between IN and OUT as shown in the functional block diagram. This diode conducts current from the OUT terminal to the IN terminal whenever IN is lower than OUT by a diode drop. This condition does not damage the TPS761xx provided the current is limited to 150 mA.

TPS76301, TPS76316, TPS76318, TPS76325, TPS76327 TPS76328, TPS76330, TPS76333, TPS76338, TPS76350 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS

SLVS181D – DECEMBER 1998 – REVISED JUNE 1999

- 150-mA Low-Dropout Regulator
- Output Voltage: 5 V, 3.8 V, 3.3 V, 3.0 V, 2.8 V, 2.7 V, 2.5 V, 1.8 V, 1.6 V and Variable
- Dropout Voltage, Typically 300 mV at 150 mA
- Thermal Protection
- Over Current Limitation
- Less Than 2- μ A Quiescent Current in Shutdown Mode
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



description

The TPS763xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in 5-terminal small outline integrated-circuit SOT-23 package, the TPS763xx series devices are ideal for cost-sensitive designs and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low—typically 300 mV at 150 mA of load current (TPS76333)—and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (140 μ A maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The TPS763xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A maximum at $T_J = 25^\circ\text{C}$. The TPS763xx is offered in 1.6-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 3.8-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.5 V to 6.5 V).

AVAILABLE OPTIONS

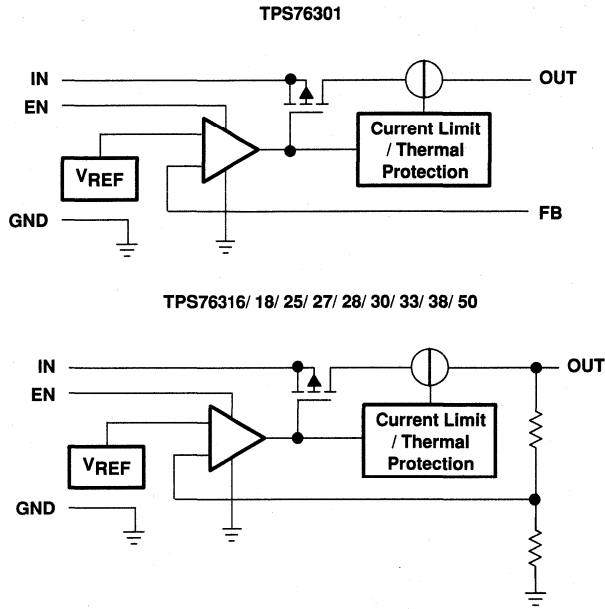
T_J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	Variable	SOT-23 (DBV)	TPS76301DBVT†	TPS76301DBVR‡	PAZI
	1.6 V		TPS76316DBVT†	TPS76316DBVR‡	PBHI
	1.8 V		TPS76318DBVT†	TPS76318DBVR‡	PBAI
	2.5 V		TPS76325DBVT†	TPS76325DBVR‡	PBBI
	2.7 V		TPS76327DBVT†	TPS76327DBVR‡	PBCI
	2.8 V		TPS76328DBVT†	TPS76328DBVR‡	PBDI
	3.0 V		TPS76330DBVT†	TPS76330DBVR‡	PBII
	3.3 V		TPS76333DBVT†	TPS76333DBVR‡	PBEI
	3.8 V		TPS76338DBVT†	TPS76338DBVR‡	PBFI
	5.0 V		TPS76350DBVT†	TPS76350DBVR‡	PBGI

† The DBVT passive indicates tape and reel of 250 parts.

‡ The DBVR passive indicates tape and reel of 3000 parts.

**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
 TPS76328, TPS76330, TPS76333, TPS76338, TPS76350
 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**
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functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
GND		Ground
EN	I	Enable input
FB	I	Feedback voltage (TPS76301 only)
IN	I	Input supply voltage
NC		No connection (fixed-voltage option only)
OUT	O	Regulated output voltage

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 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1)	–0.3 V to 10 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I †	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	–40		125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$



**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
 TPS76328, TPS76330, TPS76333, TPS76338, TPS76350
 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1\text{ V}$, $I_O = 1\text{ mA}$, $EN = IN$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _O	Output voltage	TPS76301	3.25 V > V _I ≥ 2.7 V, 2.5 V ≥ V _O ≥ 1.5 V,	I _O = 1 mA to 75 mA, T _J = 25°C	0.98 V _O	V _O	1.02 V _O	V
			3.25 V > V _I ≥ 2.7 V, 2.5 V ≥ V _O ≥ 1.5 V	I _O = 1 mA to 75 mA,	0.97 V _O	V _O	1.03 V _O	
			V _I ≥ 3.25 V, 5 V ≥ V _O ≥ 1.5 V	I _O = 1 mA to 100 mA, T _J = 25°C	0.98 V _O	V _O	1.02 V _O	
			V _I ≥ 3.25 V, 5 V ≥ V _O ≥ 1.5 V	I _O = 1 mA to 100 mA,	0.97 V _O	V _O	1.03 V _O	
			V _I ≥ 3.25 V, 5 V ≥ V _O ≥ 1.5 V	I _O = 1 mA to 150 mA, T _J = 25°C	0.975 V _O	V _O	1.025 V _O	
			V _I ≥ 3.25 V, 5 V ≥ V _O ≥ 1.5 V	I _O = 1 mA to 150 mA,	0.9625 V _O	V _O	1.0375 V _O	
		TPS76316	V _I = 2.7 V,	1 mA < I _O < 75 mA, T _J = 25°C	1.568	1.6	1.832	V
			V _I = 2.7 V,	1 mA < I _O < 75 mA	1.552	1.6	1.848	
			V _I = 3.25 V,	1 mA < I _O < 100 mA, T _J = 25°C	1.568	1.6	1.632	
			V _I = 3.25 V,	1 mA < I _O < 100 mA	1.552	1.6	1.648	
			V _I = 3.25 V,	1 mA < I _O < 150 mA, T _J = 25°C	1.560	1.6	1.640	
			V _I = 3.25 V,	1 mA < I _O < 150 mA	1.536	1.6	1.664	
		TPS76318	V _I = 2.7 V,	1 mA < I _O < 75 mA, T _J = 25°C	1.764	1.8	1.836	V
			V _I = 2.7 V,	1 mA < I _O < 75 mA	1.746	1.8	1.854	
			V _I = 3.25 V,	1 mA < I _O < 100 mA, T _J = 25°C	1.764	1.8	1.836	
			V _I = 3.25 V,	1 mA < I _O < 100 mA	1.746	1.8	1.854	
			V _I = 3.25 V,	1 mA < I _O < 150 mA, T _J = 25°C	1.755	1.8	1.845	
			V _I = 3.25 V,	1 mA < I _O < 150 mA	1.733	1.8	1.867	
		TPS76325	I _O = 1 mA to 100 mA, T _J = 25°C	2.45	2.5	2.55	V	
			I _O = 1 mA to 100 mA	2.425	2.5	2.575		
			I _O = 1 mA to 150 mA, T _J = 25°C	2.438	2.5	2.562		
			I _O = 1 mA to 150 mA	2.407	2.5	2.593		
		TPS76327	I _O = 1 mA to 100 mA, T _J = 25°C	2.646	2.7	2.754	V	
			I _O = 1 mA to 100 mA	2.619	2.7	2.781		
			I _O = 1 mA to 150 mA, T _J = 25°C	2.632	2.7	2.767		
			I _O = 1 mA to 150 mA	2.599	2.7	2.801		
		TPS76328	I _O = 1 mA to 100 mA, T _J = 25°C	2.744	2.8	2.856	V	
			I _O = 1 mA to 100 mA	2.716	2.8	2.884		
			I _O = 1 mA to 150 mA, T _J = 25°C	2.73	2.8	2.87		
		TPS76330	I _O = 1 mA to 100 mA, T _J = 25°C	2.94	3.0	3.06	V	
I _O = 1 mA to 100 mA	2.91		3.0	3.09				
I _O = 1 mA to 150 mA, T _J = 25°C	2.925		3.0	3.075				
I _O = 1 mA to 150 mA	2.888		3.0	3.112				



**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
TPS76328, TPS76330, TPS76333, TPS76338, TPS76350**
LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1\text{ V}$, $I_O = 1\text{ mA}$, $EN = IN$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

V_O	Output voltage	TPS76333	$I_O = 1\text{ mA to }100\text{ mA}$, $T_J = 25^\circ\text{C}$	3.234	3.3	3.366	V
			$I_O = 1\text{ mA to }100\text{ mA}$	3.201	3.3	3.399	
			$I_O = 1\text{ mA to }150\text{ mA}$, $T_J = 25^\circ\text{C}$	3.218	3.3	3.382	
			$I_O = 1\text{ mA to }150\text{ mA}$	3.177	3.3	3.423	
		TPS76338	$I_O = 1\text{ mA to }100\text{ mA}$, $T_J = 25^\circ\text{C}$	3.724	3.8	3.876	V
			$I_O = 1\text{ mA to }100\text{ mA}$	3.705	3.8	3.895	
			$I_O = 1\text{ mA to }150\text{ mA}$, $T_J = 25^\circ\text{C}$	3.686	3.8	3.914	
			$I_O = 1\text{ mA to }150\text{ mA}$	3.667	3.8	3.933	
		TPS76350	$I_O = 1\text{ mA to }100\text{ mA}$, $T_J = 25^\circ\text{C}$	4.875	5	5.125	V
			$I_O = 1\text{ mA to }100\text{ mA}$	4.825	5	5.175	
			$I_O = 1\text{ mA to }150\text{ mA}$, $T_J = 25^\circ\text{C}$	4.750	5	5.15	
			$I_O = 1\text{ mA to }150\text{ mA}$	4.80	5	5.20	
$I_{(Q)}$	Quiescent current (GND terminal current)	$I_O = 0\text{ to }150\text{ mA}$, $T_J = 25^\circ\text{C}$, See Note 2	85	100	μA		
		$I_O = 0\text{ to }150\text{ mA}$, See Note 2		140			
	Standby current	$EN < 0.5\text{ V}$, $T_J = 25^\circ\text{C}$	0.5	1	μA		
		$EN < 0.5\text{ V}$		2			
V_n	Output noise voltage	$BW = 300\text{ Hz to }50\text{ kHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, See Note 2	140		μV		
PSRR	Ripple rejection	$f = 1\text{ kHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, See Note 2	60		dB		
	Current limit	$T_J = 25^\circ\text{C}$, See Note 3	0.8	1.5	A		
	Output voltage line regulation ($\Delta V_O/V_O$) (see Note 4)	$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $V_I \geq 3.5\text{ V}$, $T_J = 25^\circ\text{C}$	0.04	0.07	%V		
		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $V_I \geq 3.5\text{ V}$		0.1			
V_{IH}	EN high level input	See Note 2	1.4	2	V		
V_{IL}	EN low level input	See Note 2	0.5	1.2			
I_I	EN input current	$EN = 0\text{ V}$	-0.01	-0.5	μA		
		$EN = IN$	-0.01	-0.5			

- NOTES: 2. Minimum I_N operating voltage is 2.7 V or $V_O(\text{typ}) + 1\text{ V}$, whichever is greater.
3. Test condition includes, output voltage $V_O = 0$ volts (for variable device FB is shorted to V_O), and pulse duration = 10ms.
4. If $V_O < 2.5\text{ V}$ and $V_{I\text{max}} = 10\text{ V}$, $V_{I\text{min}} = 3.5\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{I\text{max}} - 3.5\text{ V})}{100} \times 1000$$

If $V_O > 2.5\text{ V}$ and $V_{I\text{max}} = 10\text{ V}$, $V_{I\text{min}} = V_O + 1\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{I\text{max}} - (V_O + 1))}{100} \times 1000$$

**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
 TPS76328, TPS76330, TPS76333, TPS76338, TPS76350
 LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $EN = IN$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _{DO}	Dropout voltage	TPS76325	I _O = 0 mA, T _J = 25°C	0.2			mV	
			I _O = 1 mA, T _J = 25°C	3				
			I _O = 50 mA, T _J = 25°C	120	150			
			I _O = 50 mA		200			
			I _O = 75 mA, T _J = 25°C	180	225			
			I _O = 75 mA		300			
			I _O = 100 mA, T _J = 25°C	240	300			
			I _O = 100 mA		400			
			I _O = 150 mA, T _J = 25°C	360	450			
			I _O = 150 mA		600			
	Dropout voltage	TPS76333	TPS76333	I _O = 0 mA, T _J = 25°C	0.2			mV
				I _O = 1 mA, T _J = 25°C	3			
				I _O = 50 mA, T _J = 25°C	100	125		
				I _O = 50 mA		166		
				I _O = 75 mA, T _J = 25°C	150	188		
				I _O = 75 mA		250		
				I _O = 100 mA, T _J = 25°C	200	250		
				I _O = 100 mA		333		
				I _O = 150 mA, T _J = 25°C	300	375		
				I _O = 150 mA		500		
	Dropout voltage	TPS76350	TPS76350	I _O = 0 mA, T _J = 25°C	0.2			mV
				I _O = 1 mA, T _J = 25°C	2			
				I _O = 50 mA, T _J = 25°C	60	75		
				I _O = 50 mA		100		
				I _O = 75 mA, T _J = 25°C	90	113		
				I _O = 75 mA		150		
				I _O = 100 mA, T _J = 25°C	120	150		
I _O = 100 mA					200			
I _O = 150 mA, T _J = 25°C				180	225			
I _O = 150 mA					300			



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 TPS76328, TPS76330, TPS76333, TPS76338, TPS76350
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TYPICAL CHARACTERISTICS

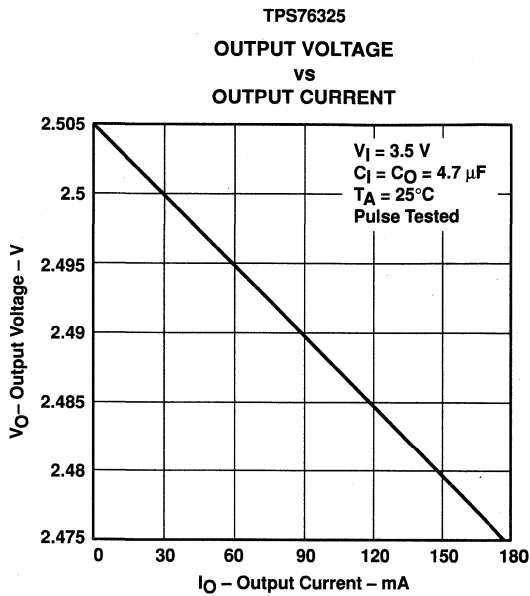


Figure 1

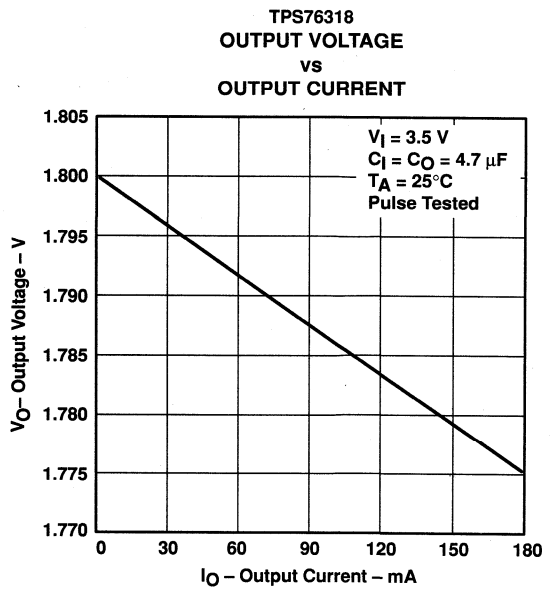


Figure 2

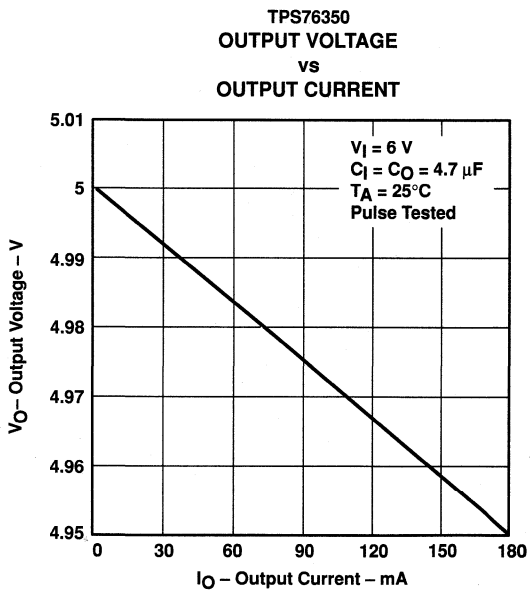


Figure 3

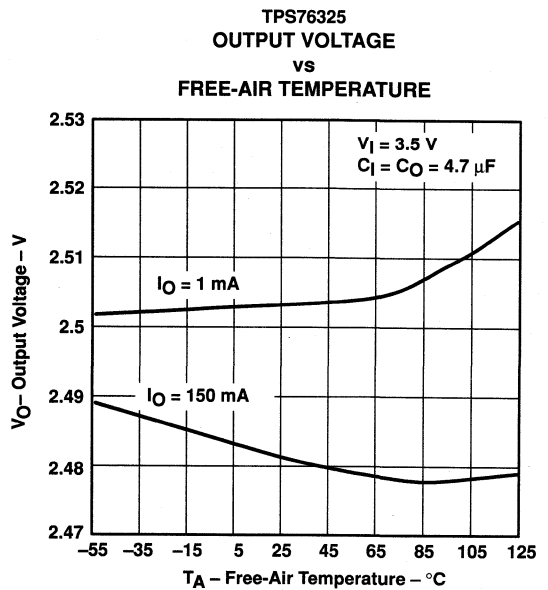


Figure 4

TYPICAL CHARACTERISTICS

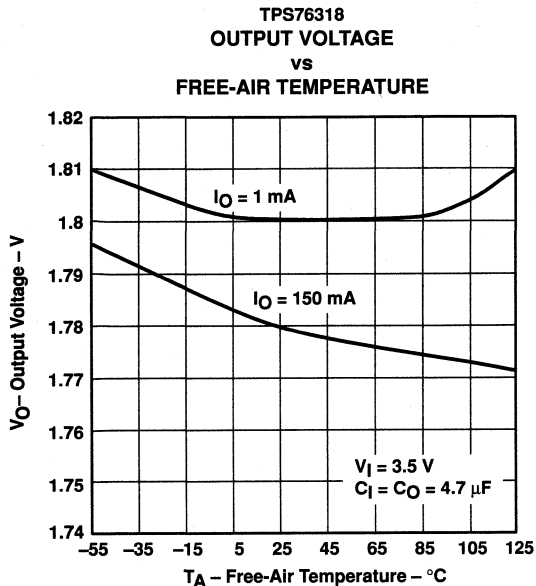


Figure 5

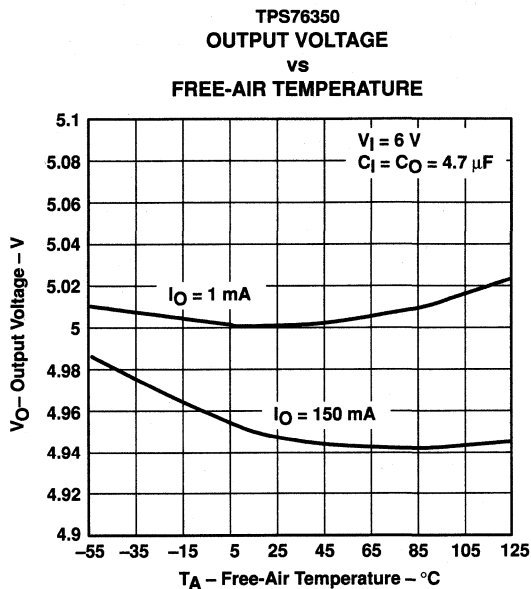


Figure 6

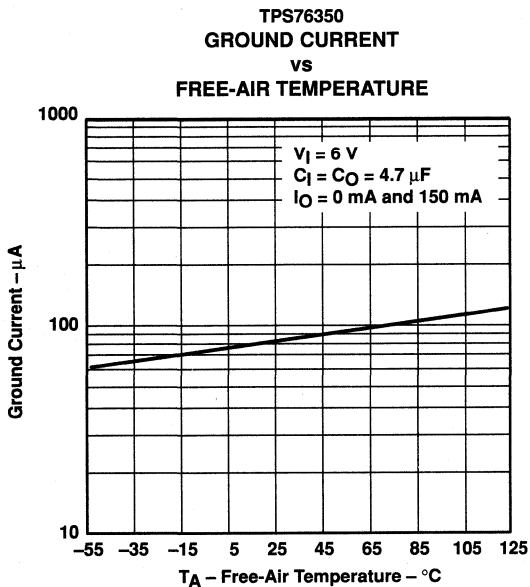


Figure 7

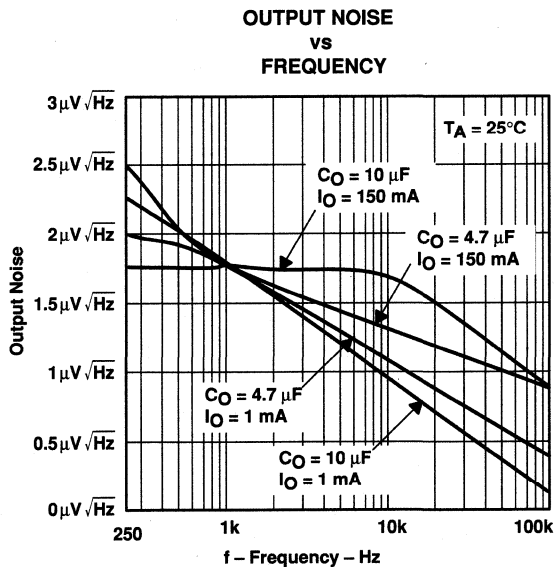


Figure 8

TYPICAL CHARACTERISTICS

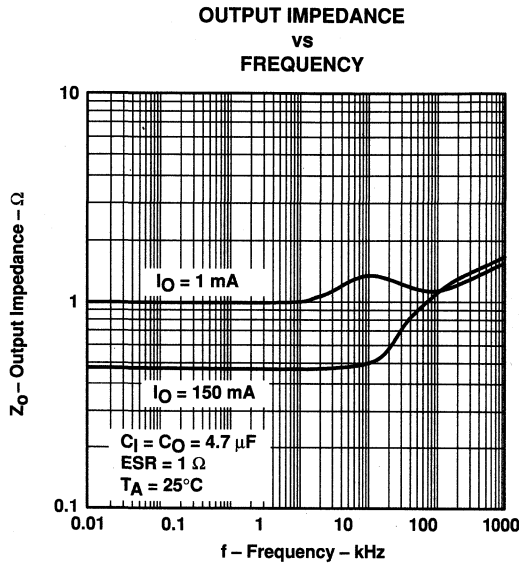


Figure 9

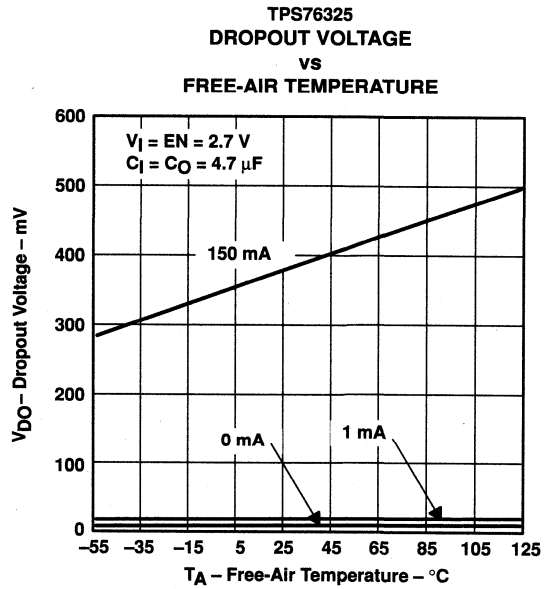


Figure 10

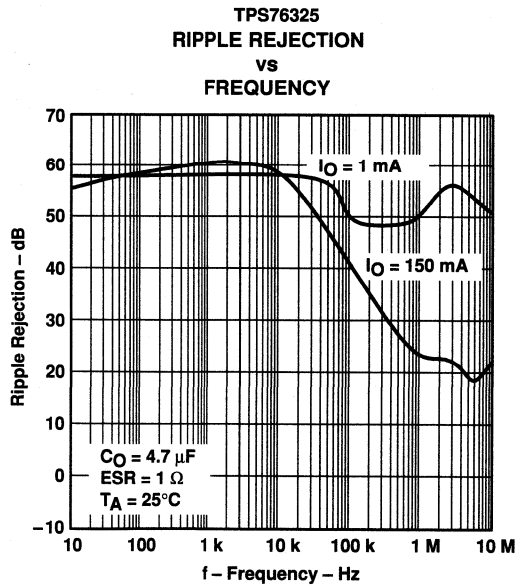


Figure 11

TYPICAL CHARACTERISTICS

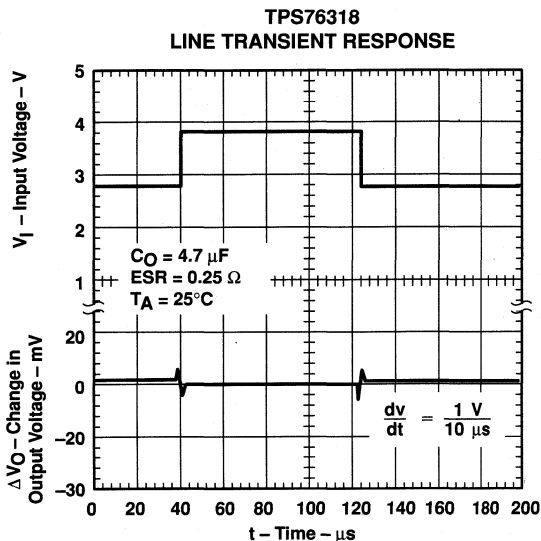


Figure 12

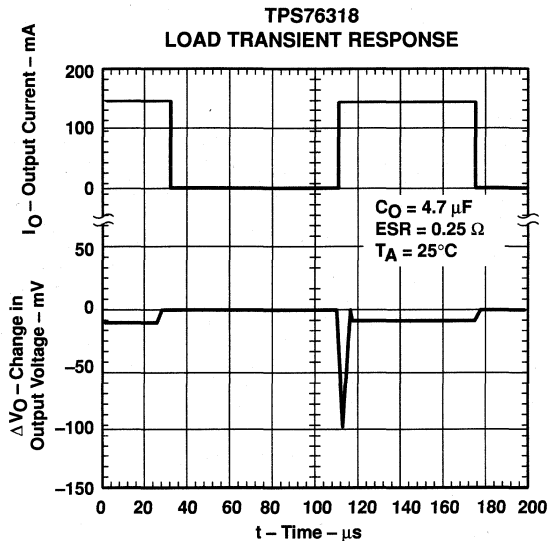


Figure 13

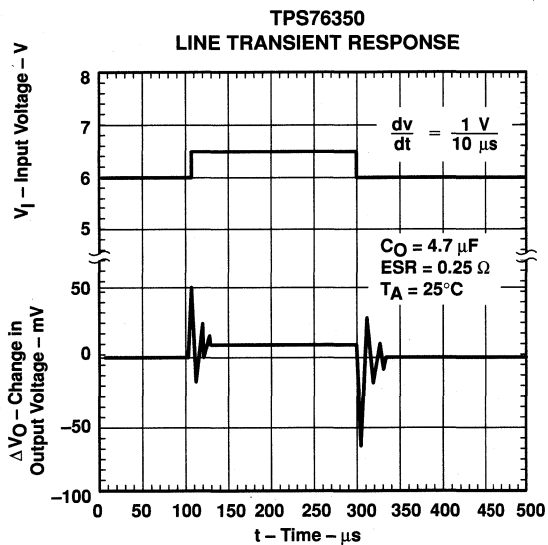


Figure 14

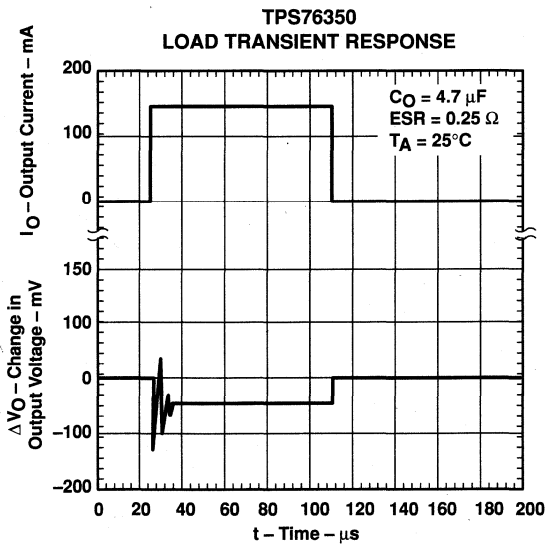


Figure 15

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 OUTPUT CURRENT

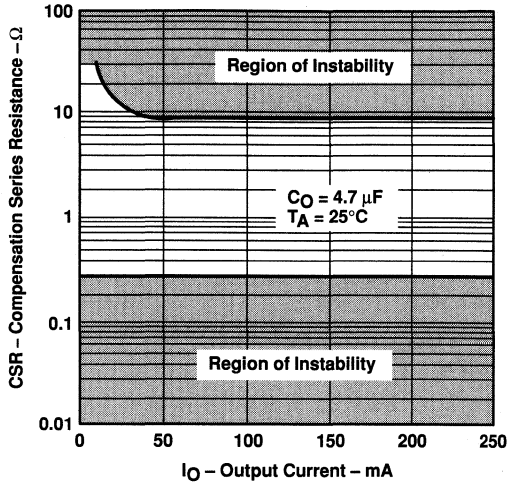


Figure 16

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 ADDED CERAMIC CAPACITANCE

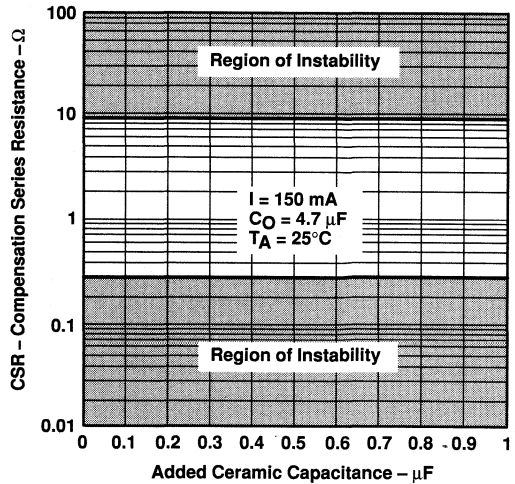


Figure 17

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 OUTPUT CURRENT

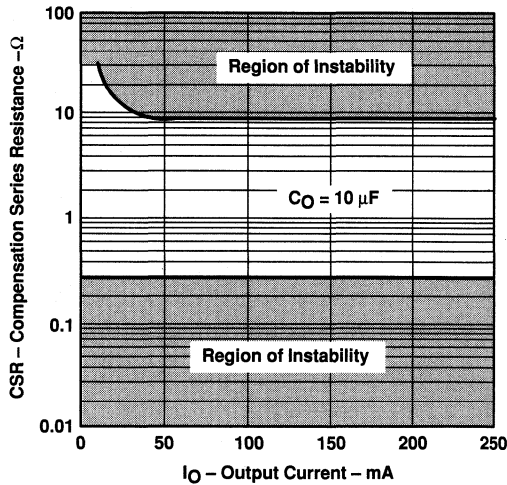


Figure 18

TYPICAL REGIONS OF STABILITY
 COMPENSATION SERIES RESISTANCE (CSR)[†]
 vs
 ADDED CERAMIC CAPACITANCE

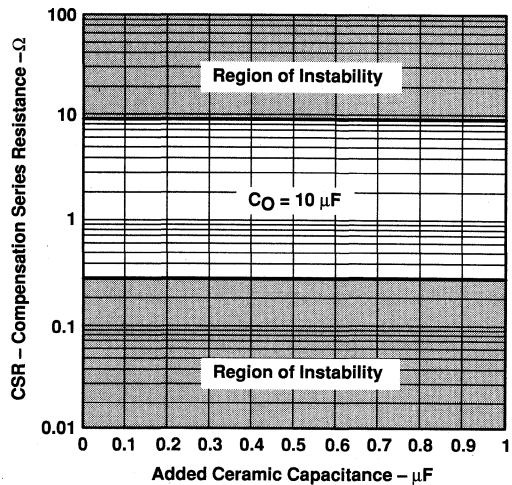


Figure 19

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
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LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

The TPS763xx low-dropout (LDO) regulators are new families of regulators which have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low quiescent current (140 μA), and an enable input to reduce supply currents to less than 2 μA when the regulator is turned off.

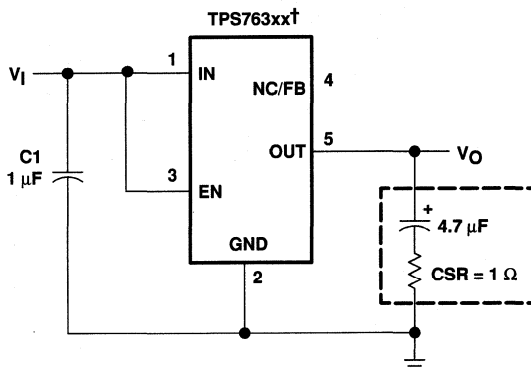
device operation

The TPS763xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS763xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic low on the enable input, EN shuts off the output and reduces the supply current to less than 2 μA . EN should be tied high in applications where the shutdown feature is not used.

A typical application circuit is shown in Figure 20.



† TPS76316, TPS76318, TPS76325, TPS76327, TPS76328, TPS7630, TPS76333, TPS76338, TPS76350 (fixed-voltage options).

Figure 20. Typical Application Circuit

**TPS76301, TPS76316, TPS76318, TPS76325, TPS76327
TPS76328, TPS76330, TPS76333, TPS76338, TPS76350
LOW-POWER 150-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047- μ F or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS763xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 μ F and the ESR (equivalent series resistance) must be between 0.2 Ω and 10 Ω . Capacitor values 4.7 μ F or larger are acceptable, provided the ESR is less than 10 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors should have minimum values of 1 μ F over the full operating temperature range of the equipment.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T494B475K016AS	KEMET	4.7 μ F	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 μ F	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 μ F	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 μ F	0.6 Ω	2.6 × 6.0 × 3.2

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.

output voltage programming

The output voltage of the TPS76301 adjustable regulator is programmed using an external resistor divider as shown in Figure 21. The output voltage is calculated using:

$$V_O = 0.995 \times V_{\text{ref}} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

$V_{\text{ref}} = 1.192$ V typ (the internal reference voltage)

0.995 is a constant used to center the load regulator (1%)

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 k Ω to set the divider current at 7 μ A and then calculate R1 using:

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APPLICATION INFORMATION

$$R1 = \left(\frac{V_O}{0.995 \times V_{ref}} - 1 \right) \times R2 \quad (2)$$

**OUTPUT VOLTAGE
 PROGRAMMING GUIDE**

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)†	
	R1	R2
2.5	187	169
3.3	301	169
3.6	348	169
4	402	169
5	549	169
6.45	750	169

† 1% values shown.

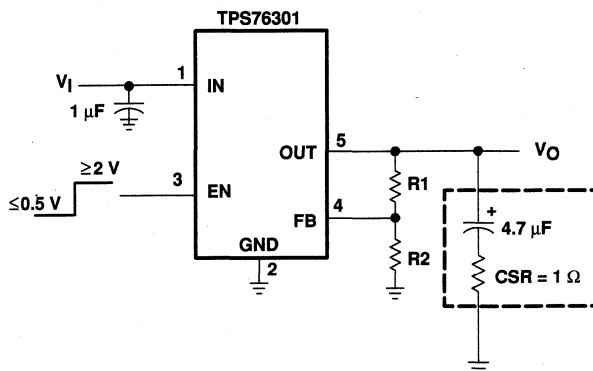


Figure 21. TPS76301 Adjustable LDO Regulator Programming

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible.

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regulator protection

The TPS763xx pass element has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

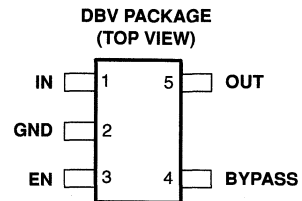
The TPS763xx also features internal current limiting and thermal protection. During normal operation, the TPS763xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, regulator operation resumes.



TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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- 150-mA Low Noise, Low-Dropout Regulator
- Output Voltage: 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V
- Output Noise Typically 50 μ V
- Quiescent Current Typically 85 μ A
- Dropout Voltage, Typically 300 mV at 150 mA
- Thermal Protection
- Over Current Limitation
- Less Than 2- μ A Quiescent Current in Shutdown Mode
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



description

The TPS764xx family of low-dropout (LDO) voltage regulators offers the benefits of a low noise, low-dropout voltage, low-power operation, and miniaturized package. Additionally, they feature low quiescent current when compared to conventional LDO regulators. Offered in 5-terminal small outline integrated-circuit SOT-23 package, the TPS764xx series devices are ideal for low-noise applications, cost-sensitive designs and applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low—typically 300 mV at 150 mA of load current (TPS76433)—and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (140 μ A maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The TPS764xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A maximum at $T_J = 25^\circ\text{C}$. The TPS764xx is offered in 2.5-V, 2.7-V, 2.8-V, 3.0-V, and 3.3-V fixed-voltages.

AVAILABLE OPTIONS

T_J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	2.5 V	SOT-23 (DBV)	TPS76425DBVT†	TPS76425DBVR‡	PBJI
	2.7 V		TPS76427DBVT†	TPS76427DBVR‡	PBKI
	2.8 V		TPS76428DBVT†	TPS76428DBVR‡	PCEI
	3.0 V		TPS76430DBVT†	TPS76430DBVR‡	PBLI
	3.3 V		TPS76433DBVT†	TPS76433DBVR‡	PBMI

† The DBVT passive indicates tape and reel of 250 parts.

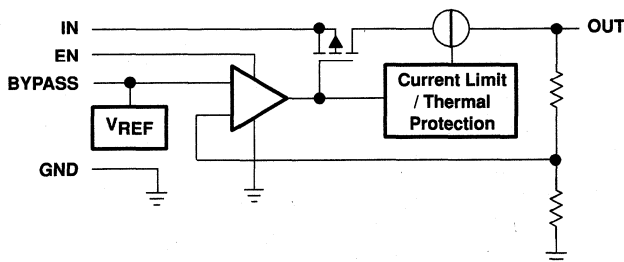
‡ The DBVR passive indicates tape and reel of 3000 parts.

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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functional block diagram

TPS76425/ 27/ 28/ 30/ 33



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
GND		Ground
EN	I	Enable input
BYPASS		Output bypass capacitor
IN	I	Input supply voltage
OUT	O	Regulated output voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1)	-0.3 V to 10 V
Voltage range at EN	-0.3 V to $V_I + 0.3$ V
Voltage on OUT,	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I †	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	-40		125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$



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LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $EN = IN$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76425	$I_O = 1 \text{ mA to } 100 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.45	2.5	2.55	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.425	2.5	2.575	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.438	2.5	2.562	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.407	2.5	2.593	
		TPS76427	$I_O = 1 \text{ mA to } 100 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.646	2.7	2.754	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.619	2.7	2.781	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.632	2.7	2.768	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.598	2.7	2.8013	
		TPS76428	$I_O = 1 \text{ mA to } 100 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.744	2.8	2.856	V
			$I_O = 1 \text{ mA to } 150 \text{ mA}$,	2.73	2.8	2.870	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.716	2.8	2.884	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.695	2.8	2.905	
		TPS76430	$I_O = 1 \text{ mA to } 100 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.94	3.0	3.06	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.925	3.0	3.075	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	2.91	3.0	3.090	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.887	3.0	3.112	
TPS76433	$I_O = 1 \text{ mA to } 100 \text{ mA}$, $T_J = 25^\circ\text{C}$	3.234	3.3	3.366	V		
	$I_O = 1 \text{ mA to } 100 \text{ mA}$	3.201	3.3	3.399			
	$I_O = 1 \text{ mA to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	3.218	3.3	3.382			
	$I_O = 1 \text{ mA to } 150 \text{ mA}$	3.177	3.3	3.423			
$I(Q)$	Quiescent current (GND terminal current)	$I_O = 0 \text{ to } 150 \text{ mA}$, $T_J = 25^\circ\text{C}$, See Note 2		85	100	μA	
		$I_O = 0 \text{ to } 150 \text{ mA}$, See Note 2			140		
	Standby current	$EN < 0.5 \text{ V}$, $T_J = 25^\circ\text{C}$		0.5	1		
		$EN < 0.5 \text{ V}$			2		
V_n	Output noise voltage	$BW = 300 \text{ Hz to } 50 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$, See Note 2		50		μV	
	Bypass voltage	$T_J = 25^\circ\text{C}$		1.192		V	
PSRR	Ripple rejection	$f = 1 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$, See Note 2		60		dB	
	Current limit	$T_J = 25^\circ\text{C}$ See Note 3		0.8	1.5	A	

NOTES: 2. Minimum I_N operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater.
3. Test condition includes, output voltage $V_O = 0 \text{ V}$ and pulse duration = 10 ms .



TPS76425, TPS76427, TPS76428, TPS76430, TPS76433

LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $EN = IN$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 4)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $V_I \geq 3.5 \text{ V}$, $T_J = 25^\circ\text{C}$		0.04	0.07	%V	
		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $V_I \geq 3.5 \text{ V}$			0.1		
V_{IH}	EN high level input	See Note 2		1.4	2	V	
V_{IL}	EN low level input	See Note 2	0.5	1.2			
I_I	EN input current	$EN = 0 \text{ V}$		-0.01	-0.5	μA	
		$EN = IN$		-0.01	-0.5		
V_{DO}	Dropout voltage (Note 5)	TPS76425	$I_O = 0 \text{ mA}$, $T_J = 25^\circ\text{C}$		0.2	mV	
			$I_O = 1 \text{ mA}$, $T_J = 25^\circ\text{C}$		3		
			$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		120		150
			$I_O = 50 \text{ mA}$				200
			$I_O = 75 \text{ mA}$, $T_J = 25^\circ\text{C}$		180		225
			$I_O = 75 \text{ mA}$				300
			$I_O = 100 \text{ mA}$, $T_J = 25^\circ\text{C}$		240		300
			$I_O = 100 \text{ mA}$				400
			$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$		360		450
			$I_O = 150 \text{ mA}$				600
		TPS76433	$I_O = 0 \text{ mA}$, $T_J = 25^\circ\text{C}$		0.2		mV
			$I_O = 1 \text{ mA}$, $T_J = 25^\circ\text{C}$		3		
			$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		100	125	
			$I_O = 50 \text{ mA}$			166	
			$I_O = 75 \text{ mA}$, $T_J = 25^\circ\text{C}$		150	188	
			$I_O = 75 \text{ mA}$			250	
			$I_O = 100 \text{ mA}$, $T_J = 25^\circ\text{C}$		200	250	
			$I_O = 100 \text{ mA}$			333	
			$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$		300	375	
			$I_O = 150 \text{ mA}$			500	

NOTES: 2. Minimum I_N operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater.

4. If $V_O < 2.5 \text{ V}$ and $V_{I\text{max}} = 10 \text{ V}$, $V_{I\text{min}} = 3.5 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - 3.5 \text{ V})}{100} \times 1000$$

If $V_O > 2.5 \text{ V}$ and $V_{I\text{max}} = 10 \text{ V}$, $V_{I\text{min}} = V_O + 1 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - (V_O + 1))}{100} \times 1000$$

5. Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_I = V_O + 1.0 \text{ V}$.



TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1
		vs Free-air temperature	2, 3, 4
V_n	Output noise	vs Frequency	5
V_n	Output noise voltage	vs Bypass capacitance	6
		vs Load current	7
Z_O	Output impedance	vs Frequency	8
V_{DO}	Dropout voltage	vs Free-air temperature	9
	Ripple rejection	vs Frequency	10
	Line transient response		11, 13
	Load transient response		12, 14
	Compensation series resistance (CSR)	vs Output current	15, 17
		vs Added ceramic capacitance	16, 18

TPS76425

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

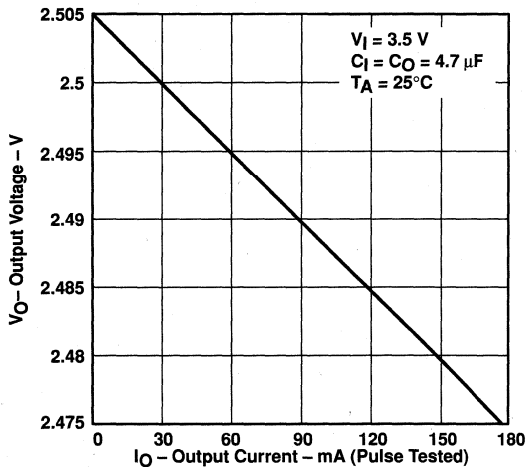


Figure 1

TPS76425

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

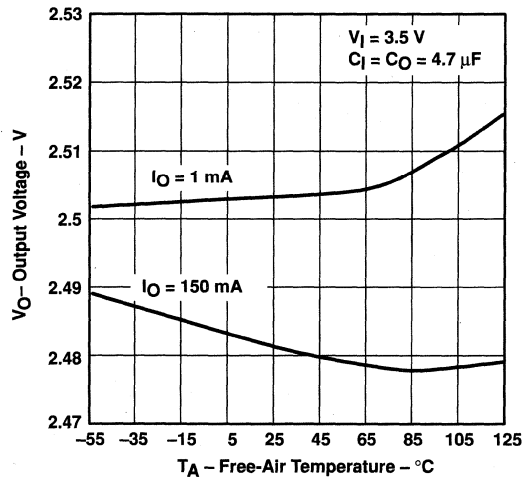


Figure 2

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433
 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

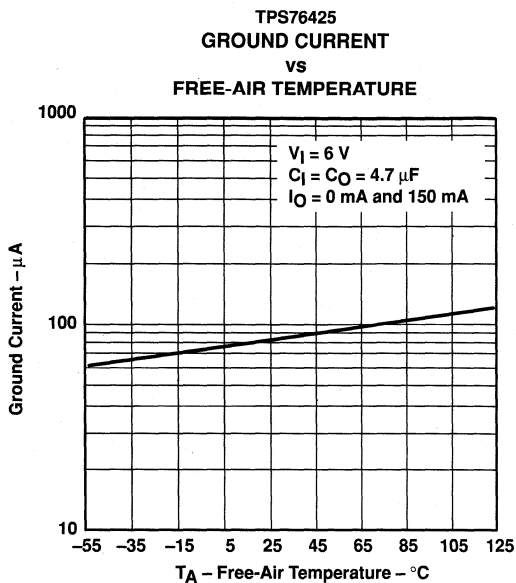


Figure 3

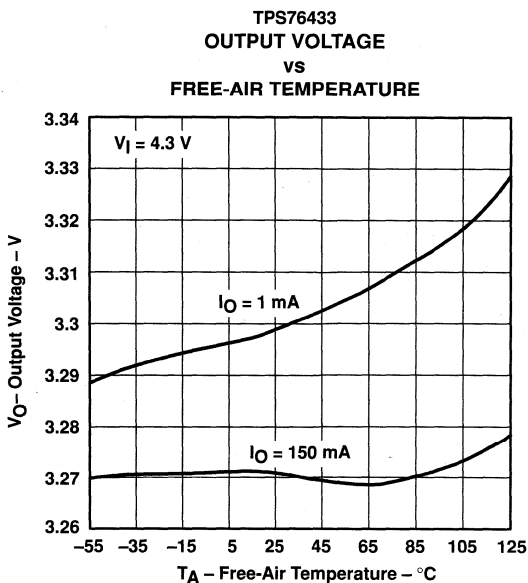


Figure 4

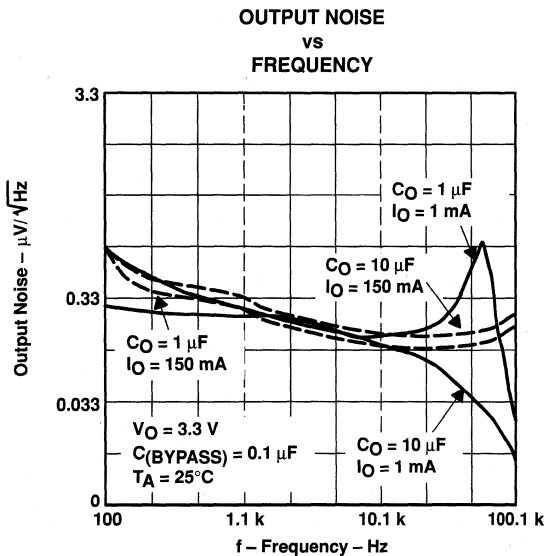


Figure 5

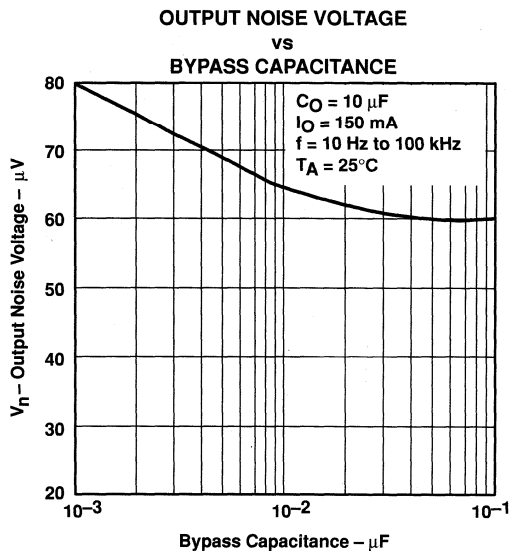


Figure 6



TPS76425, TPS76427, TPS76428, TPS76430, TPS76433
LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

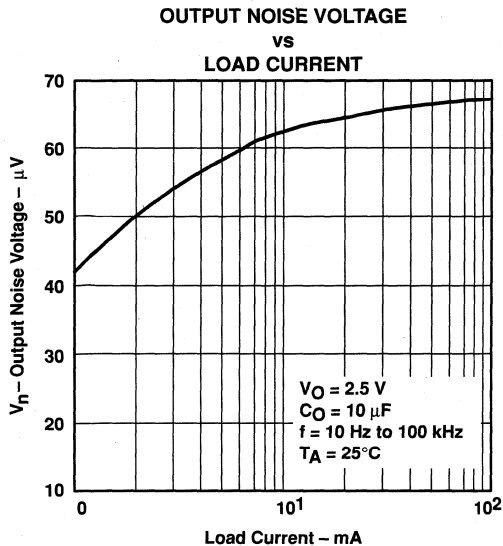


Figure 7

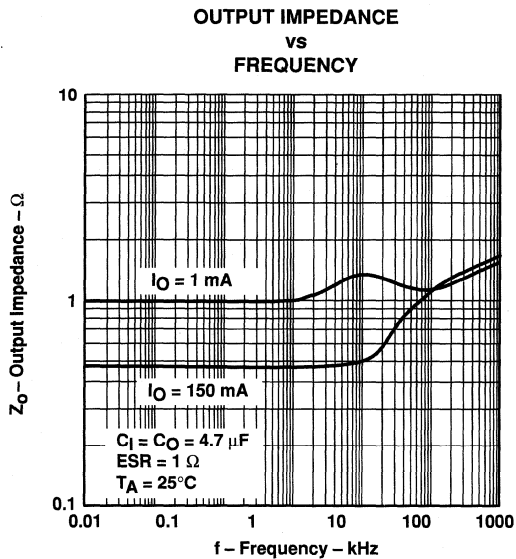


Figure 8

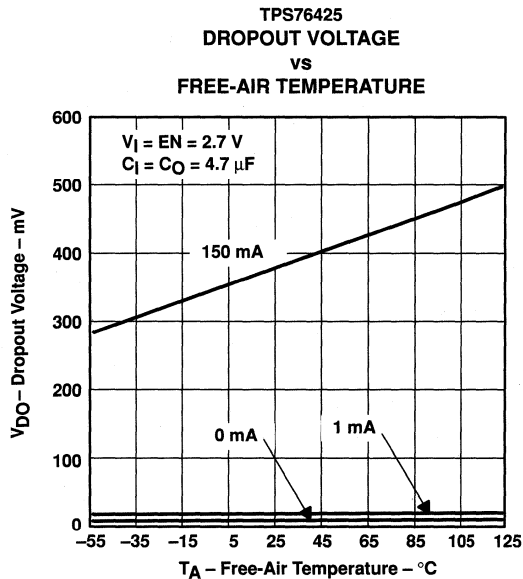


Figure 9

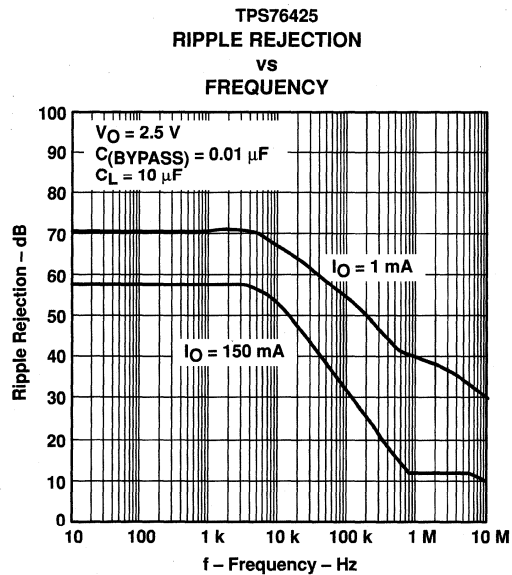


Figure 10



TPS76425, TPS76427, TPS76428, TPS76430, TPS76433
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TYPICAL CHARACTERISTICS

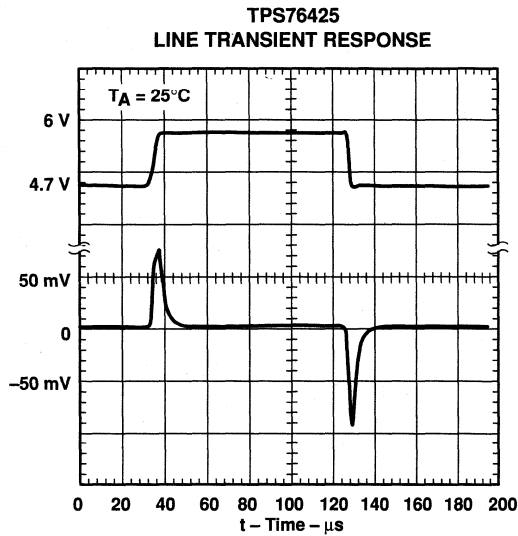


Figure 11

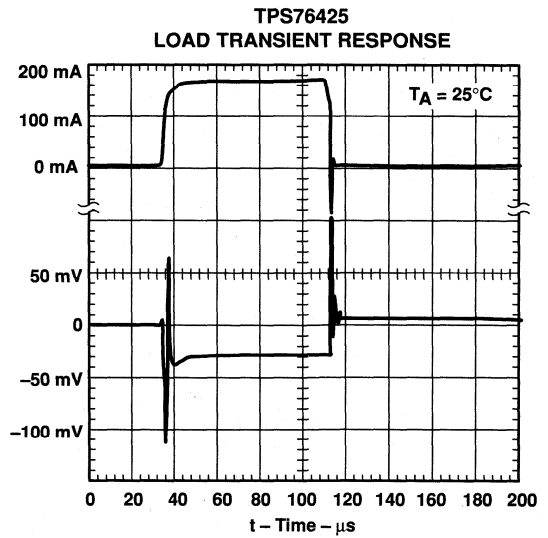


Figure 12

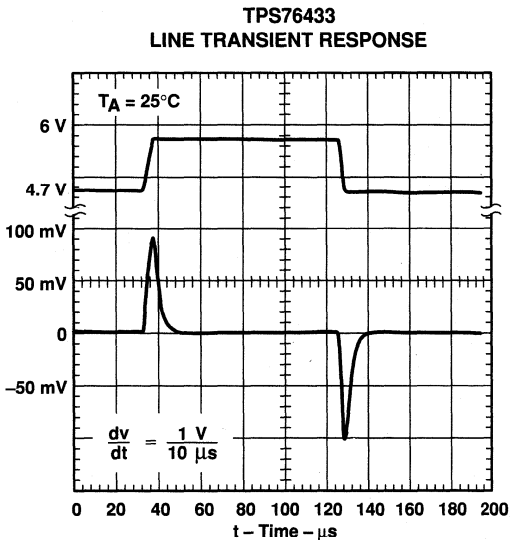


Figure 13

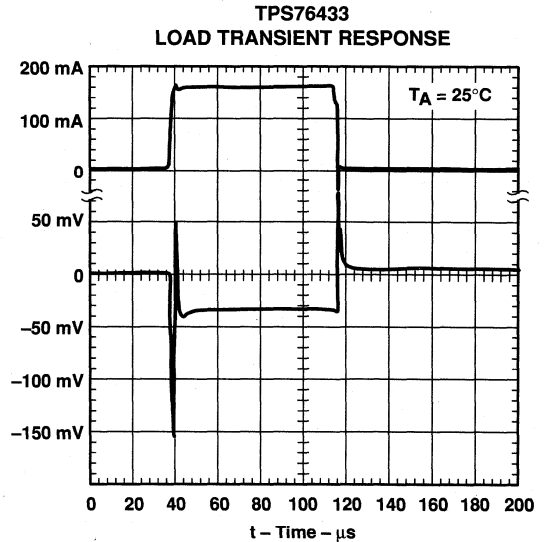


Figure 14

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
OUTPUT CURRENT

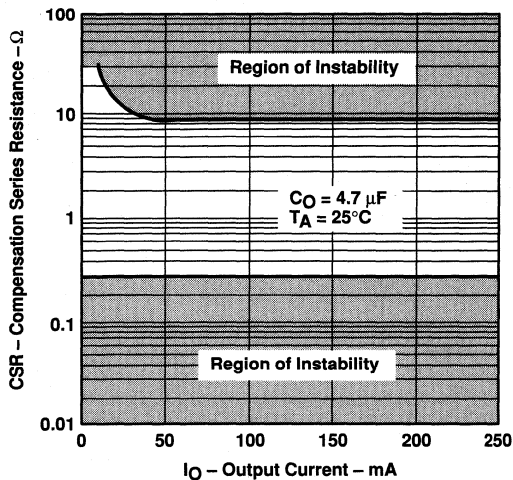


Figure 15

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
ADDED CERAMIC CAPACITANCE

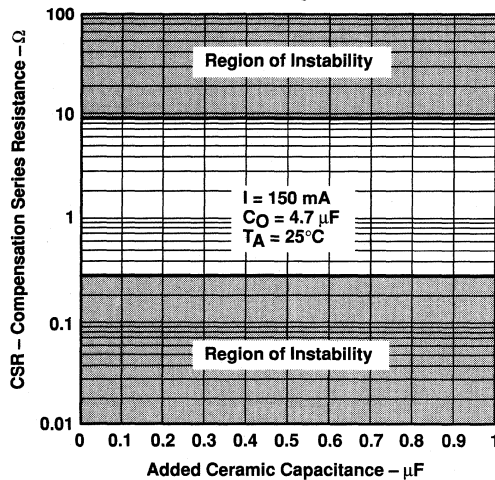


Figure 16

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
OUTPUT CURRENT

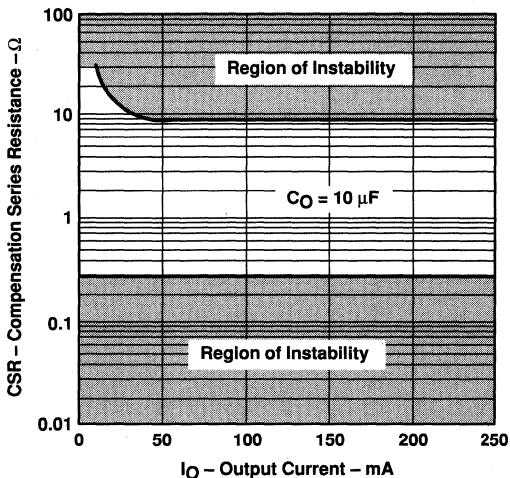


Figure 17

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)[†]
vs
ADDED CERAMIC CAPACITANCE

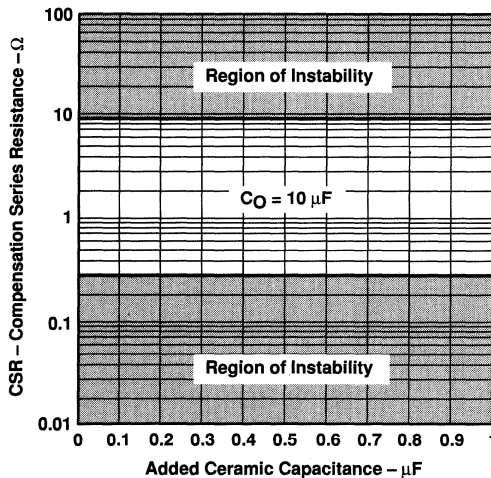


Figure 18

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

The TPS764xx family of low-noise and low-dropout (LDO) regulators are optimized for use in battery-operated equipment. They feature extremely low noise (50 μV), low dropout voltages, low quiescent current (140 μA), and an enable input to reduce supply current to less than 2 μA when the regulator is turned off.

device operation

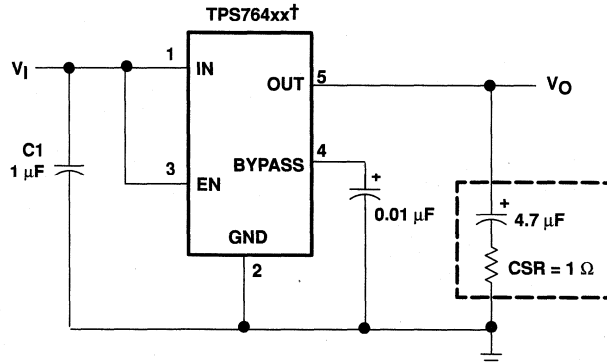
The TPS764xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device which, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS764xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

An internal resistor, in conjunction with external 0.01- μF bypass capacitor, creates a low-pass filter to further reduce the noise. The TPS764xx exhibits only 50 μV of output voltage noise using 0.01 μF bypass and 4.7- μF output capacitors.

A logic low on the enable input, EN, shuts off the output and reduces the supply current to less than 2 μA . EN should be tied high in applications where the shutdown feature is not used.

A typical application circuit is shown in Figure 22.



† TPS76425, TPS76427, TPS76430, TPS76433.

Figure 19. Typical Application Circuit

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047- μ F or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS764xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS764xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 μ F and the ESR (equivalent series resistance) must be between 0.2 Ω and 10 Ω . Capacitor values 4.7 μ F or larger are acceptable, provided the ESR is less than 10 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements previously stated. Multilayer ceramic capacitors should have minimum values of 1 μ F over the full operating temperature range of the equipment.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
T494B475K016AS	KEMET	4.7 μ F	1.5 Ω	1.9 \times 3.5 \times 2.8
195D106x0016x2T	SPRAGUE	10 μ F	1.5 Ω	1.3 \times 7.0 \times 2.7
695D106x003562T	SPRAGUE	10 μ F	1.3 Ω	2.5 \times 7.6 \times 2.5
TPSC475K035R0600	AVX	4.7 μ F	0.6 Ω	2.6 \times 6.0 \times 3.2

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Listings are sorted by height.

TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable without damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible.

regulator protection

The TPS764xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS764xx also features internal current limiting and thermal protection. During normal operation, the TPS764xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, regulator operation resumes.

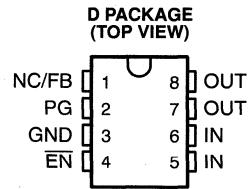


TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501

ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS236 – AUGUST 1999

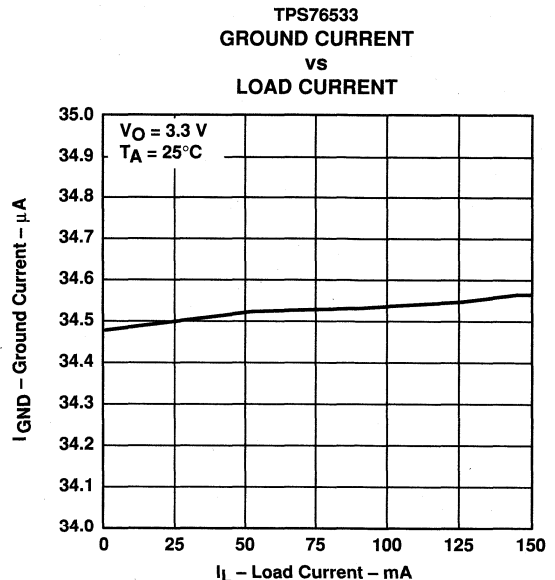
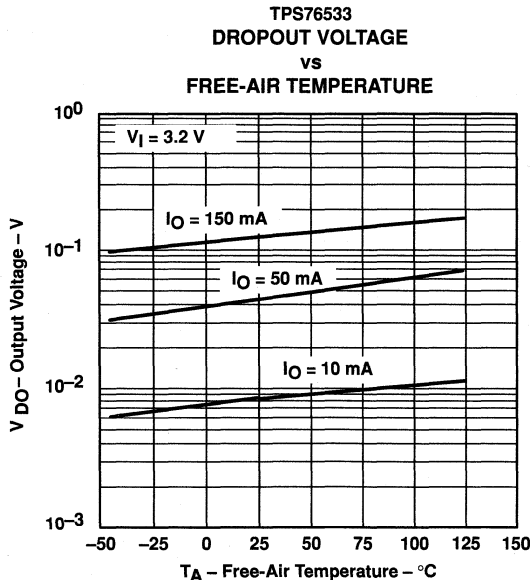
- 150-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage to 85 mV (Typ) at 150 mA (TPS76550)
- Ultra-Low 35- μ A Typical Quiescent Current
- 3% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power Good
- 8-Pin SOIC Package
- Thermal Shutdown Protection



description

This device is designed to have an ultra-low quiescent current and be stable with a 4.7- μ F capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 85 mV at an output current of 150 mA for the TPS76550) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35 μ A over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A (typ).



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS**

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description (continued)

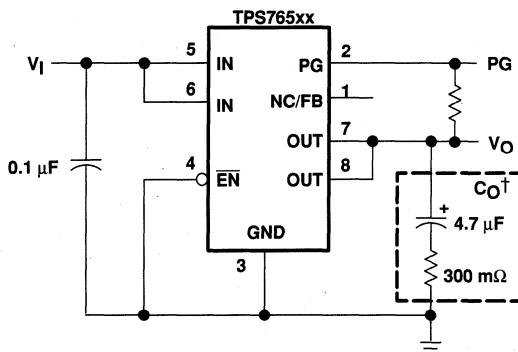
Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS765xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.25 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS765xx family is available in 8 pin SOIC package.

AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES
	TYP	SOIC (D)
-40°C to 125°C	5.0	TPS76550D
	3.3	TPS76533D
	3.0	TPS76530D
	2.8	TPS76528D
	2.7	TPS76527D
	2.5	TPS76525D
	1.8	TPS76518D
	1.5	TPS76515D
	Adjustable 1.25 V to 5.5 V	TPS76501D

The TPS76501 is programmable using an external resistor divider (see application information). The D package is available taped and reeled. Add an R suffix to the device type (e.g., TPS76501DR).



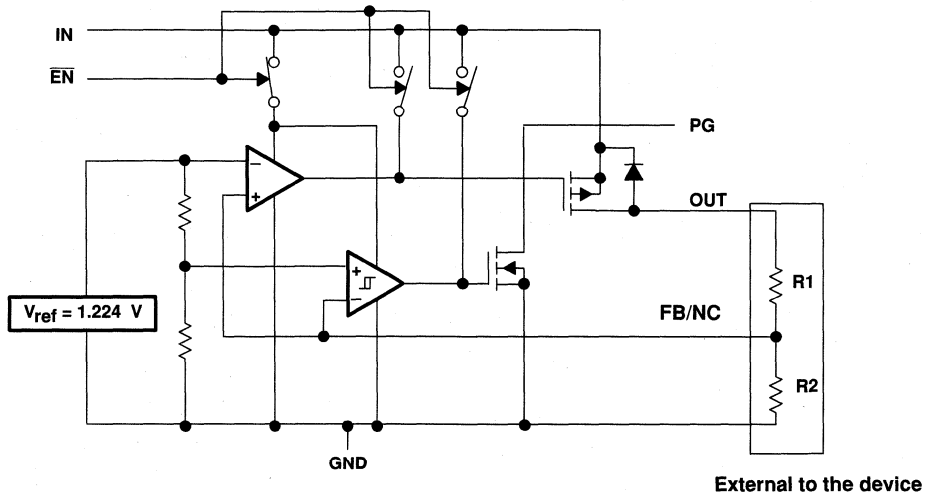
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

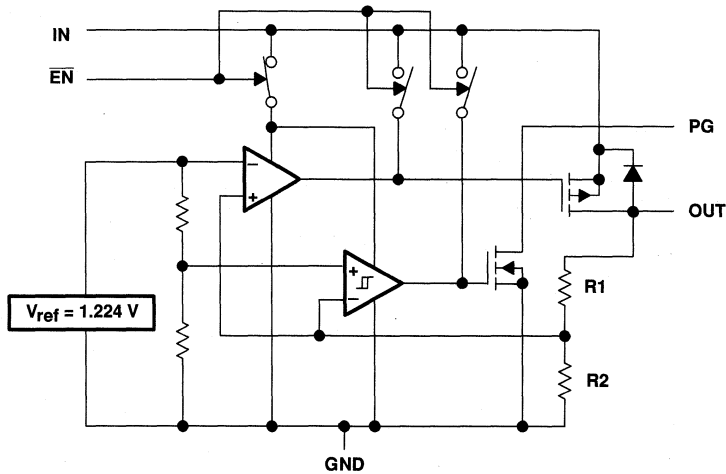
**TPS76515, TPS76518, TPS76525, TPS76527
TPS76528, TPS76530, TPS76533, TPS76550, TPS76501**
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



TPS76515, TPS76518, TPS76525, TPS76527
TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS
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Terminal Functions – SOIC Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	4	I	Enable input
FB/NC	1	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
IN	5	I	Input voltage
IN	6	I	Input voltage
OUT	7	O	Regulated output voltage
OUT	8	O	Regulated output voltage
PG	2	O	PG output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to 16.5 V
Maximum PG voltage	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See dissipation rating tables
Output voltage, V_O (OUT, FB)	7 V
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I ★	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	150	mA
Operating virtual junction temperature, T_J (Note 1)	–40	125	°C

★ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
 NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS76515, TPS76518, TPS76525, TPS76527
TPS76528, TPS76530, TPS76533, TPS76550, TPS76501**
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS236 – AUGUST 1999

**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 10 \mu\text{A}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT			
Output voltage (10 μA to 150 mA load) (see Note 2)	TPS76501	$5.5 \text{ V} \geq V_O \geq 1.25 \text{ V}$, $T_J = 25^\circ\text{C}$	V_O			V			
		$5.5 \text{ V} \geq V_O \geq 1.25 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	0.97 V_O				1.03 V_O		
	TPS76515	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.5						
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.455				1.545		
	TPS76518	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.8						
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.746				1.854		
	TPS76525	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.5						
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.425				2.575		
	TPS76527	$T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.7						
		$T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.619				2.781		
	TPS76528	$T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.8						
		$T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.716				2.884		
	TPS76530	$T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{IN} < 10 \text{ V}$	3.0						
		$T_J = -40^\circ\text{C}$ to 125°C , $4.0 \text{ V} < V_{IN} < 10 \text{ V}$	2.910				3.090		
TPS76533	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.3							
	$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.201			3.399				
TPS76550	$T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{IN} < 10 \text{ V}$	5.0							
	$T_J = -40^\circ\text{C}$ to 125°C , $6.0 \text{ V} < V_{IN} < 10 \text{ V}$	4.850			5.150				
Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$, (see Note 2)		$10 \mu\text{A} < I_O < 150 \text{ mA}$, $T_J = 25^\circ\text{C}$	35			μA			
		$I_O = 150 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					50		
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$	0.01			%/V			
Load regulation		$I_O = 10 \mu\text{A}$ to 150 mA	0.3%						
Output noise voltage		BW = 300 Hz to 50 kHz, $C_O = 4.7 \mu\text{F}$, $T_J = 25^\circ\text{C}$	200			μVrms			
Output current Limit		$V_O = 0 \text{ V}$		0.8	1.2	A			
Thermal shutdown junction temperature			150			$^\circ\text{C}$			
Standby current		$\overline{\text{EN}} = V_I$, $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_I < 10 \text{ V}$	1			μA			
		$\overline{\text{EN}} = V_I$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_I < 10 \text{ V}$				10	μA		
FB input current	TPS76501	FB = 1.5 V	2			nA			
High level enable input voltage			2.0			V			
Low level enable input voltage						0.8	V		
Power supply ripple rejection (see Note 2)		f = 1 kHz, $I_O = 10 \mu\text{A}$, $C_O = 4.7 \mu\text{F}$, $T_J = 25^\circ\text{C}$	63			dB			
PG	Minimum input voltage for valid PG		$I_O(\text{PG}) = 300 \mu\text{A}$			1.1	V		
	Trip threshold voltage		V_O decreasing			92	98	% V_O	
	Hysteresis voltage		Measured at V_O			0.5	% V_O		
	Output low voltage		$V_I = 2.7 \text{ V}$, $I_O(\text{PG}) = 1 \text{ mA}$				0.15	0.4	V
	Leakage current		$V(\text{PG}) = 5 \text{ V}$				1	μA	
Input current (EN)		$\overline{\text{EN}} = 0 \text{ V}$	-1	0	1	μA			
		$\overline{\text{EN}} = V_I$	-1				1		

NOTE: 2. Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10 V.



**TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS**

SLVS236 – AUGUST 1999

**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 10 \mu\text{A}$, $\text{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage (See Note 4)	TPS76528	$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$			190		mV
		$I_O = 150 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$				330	
	TPS76530	$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$			160		
		$I_O = 150 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$				280	
	TPS76533	$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$			140		
		$I_O = 150 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$				240	
	TPS76550	$I_O = 150 \text{ mA}$, $T_J = 25^\circ\text{C}$				85	
		$I_O = 150 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$				150	

NOTES: 3. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imin}} = 2.7 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imin}} = V_O + 1 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

4. IN voltage equals $V_O(\text{Typ}) - 100 \text{ mV}$; TPS76501 output voltage set to 3.3 V nominal with external resistor divider. TPS76515, TPS76518, TPS76525, and TPS76527 dropout voltage limited by input voltage range limitations (i.e., TPS76530 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

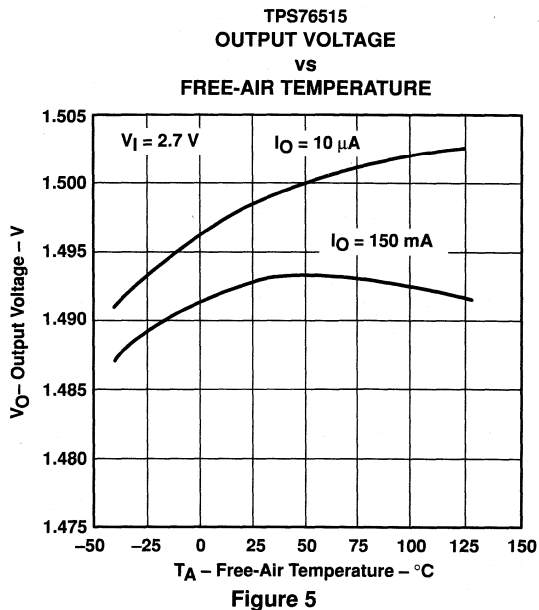
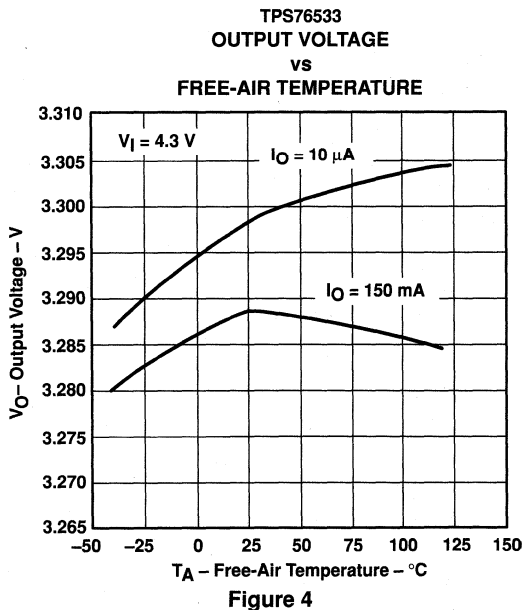
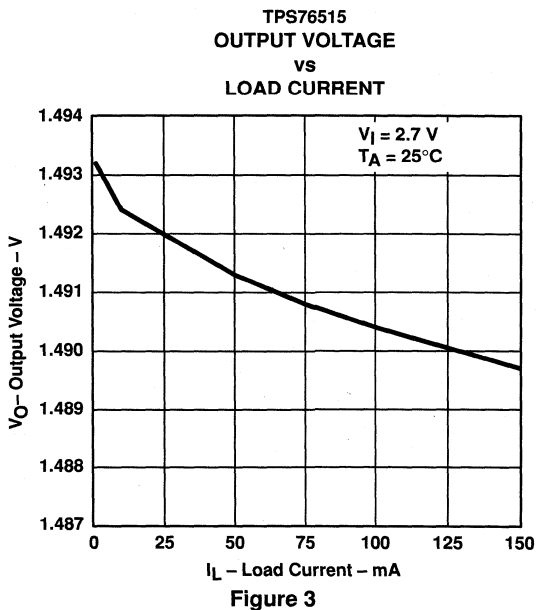
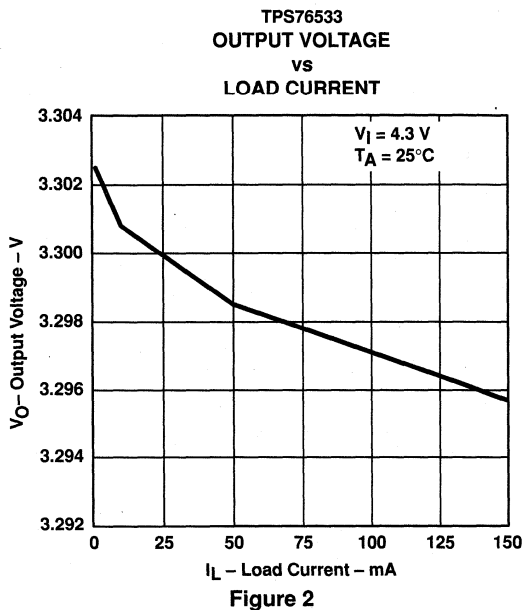
		FIGURE
Output voltage	vs Load current	2, 3
	vs Free-air temperature	4, 5
Ground current	vs Load current	6, 7
	vs Free-air temperature	8, 9
Power supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
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Line transient response		15, 17
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Output voltage	vs Time	19
Dropout voltage	vs Input voltage	20
Equivalent series resistance (ESR)	vs Output current	21 – 24
Equivalent series resistance (ESR)	vs Added ceramic capacitance	25, 26



TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

TPS76533
 GROUND CURRENT
 vs
 LOAD CURRENT

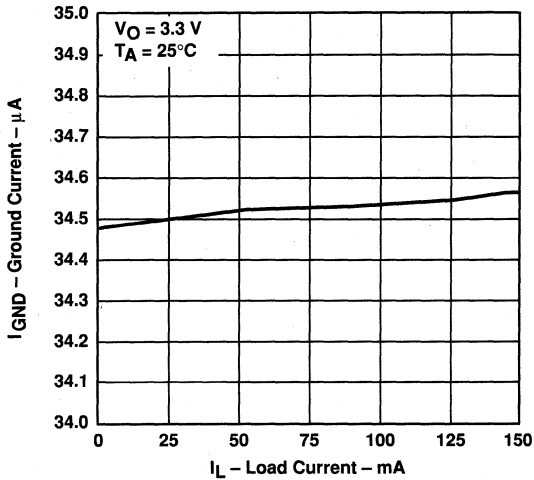


Figure 6

TPS76515
 GROUND CURRENT
 vs
 LOAD CURRENT

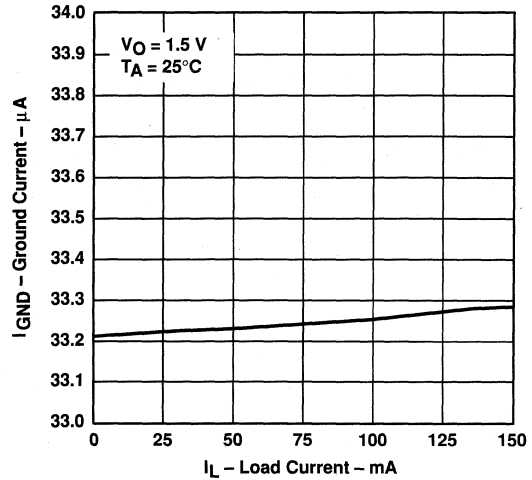


Figure 7

TPS76533
 GROUND CURRENT
 vs
 FREE-AIR TEMPERATURE

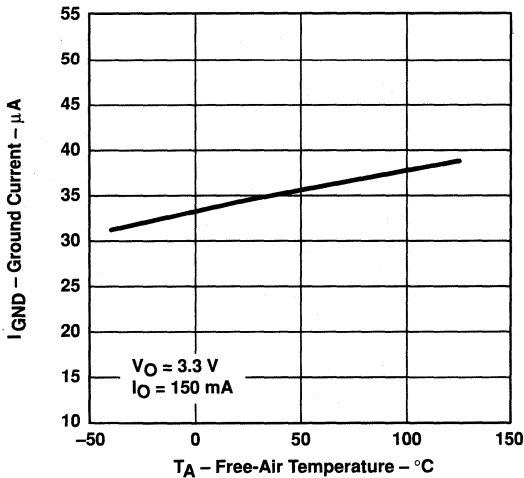


Figure 8

TPS76515
 GROUND CURRENT
 vs
 FREE-AIR TEMPERATURE

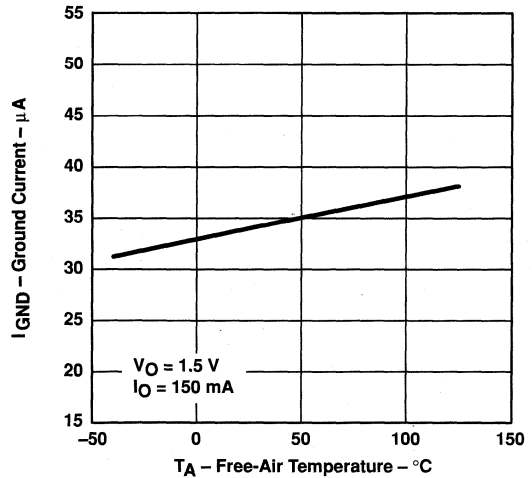
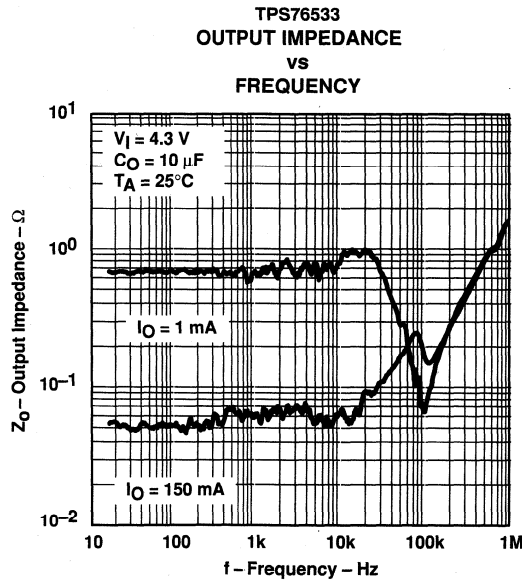
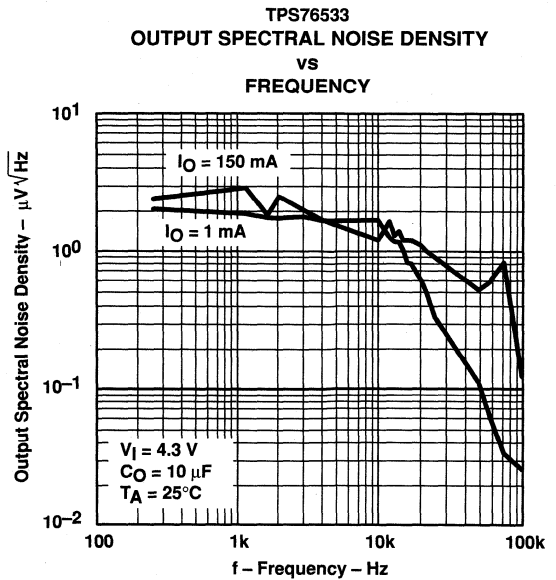
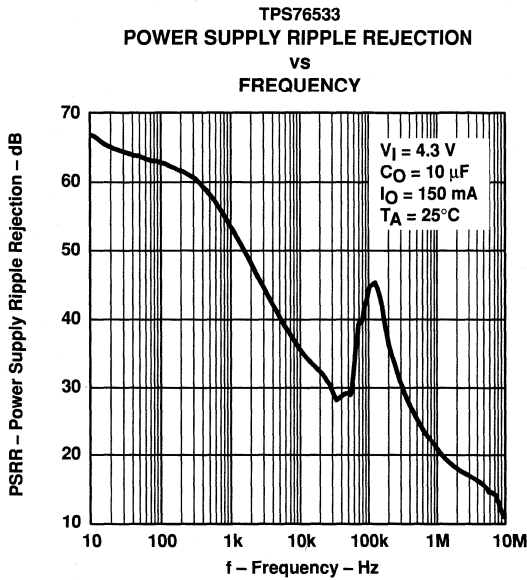


Figure 9

TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

TPS76550
 DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

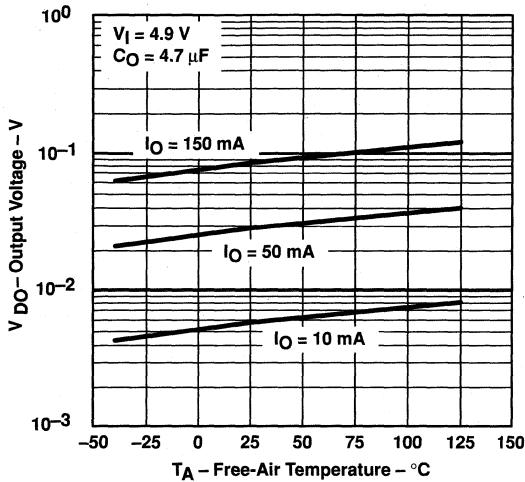


Figure 13

TPS76533
 DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

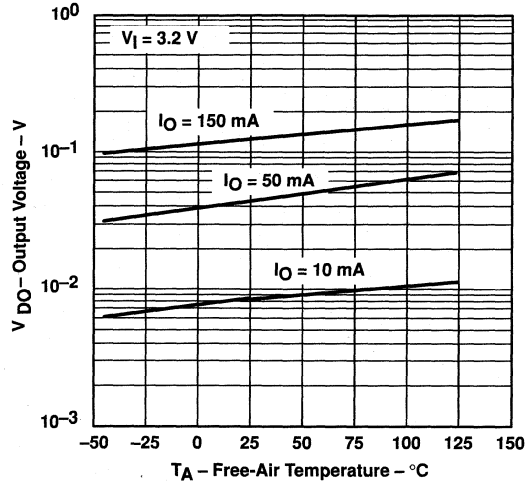


Figure 14

TPS76515
 LINE TRANSIENT RESPONSE

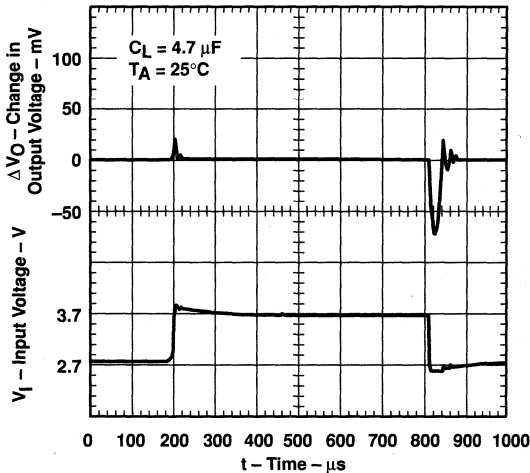


Figure 15

TPS76515
 LOAD TRANSIENT RESPONSE

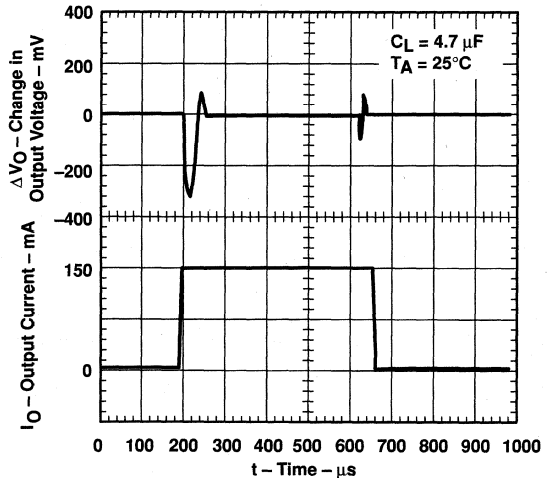


Figure 16

TPS76515, TPS76518, TPS76525, TPS76527
 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

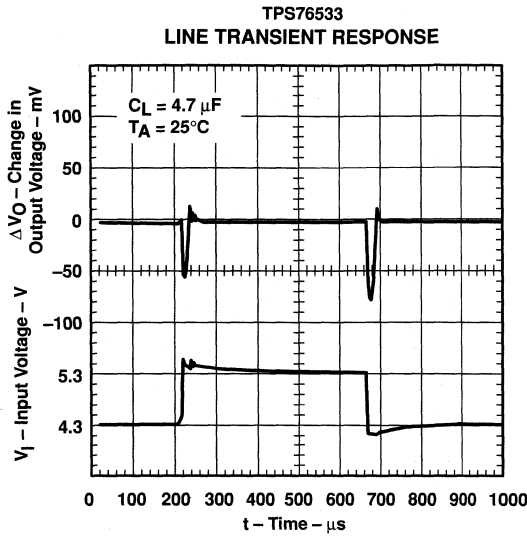


Figure 17

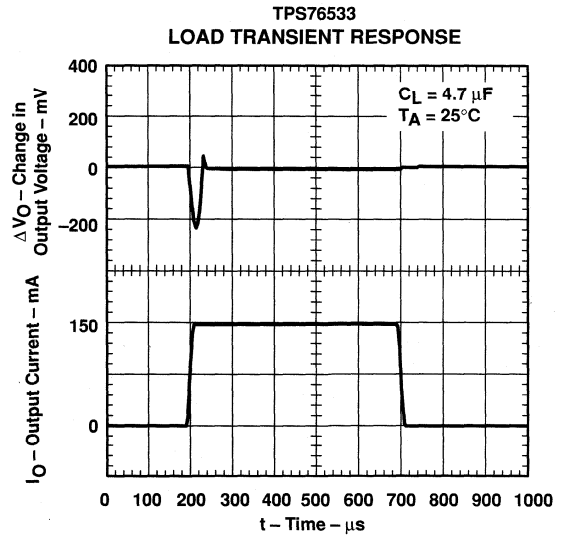


Figure 18

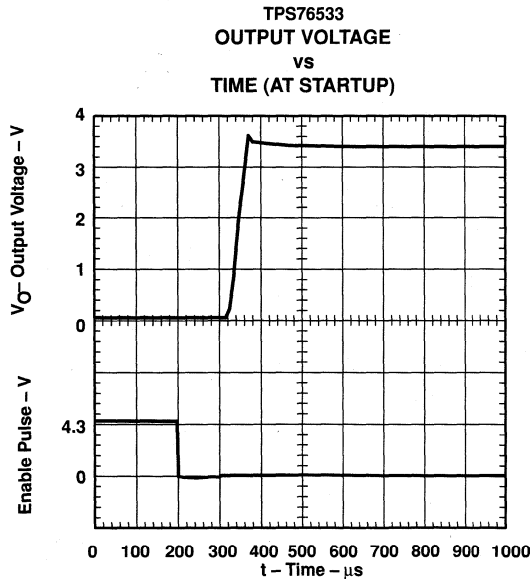


Figure 19

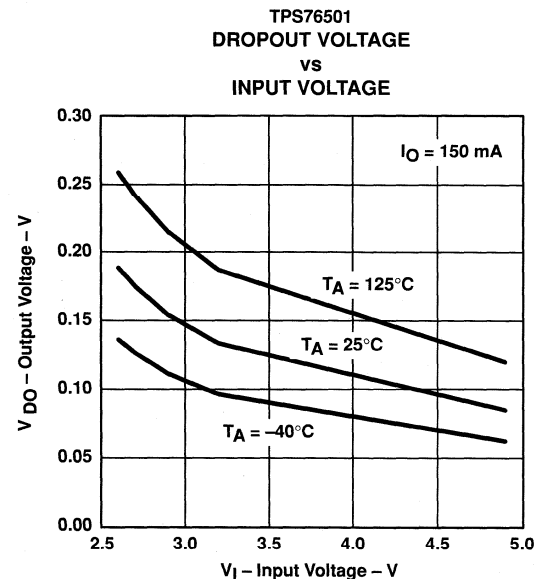


Figure 20

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

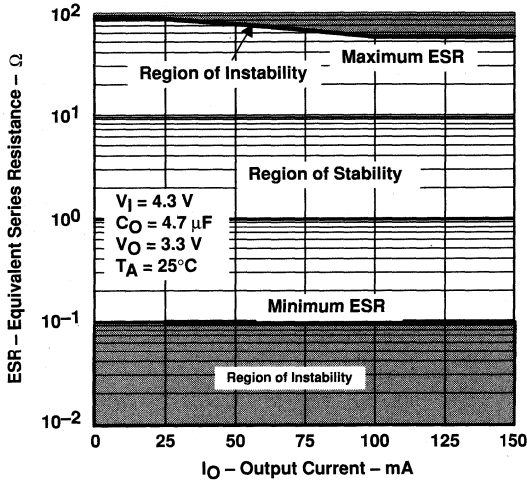


Figure 21

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

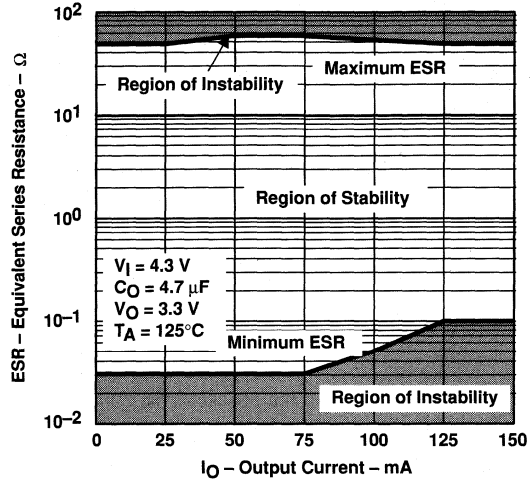


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

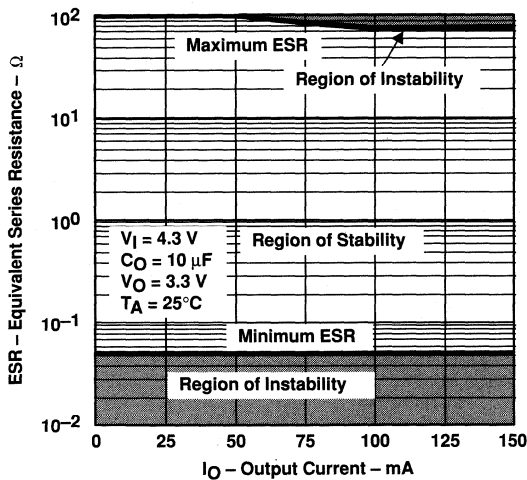


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

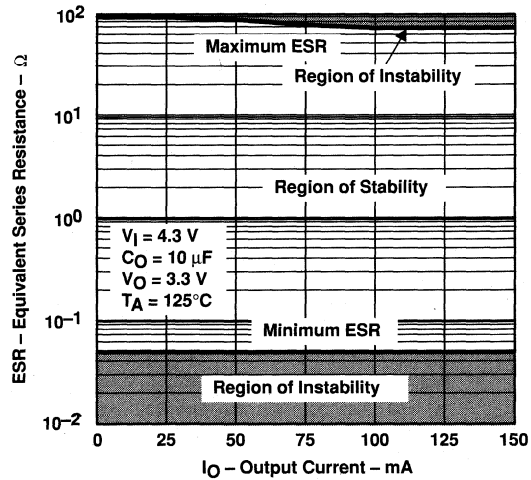


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TYPICAL CHARACTERISTICS

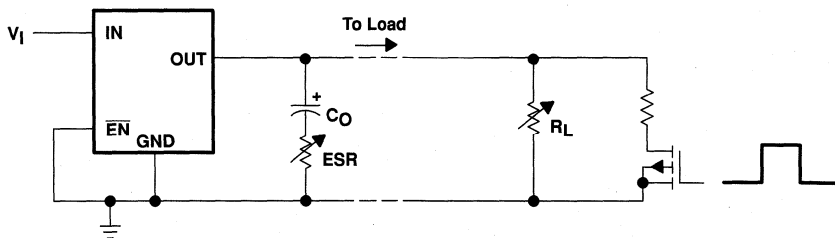
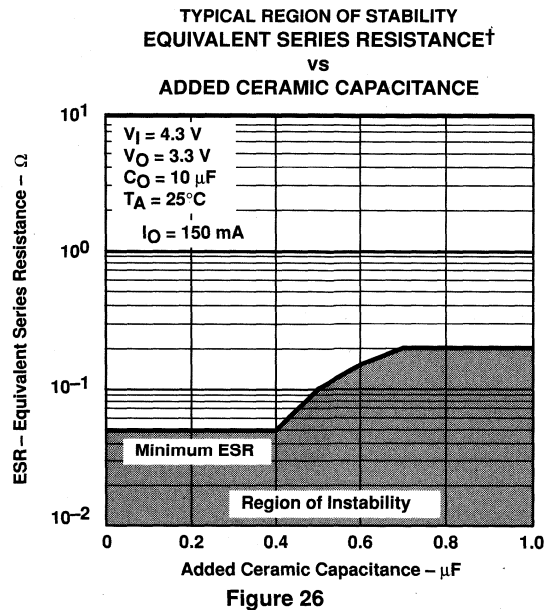
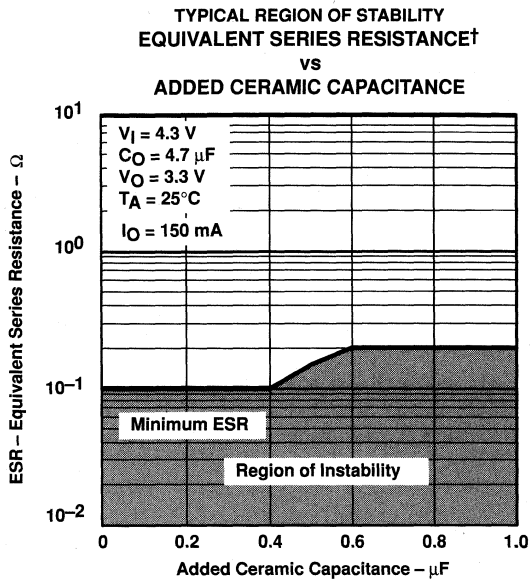


Figure 27. Test Circuit for Typical Regions of Stability (Figures 20 through 23) (Fixed Output Options)

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS76515, TPS76518, TPS76525, TPS76527
TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

The TPS765xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76501 (adjustable from 1.25 V to 5.5 V).

device operation

The TPS765xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS765xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS765xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS765xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1 μ A (typ). If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160 μ s.

minimum load requirements

The TPS765xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 29. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS765xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS765xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 μ F and the ESR (equivalent series resistance) must be between 300-m Ω and 20- Ω . Capacitor values 4.7 μ F or larger are acceptable, provided the ESR is less than 20 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.



**TPS76515, TPS76518, TPS76525, TPS76527
TPS76528, TPS76530, TPS76533, TPS76550, TPS76501**
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

external capacitor requirements (continued)

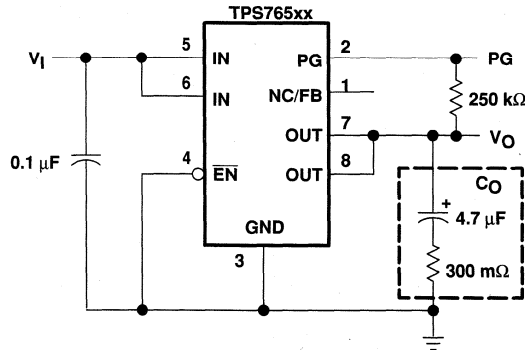


Figure 28. Typical Application Circuit (Fixed Versions)

programming the TPS76501 adjustable LDO regulator

The output voltage of the TPS76501 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

$$V_{ref} = 1.224 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

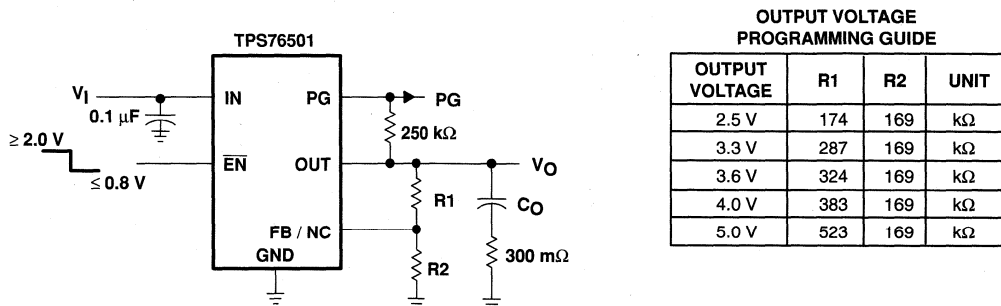


Figure 29. TPS76501 Adjustable LDO Regulator Programming

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TPS76528, TPS76530, TPS76533, TPS76550, TPS76501
ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

power-good indicator

The TPS765xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS765xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS765xx also features internal current limiting and thermal protection. During normal operation, the TPS765xx limits output current to approximately 0.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

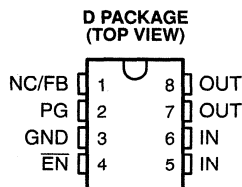
Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

TPS76615, TPS76618, TPS76625, TPS76627
 TPS76628, TPS76630, TPS76633, TPS76650, TPS76601

ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS

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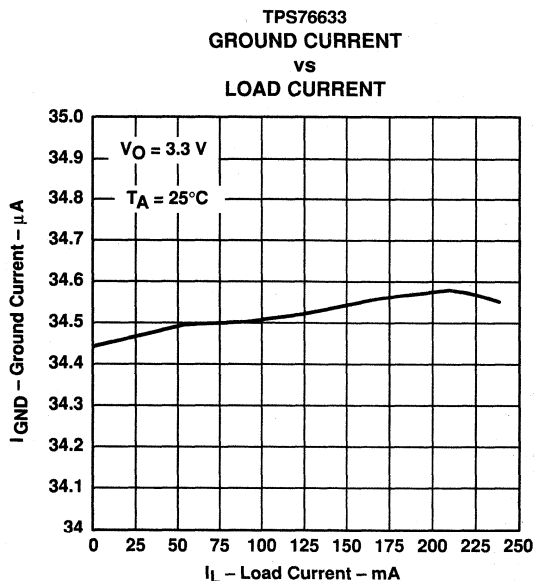
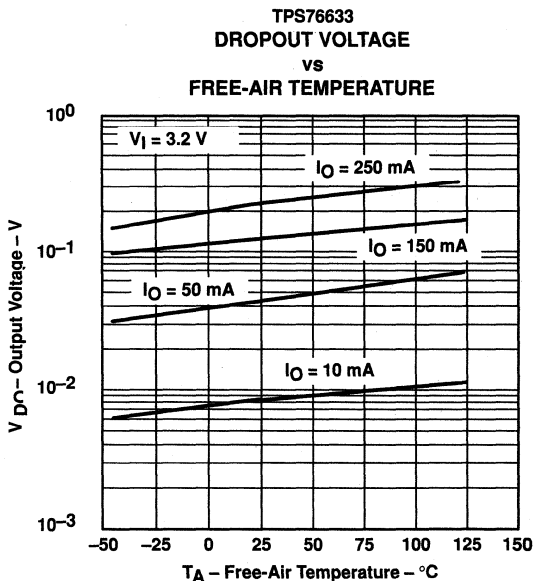
- 250-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage to 140 mV (Typ) at 250 mA (TPS76650)
- Ultra-Low 35- μ A Typical Quiescent Current
- 3% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power Good
- 8-Pin SOIC Package
- Thermal Shutdown Protection



description

This device is designed to have an ultra-low quiescent current and be stable with a 4.7- μ F capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 250 mA for the TPS76650) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35 μ A over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A (typ).



PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS76615, TPS76618, TPS76625, TPS76627
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ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS
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description (continued)

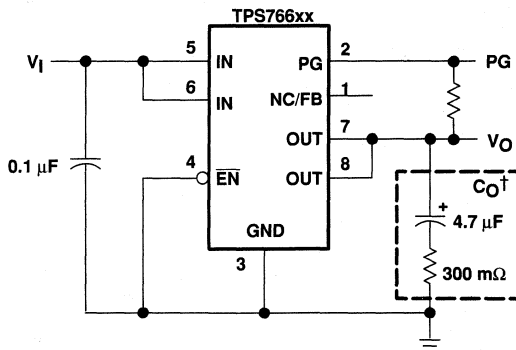
Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS766xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.25 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS766xx family is available in 8 pin SOIC package.

AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES
	TYP	SOIC (D)
-40°C to 125°C	5.0	TPS76650D
	3.3	TPS76633D
	3.0	TPS76630D
	2.8	TPS76628D
	2.7	TPS76627D
	2.5	TPS76625D
	1.8	TPS76618D
	1.5	TPS76615D
	Adjustable 1.25 V to 5.5 V	TPS76601D

The TPS76601 is programmable using an external resistor divider (see application information). The D package is available taped and reeled. Add an R suffix to the device type (e.g., TPS76601DR).



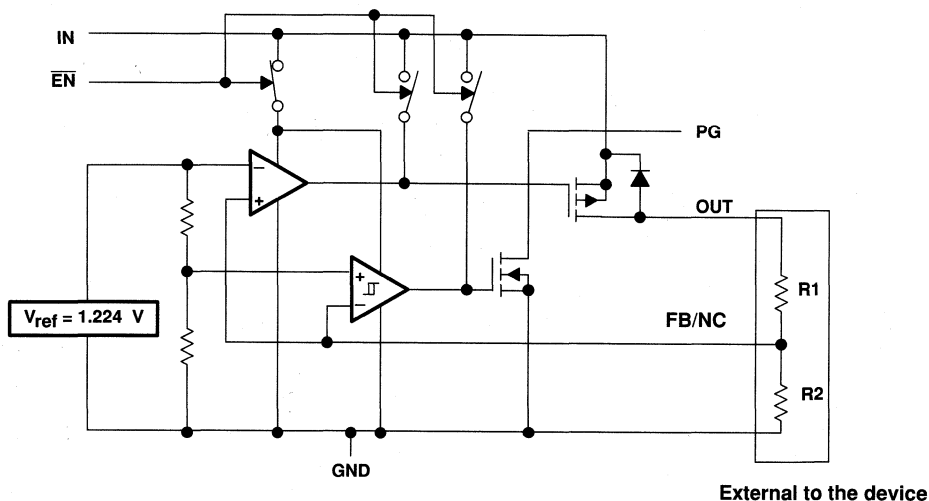
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

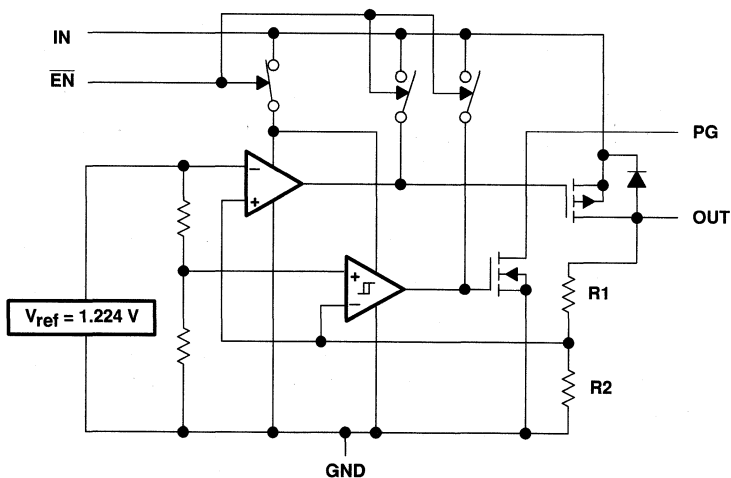
TPS76615, TPS76618, TPS76625, TPS76627
 TPS76628, TPS76630, TPS76633, TPS76650, TPS76601
 ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



**TPS76615, TPS76618, TPS76625, TPS76627
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Terminal Functions – SOIC Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	4	I	Enable input
FB/NC	1	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
IN	5	I	Input voltage
IN	6	I	Input voltage
OUT	7	O	Regulated output voltage
OUT	8	O	Regulated output voltage
PG	2	O	PG output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to 16.5 V
Maximum PG voltage	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See dissipation rating tables
Output voltage, V_O (OUT, FB)	7 V
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I *	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	250	mA
Operating virtual junction temperature, T_J (Note 1)	–40	125	°C

* To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
 NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



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**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(typ)} + 1\text{ V}$, $I_O = 10\ \mu\text{A}$, $\text{EN} = 0\text{ V}$, $C_O = 4.7\ \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output voltage (10 μA to 250 mA load) (see Note 2)	TPS76601	$5.5\text{ V} \geq V_O \geq 1.25\text{ V}$, $T_J = 25^\circ\text{C}$		V_O		V	
		$5.5\text{ V} \geq V_O \geq 1.25\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	$0.97V_O$		$1.03V_O$		
	TPS76615	$T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_{IN} < 10\text{ V}$		1.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7\text{ V} < V_{IN} < 10\text{ V}$	1.455		1.545		
	TPS76618	$T_J = 25^\circ\text{C}$, $2.8\text{ V} < V_{IN} < 10\text{ V}$		1.8			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.746		1.854		
	TPS76625	$T_J = 25^\circ\text{C}$, $3.5\text{ V} < V_{IN} < 10\text{ V}$		2.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5\text{ V} < V_{IN} < 10\text{ V}$	2.425		2.575		
	TPS76627	$T_J = 25^\circ\text{C}$, $3.7\text{ V} < V_{IN} < 10\text{ V}$		2.7			
		$T_J = -40^\circ\text{C}$ to 125°C , $3.7\text{ V} < V_{IN} < 10\text{ V}$	2.619		2.781		
	TPS76628	$T_J = 25^\circ\text{C}$, $3.8\text{ V} < V_{IN} < 10\text{ V}$		2.8			
		$T_J = -40^\circ\text{C}$ to 125°C , $3.8\text{ V} < V_{IN} < 10\text{ V}$	2.716		2.884		
	TPS76630	$T_J = 25^\circ\text{C}$, $4.0\text{ V} < V_{IN} < 10\text{ V}$		3.0			
		$T_J = -40^\circ\text{C}$ to 125°C , $4.0\text{ V} < V_{IN} < 10\text{ V}$	2.910		3.090		
	TPS76633	$T_J = 25^\circ\text{C}$, $4.3\text{ V} < V_{IN} < 10\text{ V}$		3.3			
		$T_J = -40^\circ\text{C}$ to 125°C , $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.201		3.399		
TPS76650	$T_J = 25^\circ\text{C}$, $6.0\text{ V} < V_{IN} < 10\text{ V}$		5.0				
	$T_J = -40^\circ\text{C}$ to 125°C , $6.0\text{ V} < V_{IN} < 10\text{ V}$	4.850		5.150			
Quiescent current (GND current) $\text{EN} = 0\text{V}$, (see Note 2)		$10\ \mu\text{A} < I_O < 250\text{ mA}$, $T_J = 25^\circ\text{C}$		35		μA	
		$I_O = 250\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			50		
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$		0.01		%/V	
Load regulation		$I_O = 10\ \mu\text{A}$ to 250 mA		0.5%			
Output noise voltage		$\text{BW} = 300\text{ Hz}$ to 50 kHz , $C_O = 4.7\ \mu\text{F}$, $T_J = 25^\circ\text{C}$		200		μVrms	
Output current Limit		$V_O = 0\text{ V}$		0.8	1.2	A	
Thermal shutdown junction temperature				150		$^\circ\text{C}$	
Standby current		$\text{EN} = V_I$, $T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_I < 10\text{ V}$		1		μA	
		$\text{EN} = V_I$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7\text{ V} < V_I < 10\text{ V}$			10	μA	
FB input current	TPS76601	$\text{FB} = 1.5\text{ V}$		2		nA	
High level enable input voltage				2.0		V	
Low level enable input voltage					0.8	V	
Power supply ripple rejection (see Note 2)		$f = 1\text{ kHz}$, $C_O = 4.7\ \mu\text{F}$, $I_O = 10\ \mu\text{A}$, $T_J = 25^\circ\text{C}$		63		dB	
PG	Minimum input voltage for valid PG		$I_O(\text{PG}) = 300\ \mu\text{A}$	1.1		V	
	Trip threshold voltage		V_O decreasing	92	98	% V_O	
	Hysteresis voltage		Measured at V_O	0.5		% V_O	
	Output low voltage		$V_I = 2.7\text{ V}$, $I_O(\text{PG}) = 1\text{ mA}$	0.15	0.4	V	
	Leakage current		$V(\text{PG}) = 5\text{ V}$			1 μA	
Input current (EN)		$\text{EN} = 0\text{ V}$	-1	0	1	μA	
		$\text{EN} = V_I$	-1		1		

NOTE: 2. Minimum IN operating voltage is 2.7 V or $V_{O(typ)} + 1\text{ V}$, whichever is greater. Maximum IN voltage 10 V.

**TPS76615, TPS76618, TPS76625, TPS76627
 TPS76628, TPS76630, TPS76633, TPS76650, TPS76601
 ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS**

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**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 10 \mu\text{A}$, $\text{EN} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout voltage (See Note 4)	TPS76628	$I_O = 250 \text{ mA}$, $T_J = 25^\circ\text{C}$		310		mV
		$I_O = 250 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			540	
	TPS76630	$I_O = 250 \text{ mA}$, $T_J = 25^\circ\text{C}$		270		
		$I_O = 250 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			470	
	TPS76633	$I_O = 250 \text{ mA}$, $T_J = 25^\circ\text{C}$		230		
		$I_O = 250 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			400	
	TPS76650	$I_O = 250 \text{ mA}$, $T_J = 25^\circ\text{C}$		140		
		$I_O = 250 \text{ mA}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$			250	

NOTES: 3. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imin}} = 2.7 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imin}} = V_O + 1 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

4. IN voltage equals $V_O(\text{Typ}) - 100 \text{ mV}$; TPS76601 output voltage set to 3.3 V nominal with external resistor divider. TPS76615, TPS76618, TPS76625, and TPS76627 dropout voltage limited by input voltage range limitations (i.e., TPS76630 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

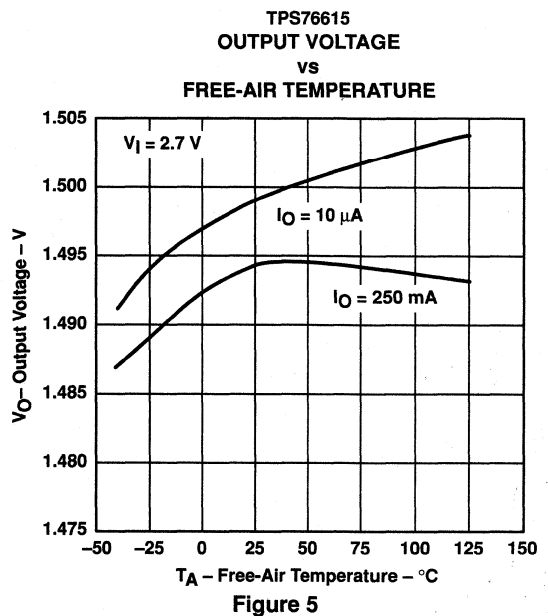
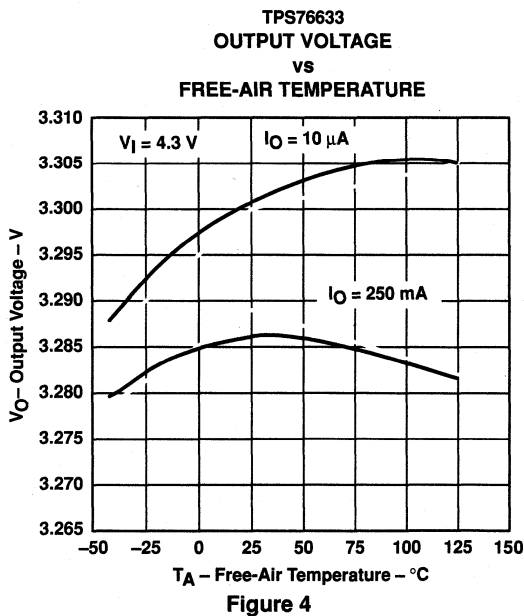
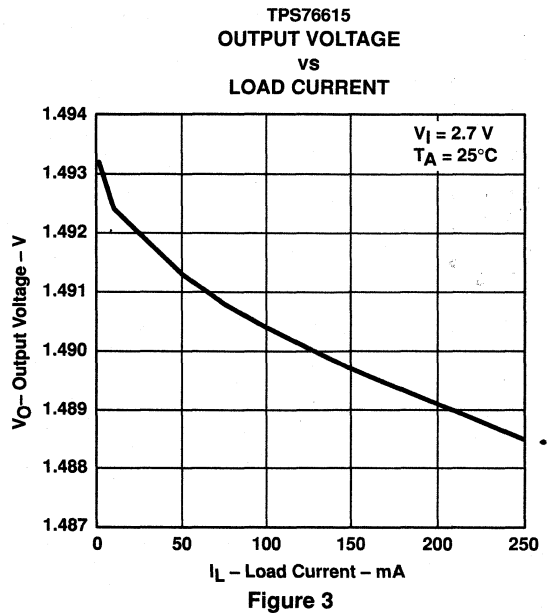
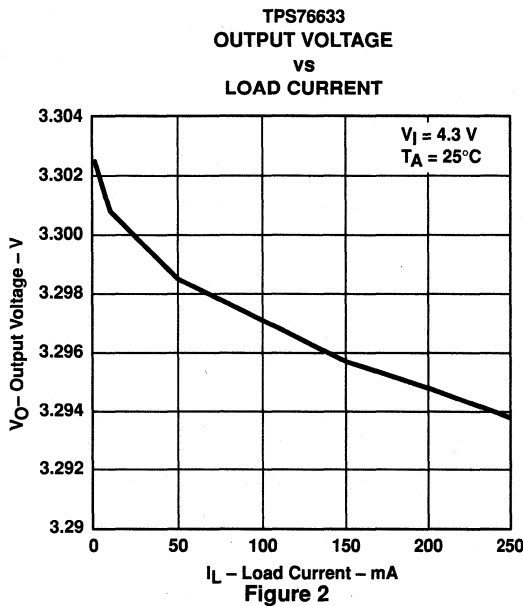
		FIGURE
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

TPS76633
 GROUND CURRENT
 vs
 LOAD CURRENT

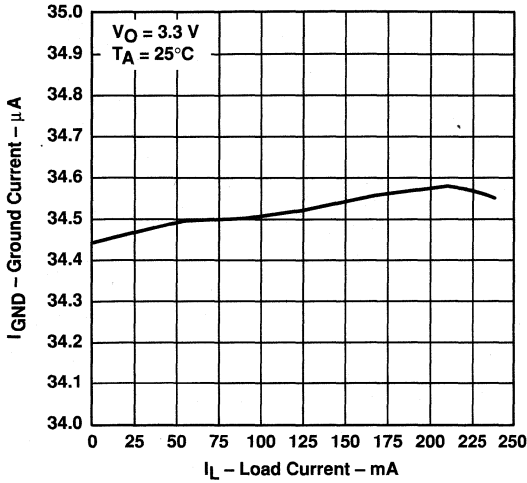


Figure 6

TPS76615
 GROUND CURRENT
 vs
 LOAD CURRENT

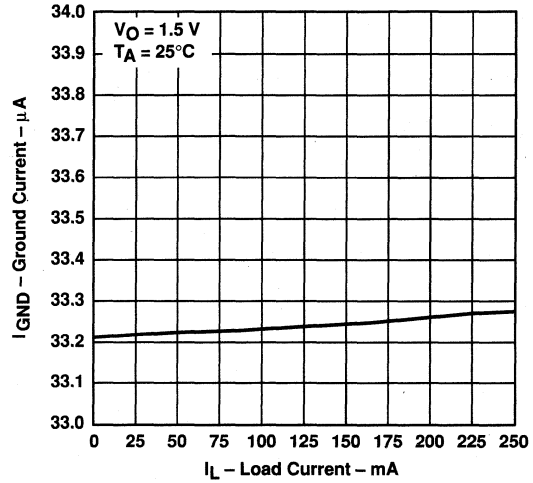


Figure 7

TPS76633
 GROUND CURRENT
 vs
 FREE-AIR TEMPERATURE

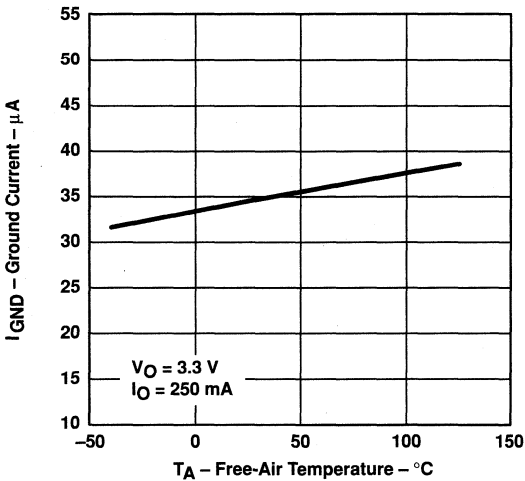


Figure 8

TPS76615
 GROUND CURRENT
 vs
 FREE-AIR TEMPERATURE

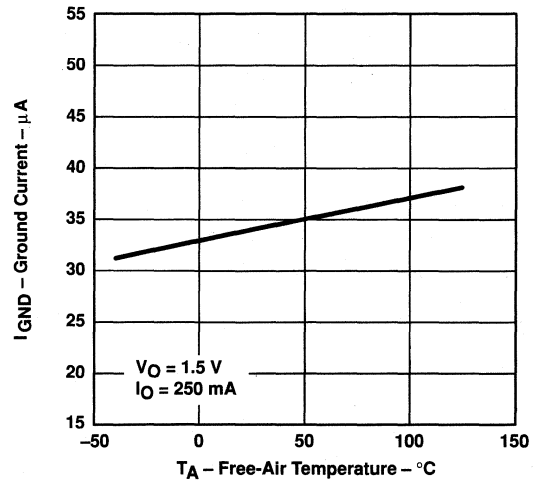


Figure 9

TYPICAL CHARACTERISTICS

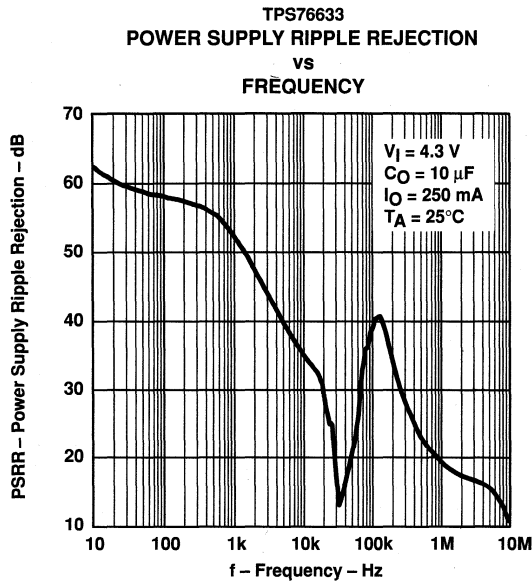


Figure 10

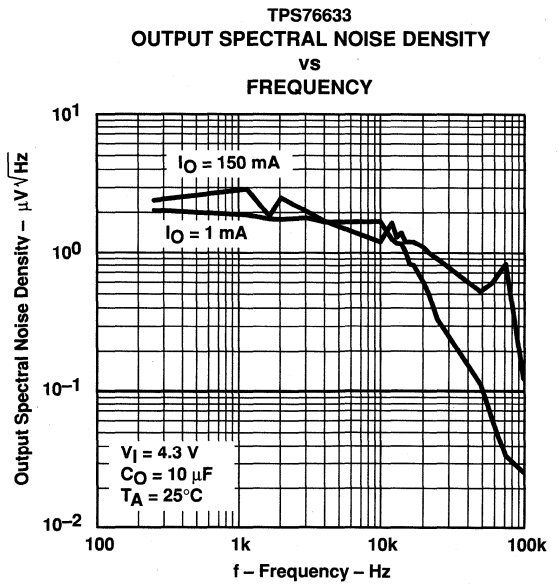


Figure 11

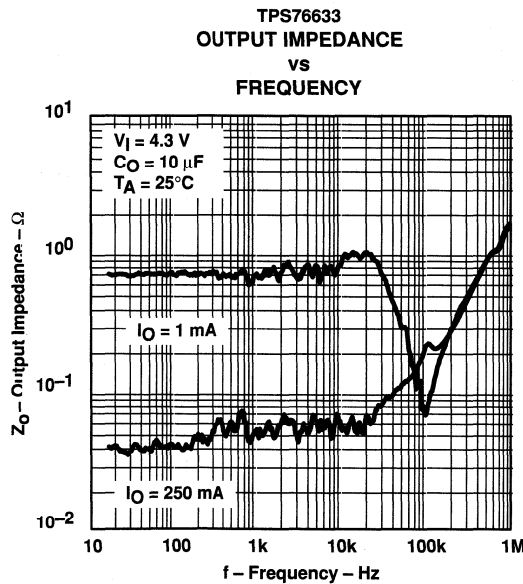


Figure 12

TYPICAL CHARACTERISTICS

TPS76650
 DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

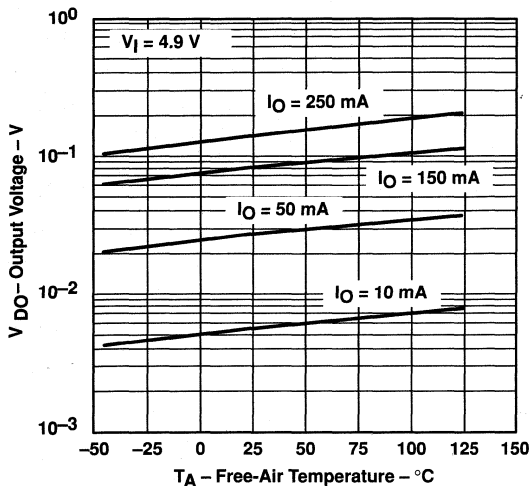


Figure 13

TPS76633
 DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

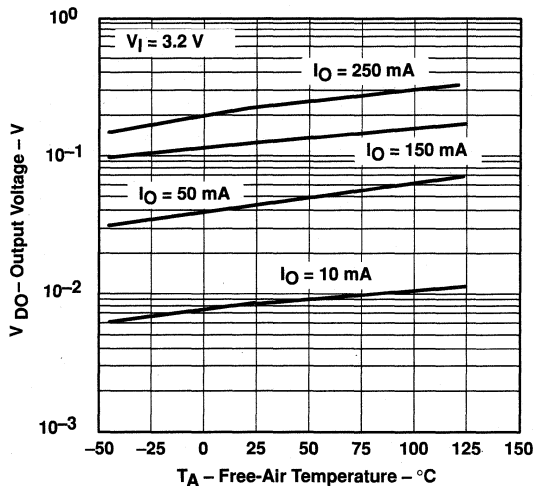


Figure 14

TPS76615
 LINE TRANSIENT RESPONSE

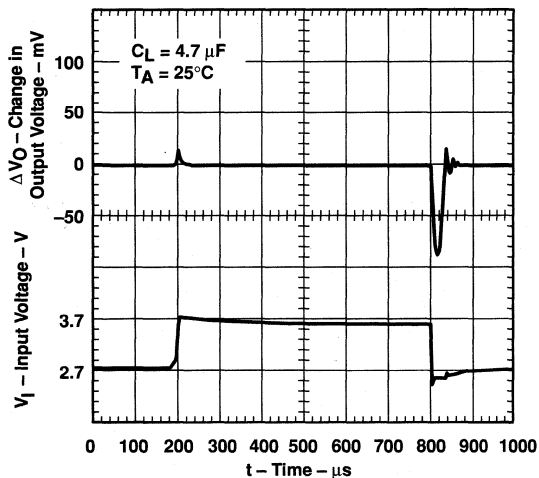


Figure 15

TPS76615
 LOAD TRANSIENT RESPONSE

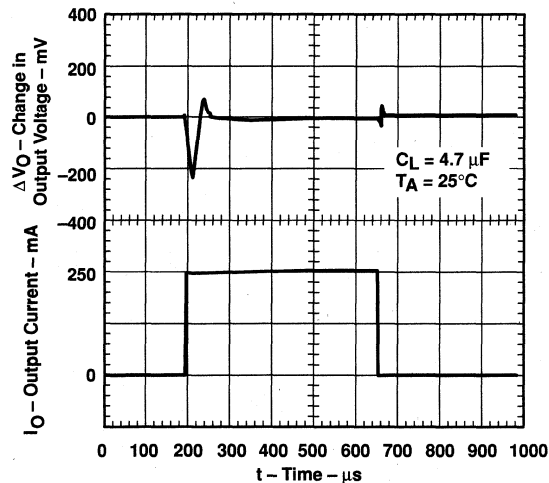


Figure 16

TPS76615, TPS76618, TPS76625, TPS76627
 TPS76628, TPS76630, TPS76633, TPS76650, TPS76601
ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS

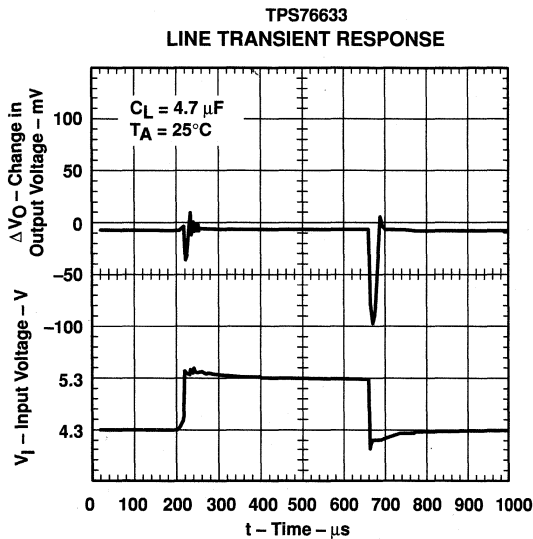


Figure 17

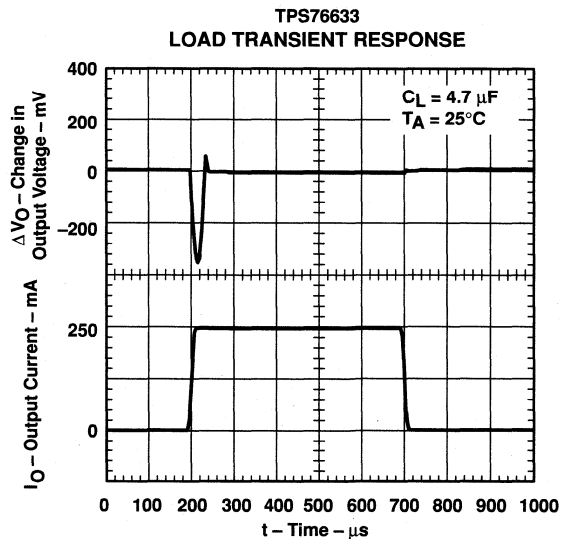


Figure 18

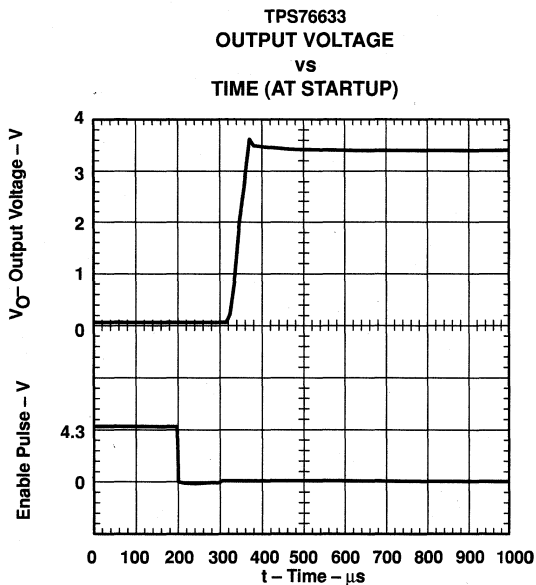


Figure 19

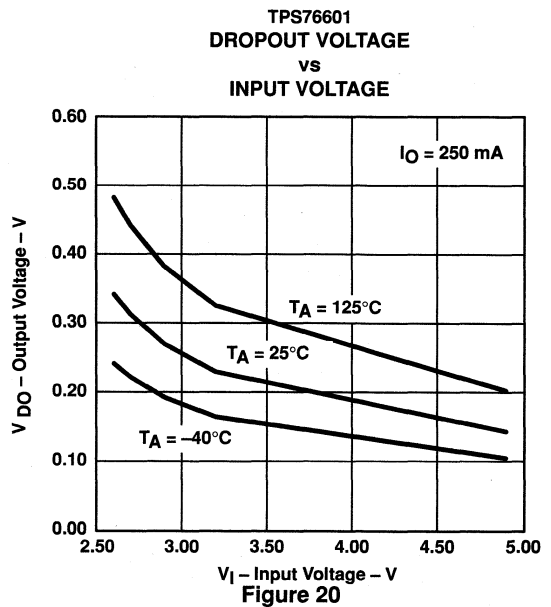


Figure 20

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

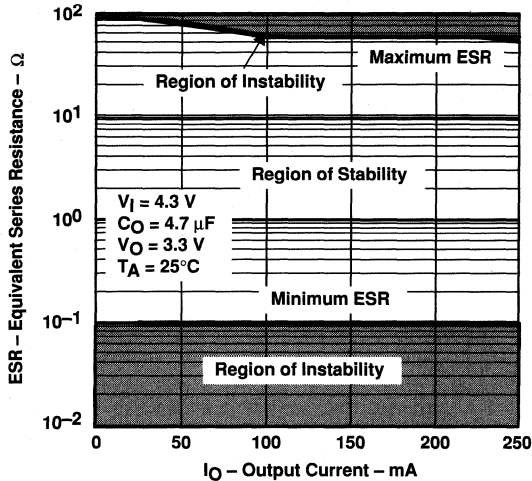


Figure 21

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

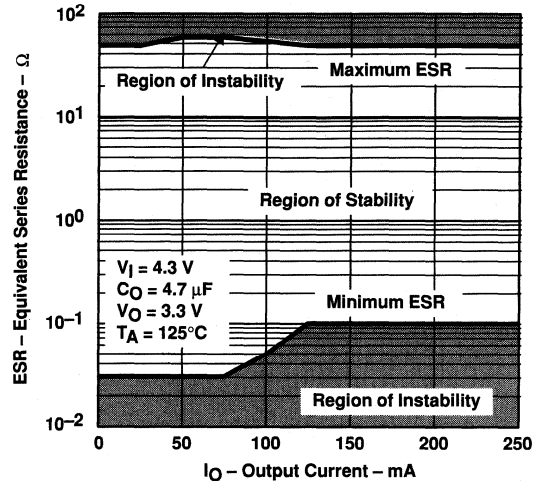


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

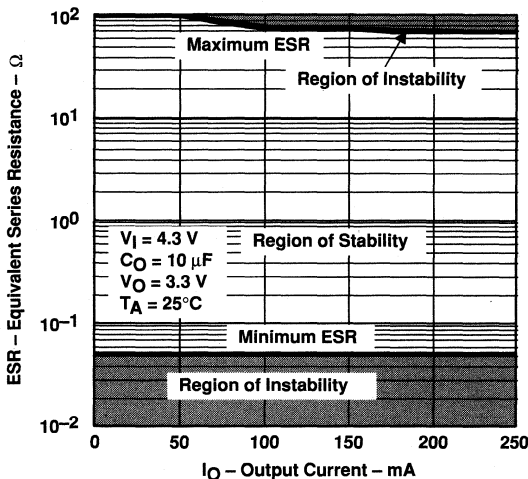


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

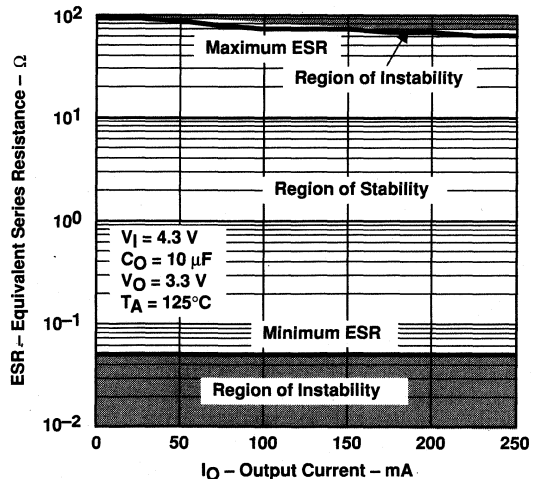


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 ADDED CERAMIC CAPACITANCE

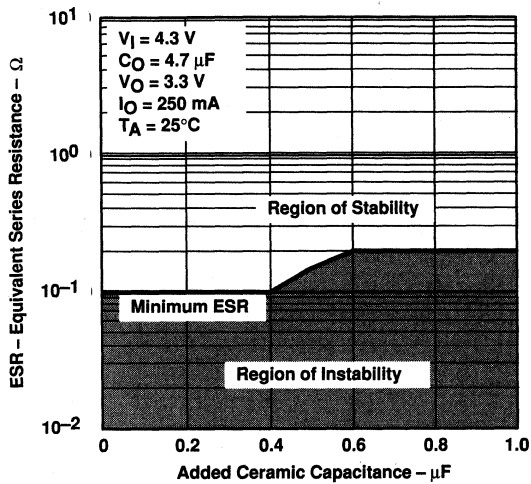


Figure 25

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 ADDED CERAMIC CAPACITANCE

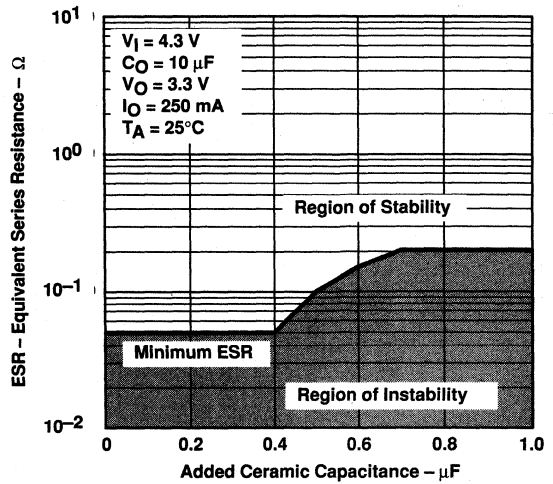


Figure 26

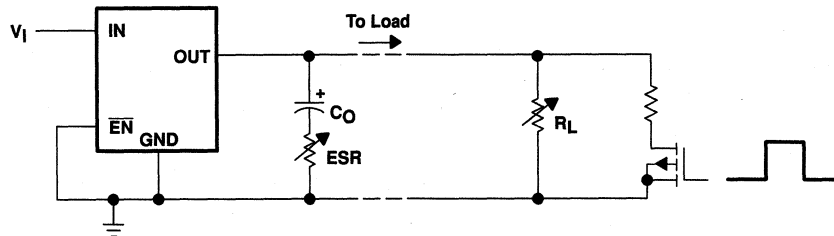


Figure 27. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_0 .

TPS76615, TPS76618, TPS76625, TPS76627
TPS76628, TPS76630, TPS76633, TPS76650, TPS76601
ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS
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APPLICATION INFORMATION

The TPS766xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76601 (adjustable from 1.25 V to 5.5 V).

device operation

The TPS766xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS766xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS766xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS766xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1 μ A (typ). If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160 μ s.

minimum load requirements

The TPS766xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 29. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS766xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS766xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 μ F and the ESR (equivalent series resistance) must be between 300-m Ω and 20- Ω . Capacitor values 4.7 μ F or larger are acceptable, provided the ESR is less than 20 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

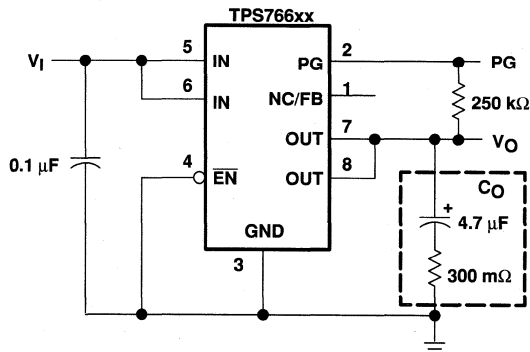


Figure 28. Typical Application Circuit (Fixed Versions)

programming the TPS76601 adjustable LDO regulator

The output voltage of the TPS76601 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

$$V_{ref} = 1.224 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

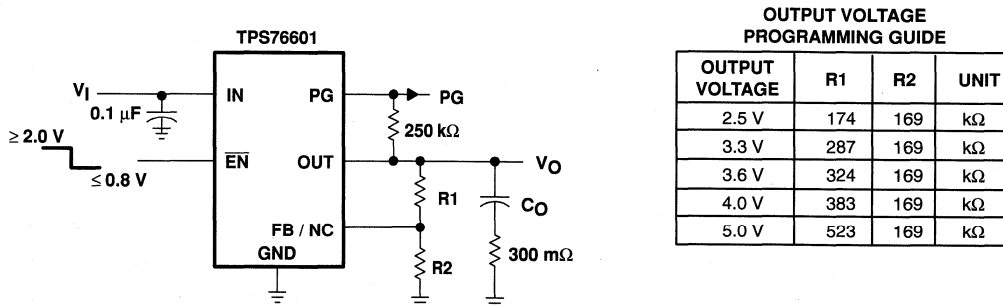


Figure 29. TPS76601 Adjustable LDO Regulator Programming

**TPS76615, TPS76618, TPS76625, TPS76627
TPS76628, TPS76630, TPS76633, TPS76650, TPS76601
ULTRA LOW QUIESCENT CURRENT 250-mA LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

power-good indicator

The TPS766xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS766xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS766xx also features internal current limiting and thermal protection. During normal operation, the TPS766xx limits output current to approximately 0.8 μ A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

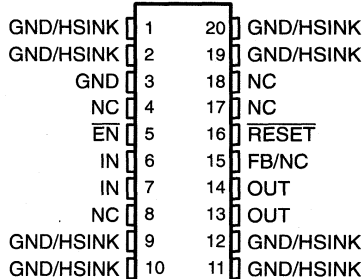
SLVS208C – MAY 1999 – REVISED SEPTEMBER 1999

- 1 A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76750)
- Ultra Low 85 μ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

description

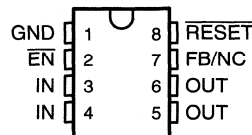
This device is designed to have a fast transient response and be stable with 10- μ F low ESR capacitors. This combination provides high performance at a reasonable cost.

**PWP PACKAGE
(TOP VIEW)**

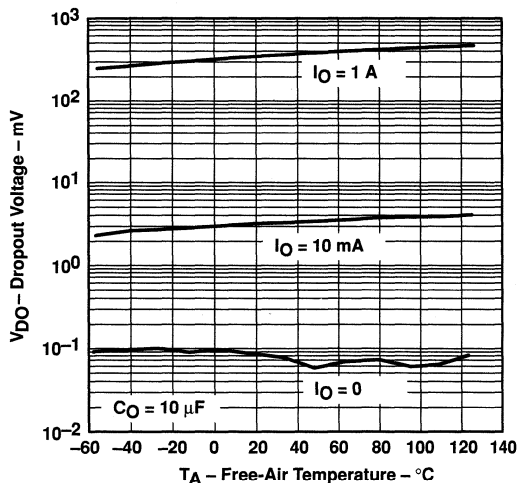


NC – No internal connection

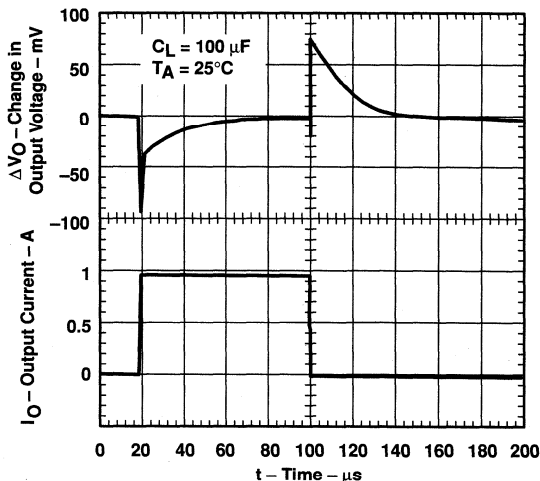
**D PACKAGE
(TOP VIEW)**



**TPS76733
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



**TPS76733
LOAD TRANSIENT RESPONSE**



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**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

SLVS208C – MAY 1999 – REVISED SEPTEMBER 1999

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = 25^\circ\text{C}$.

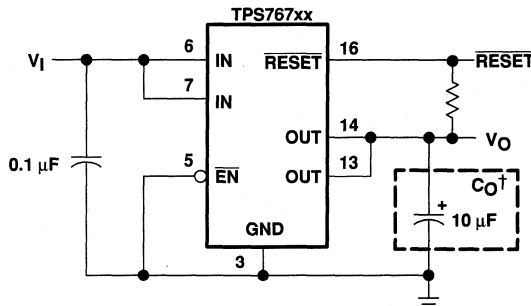
The $\overline{\text{RESET}}$ output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in 8 pin SOIC and 20 pin PWP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES	
	TYP	TSSOP (PWP)	SOIC (D)
-40°C to 125°C	5.0	TPS76750Q	TPS76750Q
	3.3	TPS76733Q	TPS76733Q
	3.0	TPS76730Q	TPS76730Q
	2.8	TPS76728Q	TPS76728Q
	2.7	TPS76727Q	TPS76727Q
	2.5	TPS76725Q	TPS76725Q
	1.8	TPS76718Q	TPS76718Q
	1.5	TPS76715Q	TPS76715Q
	Adjustable 1.5 V to 5.5 V	TPS76701Q	TPS76701Q

The TPS76701 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76701QDR).

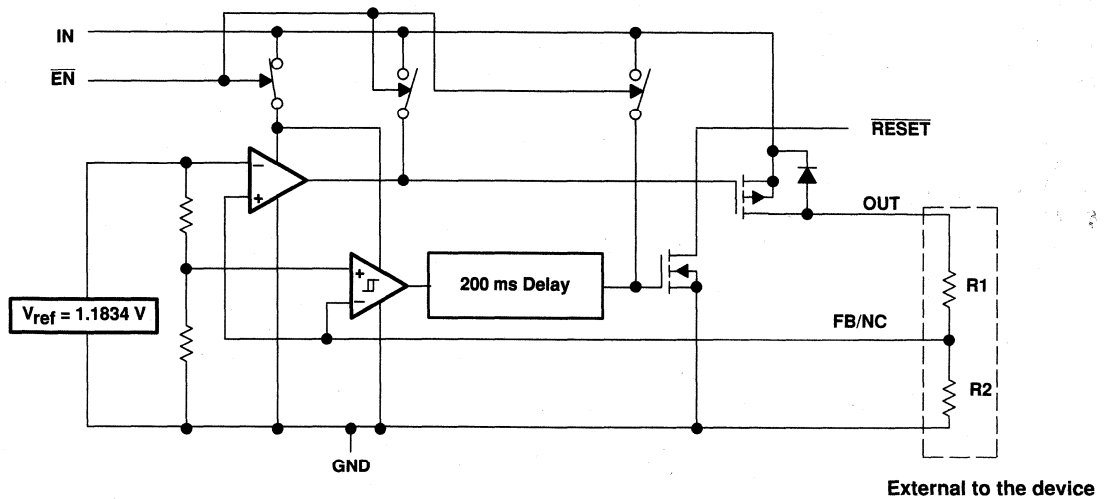


† See application information section for capacitor selection details.

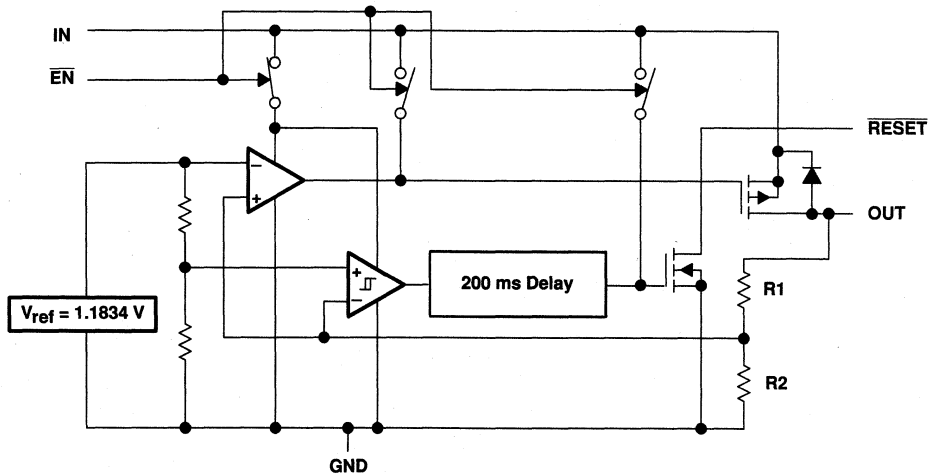
Figure 1. Typical Application Configuration (For Fixed Output Options)

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS
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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
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Terminal Functions – SOIC Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
RESET	8	O	RESET output

Terminal Functions – PWP Package

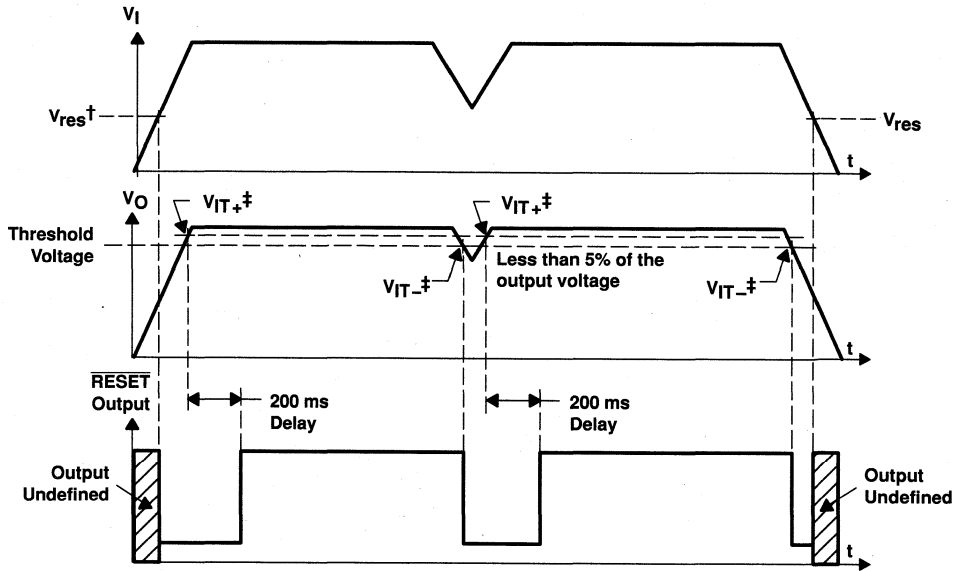
TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
RESET	16	O	RESET output



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timing diagram



$^\dagger V_{res}$ is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

$^\ddagger V_{IT-}$ Trip voltage is typically 5% lower than the output voltage ($95\%V_O$). V_{IT-} to V_{IT+} is the hysteresis voltage.

**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	-0.3 V to 13.5 V
Voltage range at \overline{EN}	-0.3 V to $V_I + 0.3$ V
Maximum \overline{RESET} voltage	16.5 V
Peak output current	Internally limited
Output voltage, V_O (OUT, FB)	7 V
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in x 5-in PCB, 1 oz. copper, 2-in x 2-in coverage (4 in²).

|| This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in x 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I *	2.7	10	V
Output voltage range, V_O	1.5	5.5	V
Output current, I_O (Note 1)	0	1.0	A
Operating virtual junction temperature, T_J (Note 1)	-40	125	°C

* To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
 NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Output voltage (10 μA to 1 A load) (see Note 2)	TPS76701	$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$	V_O			V		
		$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	0.98 V_O				1.02 V_O	
	TPS76715	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.5					
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.470				1.530	
	TPS76718	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.8					
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.764				1.836	
	TPS76725	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.5					
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.450				2.550	
	TPS76727	$T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.7					
		$T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.646				2.754	
	TPS76728	$T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.8					
		$T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.744				2.856	
	TPS76730	$T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.0					
		$T_J = -40^\circ\text{C}$ to 125°C , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.940				3.060	
	TPS76733	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.3					
		$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.234				3.366	
TPS76750	$T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	5.0						
	$T_J = -40^\circ\text{C}$ to 125°C , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	4.900			5.100			
Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$, (see Note 2)		$10 \mu\text{A} < I_O < 1 \text{ A}$, $T_J = 25^\circ\text{C}$	85			μA		
		$I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C	125					
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$	0.01			%/V		
Load regulation			3			mV		
Output noise voltage		BW = 300 Hz to 50 kHz, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	190			μV_{rms}		
Output current Limit		$V_O = 0 \text{ V}$	1.7		2	A		
Thermal shutdown junction temperature			150			$^\circ\text{C}$		
Standby current		$\overline{\text{EN}} = V_I$, $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_I < 10 \text{ V}$	1			μA		
		$\overline{\text{EN}} = V_I$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_I < 10 \text{ V}$	10			μA		
FB input current	TPS76701	FB = 1.5 V	2			nA		
High level enable input voltage			1.7			V		
Low level enable input voltage			0.9			V		
Power supply ripple rejection (see Note 2)		$f = 1 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	60			dB		
Reset	Minimum input voltage for valid $\overline{\text{RESET}}$		$I_O(\overline{\text{RESET}}) = 300\mu\text{A}$			1.1	V	
	Trip threshold voltage		V_O decreasing			92	98	% V_O
	Hysteresis voltage		Measured at V_O			0.5		% V_O
	Output low voltage		$V_I = 2.7 \text{ V}$, $I_O(\overline{\text{RESET}}) = 1 \text{ mA}$	0.15		0.4	V	
	Leakage current		$V(\overline{\text{RESET}}) = 5 \text{ V}$	1			μA	
	RESET time-out delay			200			ms	

NOTE 2: Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10V.

**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(typ)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input current (EN)		$\overline{EN} = 0\text{ V}$		-1	0	1	μA
		$\overline{EN} = V_i$		-1		1	
Dropout voltage (See Note 4)	TPS76728	$I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		500			mV
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$		825			
	TPS76730	$I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		450			
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$		675			
	TPS76733	$I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		350			
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$		575			
	TPS76750	$I_O = 1\text{ A}$, $T_J = 25^\circ\text{C}$		230			
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$		380			

NOTES: 3. If $V_O \leq 1.8\text{ V}$ then $V_{imax} = 10\text{ V}$, $V_{imin} = 2.7\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{imax} - 2.7\text{ V})}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$ then $V_{imax} = 10\text{ V}$, $V_{imin} = V_O + 1\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{imax} - (V_O + 1\text{ V}))}{100} \times 1000$$

4. I_N voltage equals $V_O(\text{Typ}) - 100\text{ mV}$; TPS76701 output voltage set to 3.3 V nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

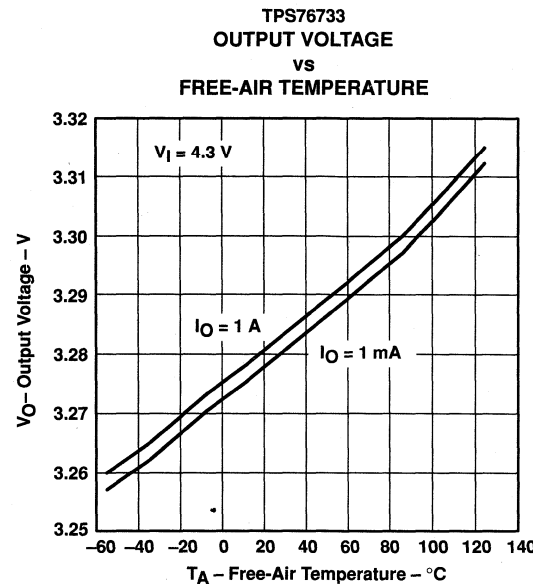
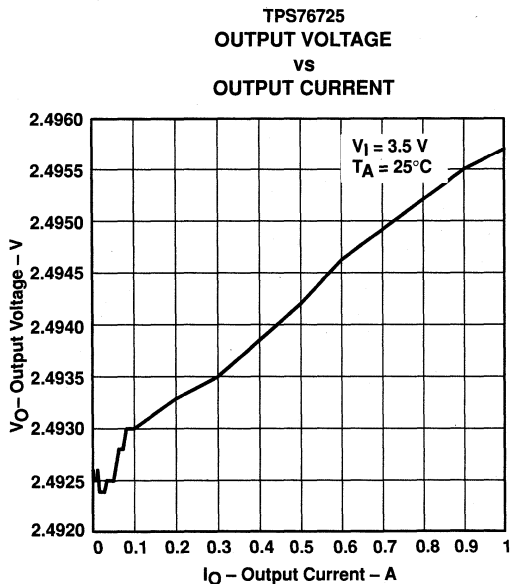
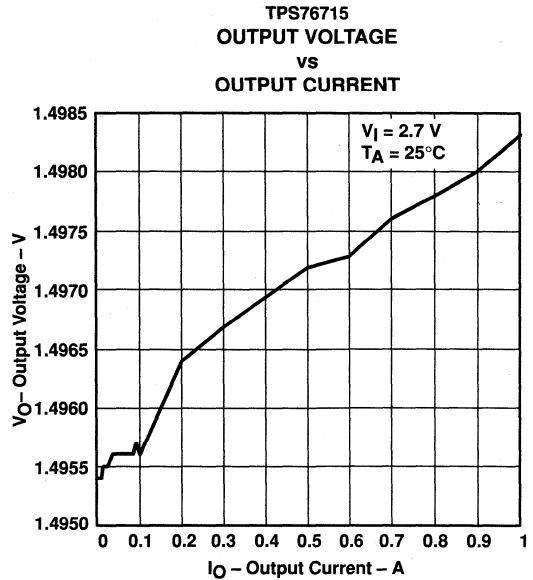
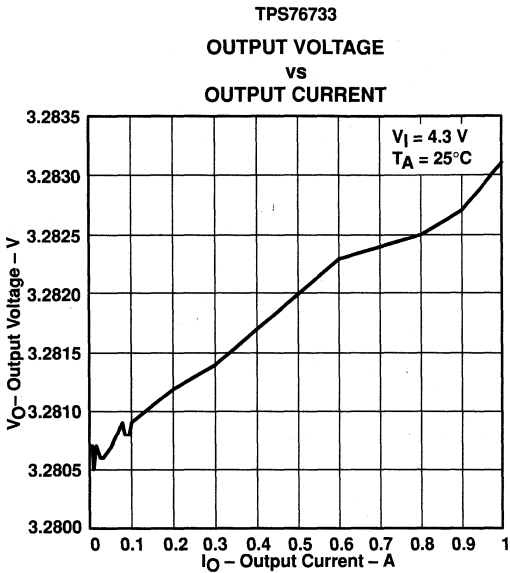
			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8, 9
	Power supply ripple rejection	vs Frequency	10
	Output noise	vs Frequency	11
Z_o	Output impedance	vs Frequency	12
V_{DO}	Dropout voltage	vs Free-air temperature	13
		Line transient response	14, 16
	Load transient response		15, 17
	Output voltage	vs Time	18
	Dropout voltage	vs Input voltage	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24



**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

TPS76715
OUTPUT VOLTAGE
 vs
FREE-AIR TEMPERATURE

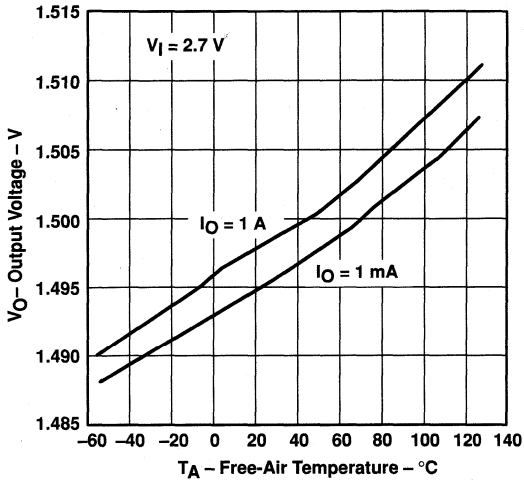


Figure 6

TPS76725
OUTPUT VOLTAGE
 vs
FREE-AIR TEMPERATURE

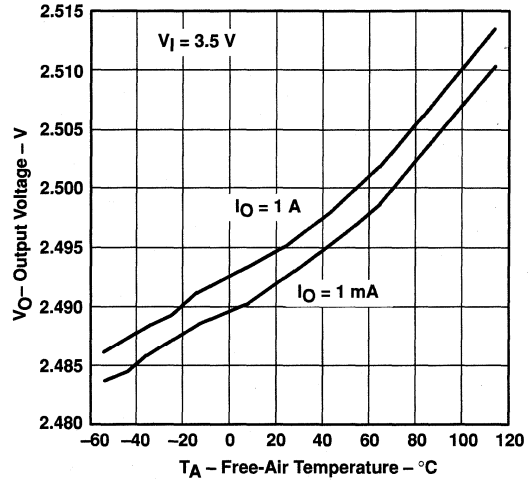


Figure 7

TPS76733
GROUND CURRENT
 vs
FREE-AIR TEMPERATURE

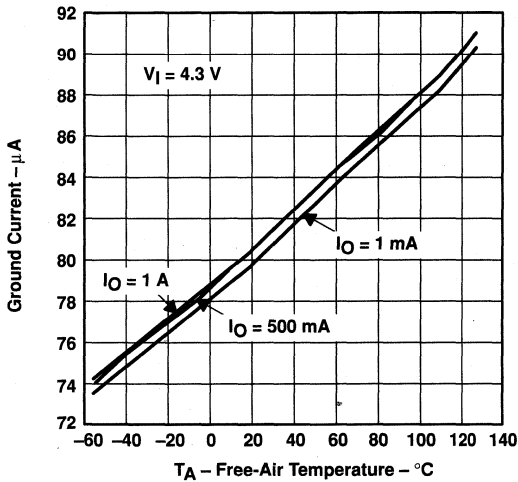


Figure 8

TPS76715
GROUND CURRENT
 vs
FREE-AIR TEMPERATURE

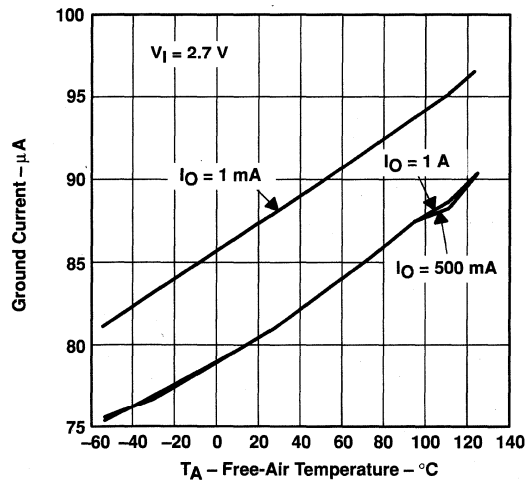


Figure 9

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

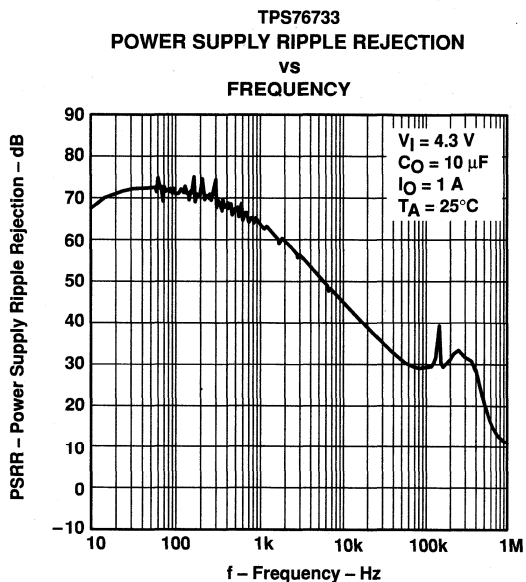


Figure 10

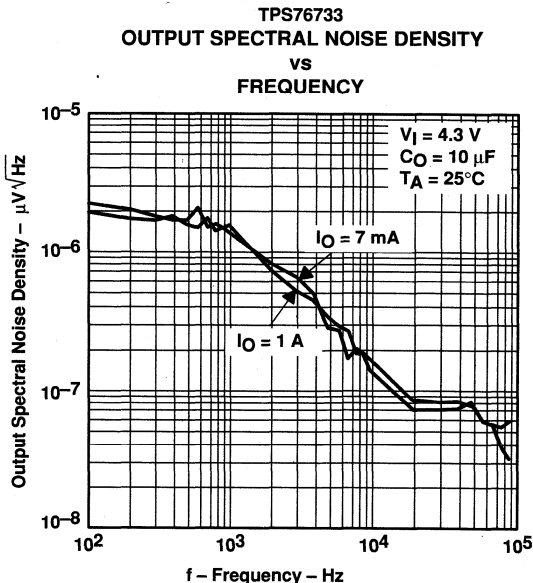


Figure 11

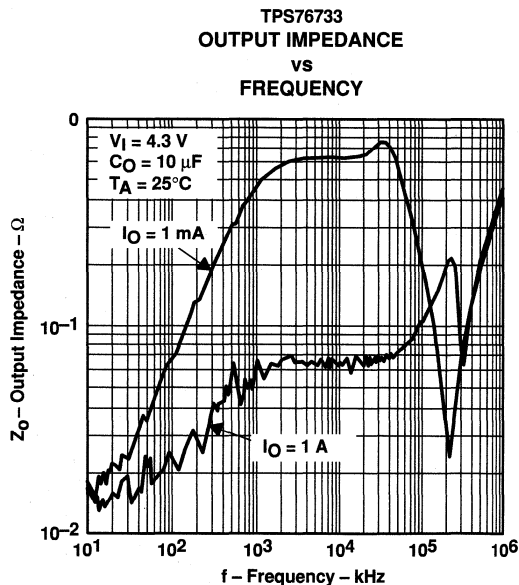


Figure 12

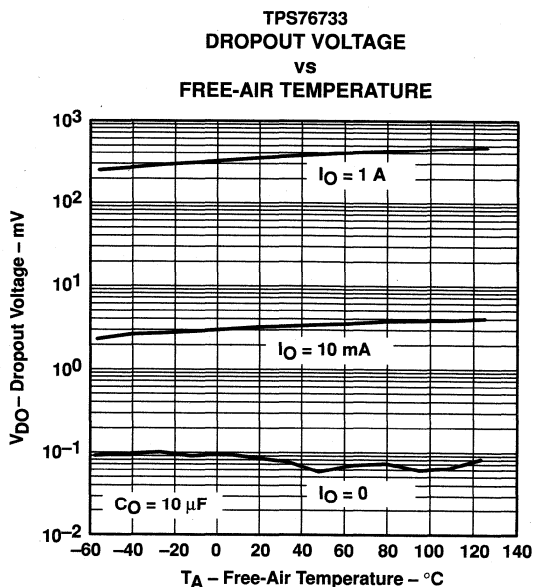


Figure 13

TYPICAL CHARACTERISTICS

TPS76715
LINE TRANSIENT RESPONSE

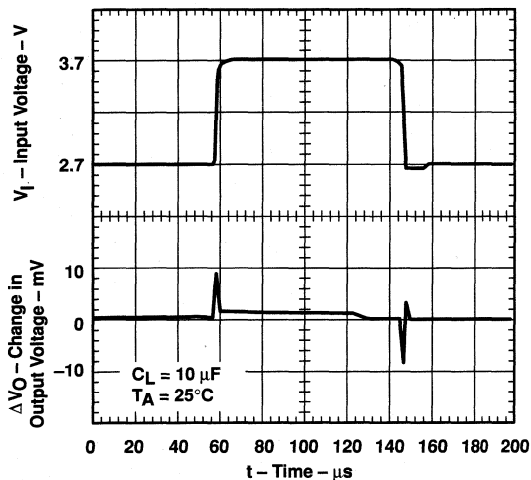


Figure 14

TPS76715
LOAD TRANSIENT RESPONSE

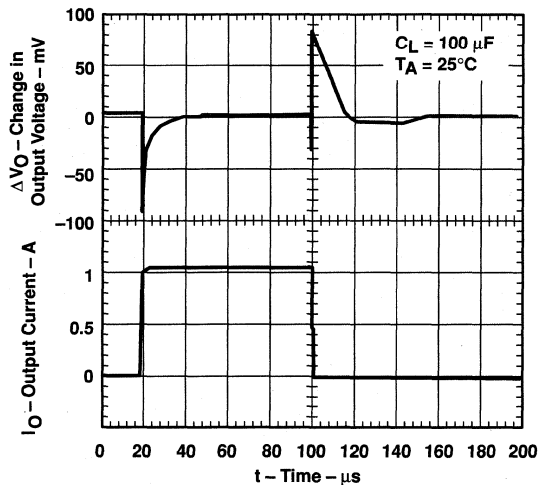


Figure 15

TPS76733
LINE TRANSIENT RESPONSE

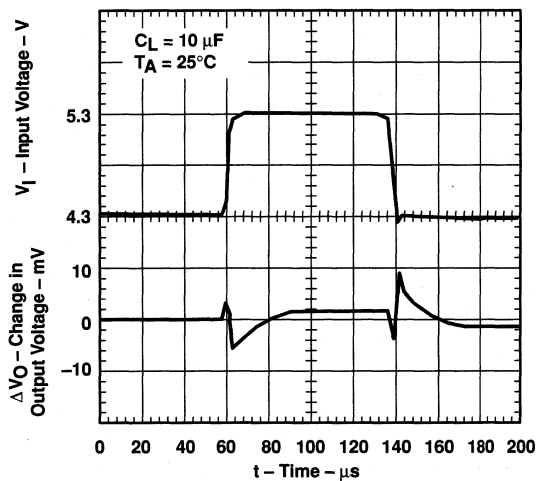


Figure 16

TPS76733
LOAD TRANSIENT RESPONSE

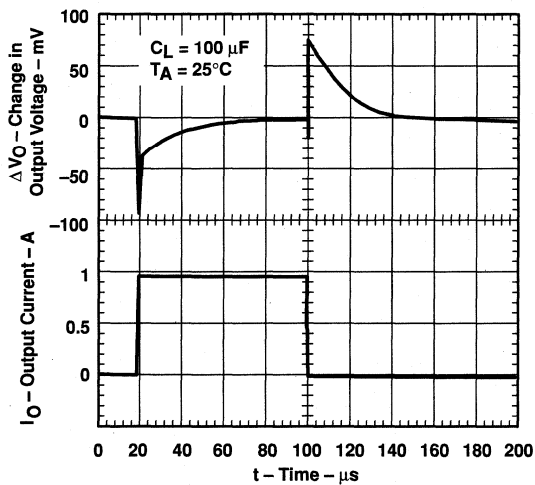


Figure 17

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
 TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

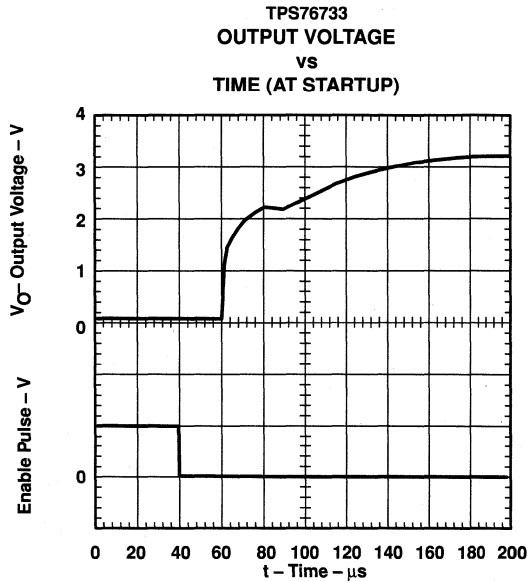


Figure 18

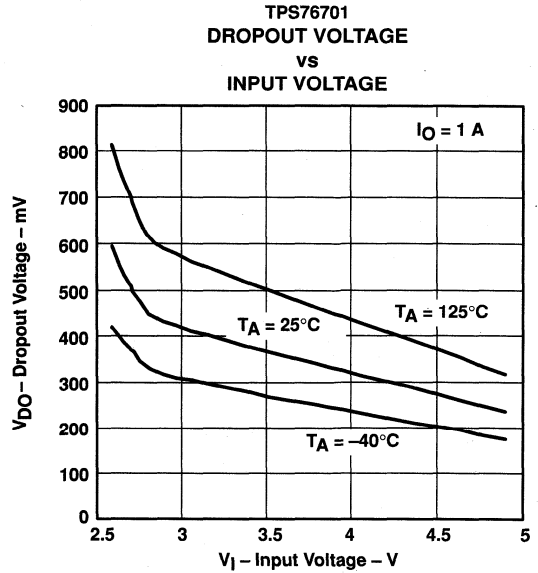


Figure 19

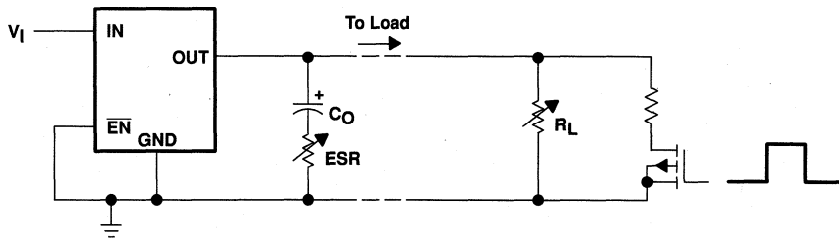


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

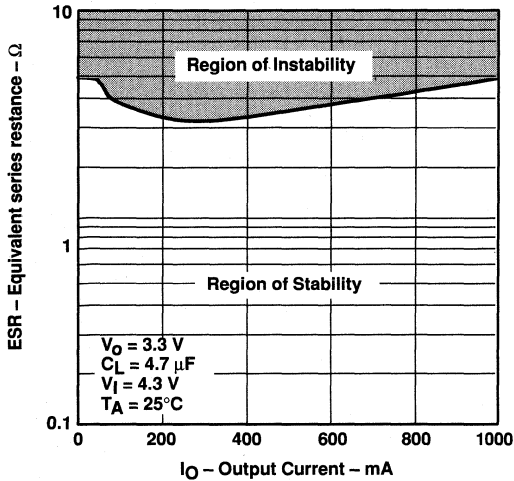


Figure 21

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

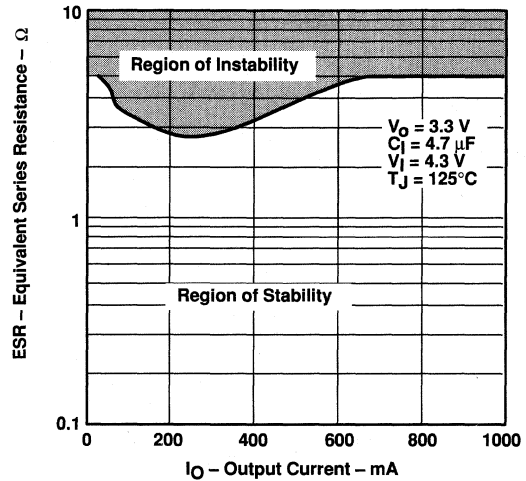


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

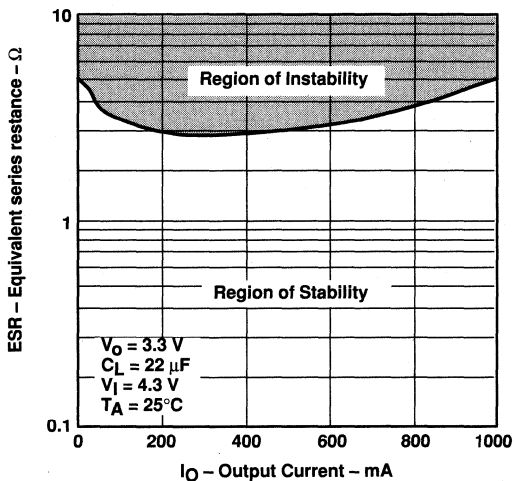


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

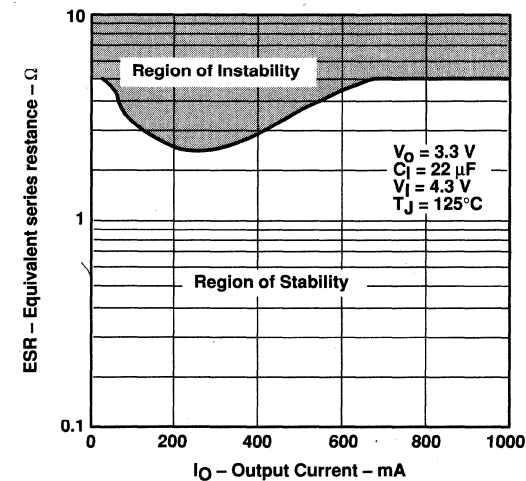


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

SLVS208C – MAY 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

device operation

The TPS767xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS767xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μ A. If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μ s.

minimum load requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μ F and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μ F or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 μ F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.



APPLICATION INFORMATION

external capacitor requirements (continued)

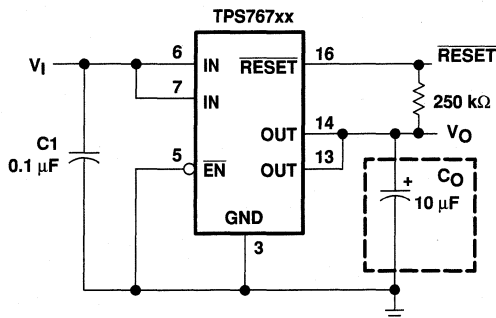


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS76701 adjustable LDO regulator

The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

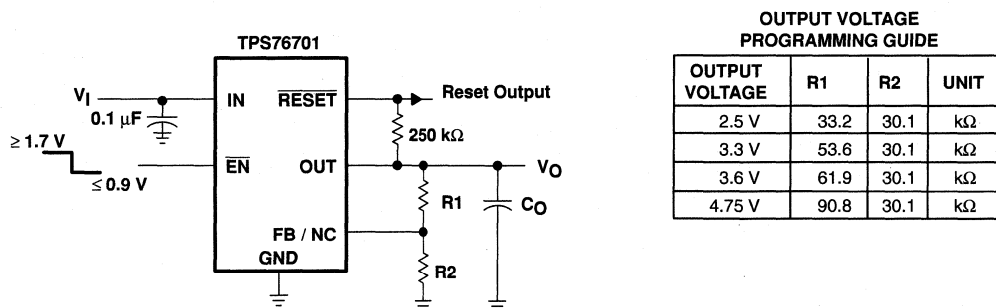


Figure 26. TPS76701 Adjustable LDO Regulator Programming

TPS76715Q, TPS76718Q, TPS76725Q, TPS76727Q
TPS76728Q, TPS76730Q, TPS76733Q, TPS76750Q, TPS76701Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

SLVS208C – MAY 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

reset indicator

The TPS767xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

regulator protection

The TPS767xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\text{max})}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\text{max})}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}}$$

Where

$T_{J(\text{max})}$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

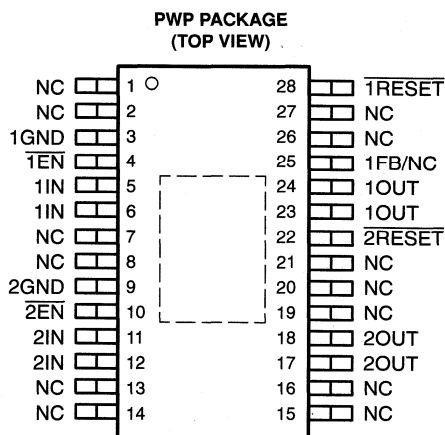
Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.



TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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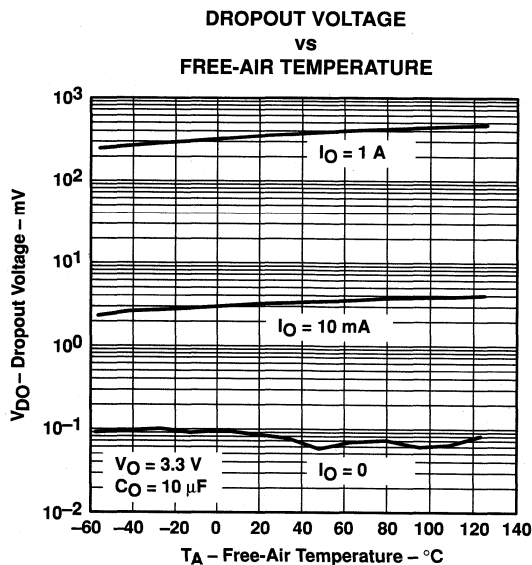
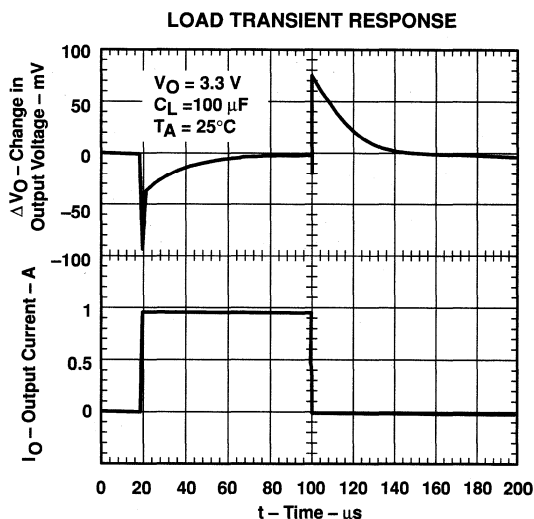
- Dual Output Voltages for Split-Supply Applications
- Output Current Range of 0 mA to 1.0 A Per Regulator
- 3.3-V/2.5-V, 3.3-V/1.8-V, and 3.3-V/Adjustable Output
- Fast-Transient Response
- 2% Tolerance Over Load and Temperature
- Dropout Voltage Typically 350 mV at 1 A
- Ultra Low 85 μ A Typical Quiescent Current
- 1 μ A Quiescent Current During Shutdown
- Dual Open Drain Power-On Reset With 200-ms Delay for Each Regulator
- 28-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection for Each Regulator



NC – No internal connection

description

The TPS767D3xx family of dual voltage regulators offers fast transient response, low dropout voltages and dual outputs in a compact package and incorporating stability with 10- μ F low ESR output capacitors.



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This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

**TEXAS
INSTRUMENTS**

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TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

The TPS767D3xx family of dual voltage regulators is designed primarily for DSP applications. These devices can be used in any mixed-output voltage application, with each regulator supporting up to 1 A. Dual active-low reset signals allow resetting of core-logic and I/O separately.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 350 mV at an output current of 1 A for the TPS767D325) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = 25^\circ\text{C}$.

The $\overline{\text{RESET}}$ output of the TPS767D3xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767D3xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767D3xx is offered in 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767D3xx family is available in 28 pin PWP TSSOP package. They operate over a junction temperature range of -40°C to 125°C .

AVAILABLE OPTIONS

T_A	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
-40°C to 125°C	Adj (1.5 – 5.5 V)	3.3 V	TPS767D301PWP
	1.8 V	3.3 V	TPS767D318PWP
	2.5 V	3.3 V	TPS767D325PWP

The TPS767D301 is adjustable using an external resistor divider (see application information). The PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS767D301PWPR).

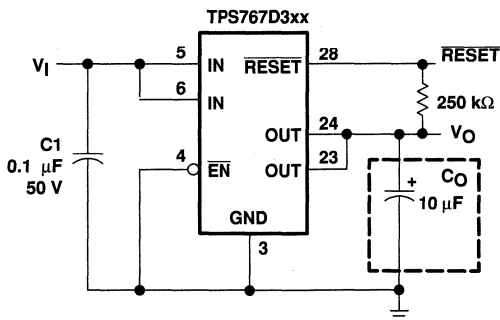
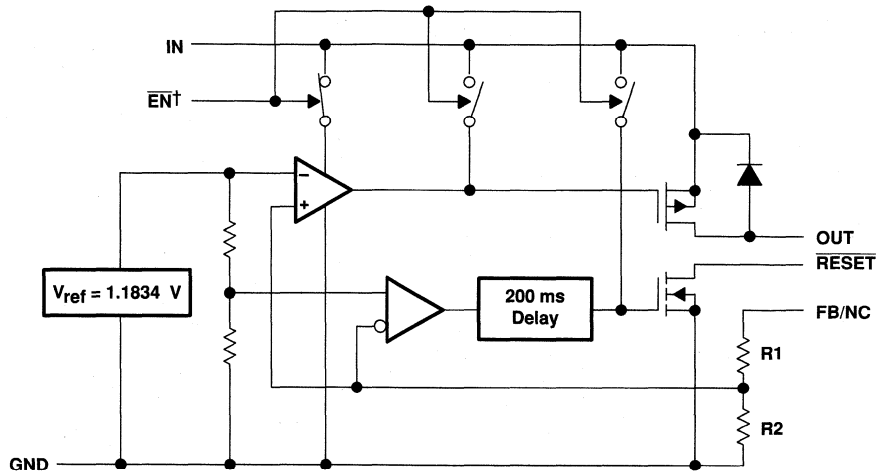


Figure 1. Typical Application Circuit (Fixed Versions) for Single Channel

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

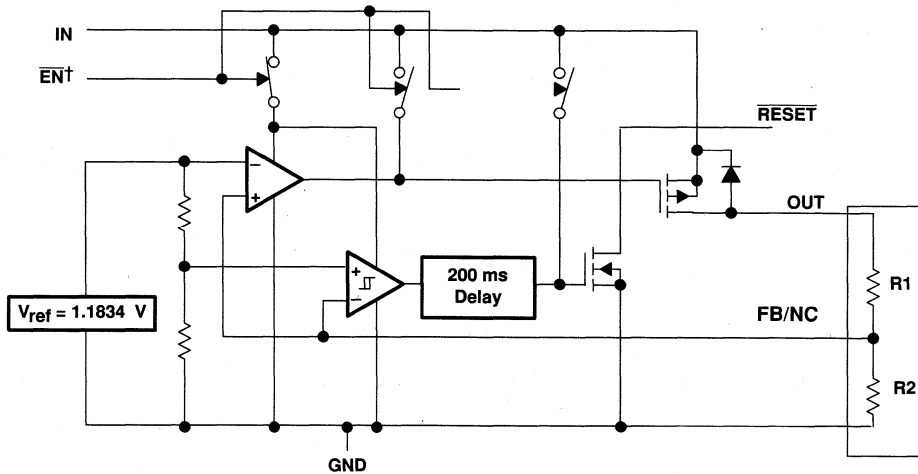
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functional block diagram—fixed-voltage version (for each LDO)



† Switch positions shown with \overline{EN} low (active).

functional block diagram—adjustable version (for each LDO)



† Switch positions shown with \overline{EN} low (active).

External to the device

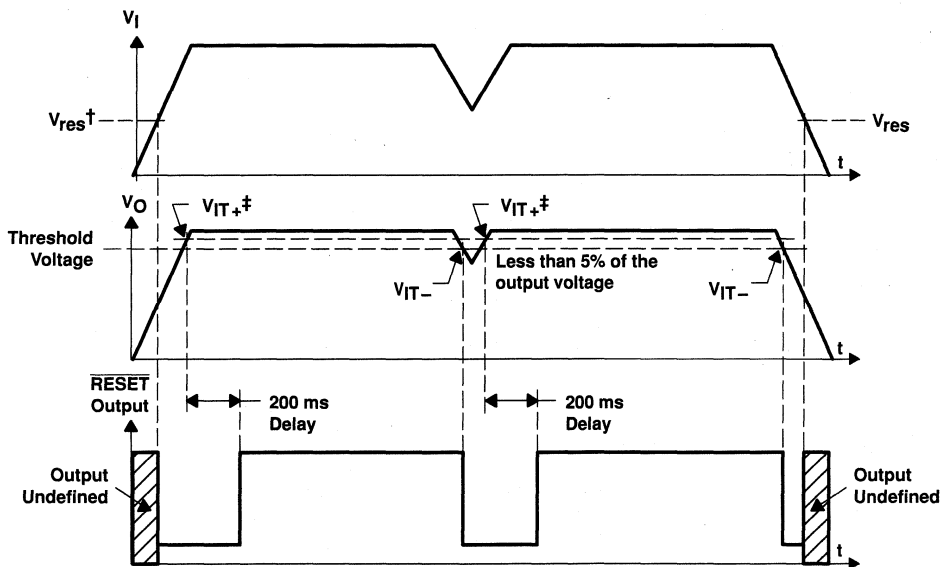
TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
1GND	3		Regulator #1 ground
1EN	4	I	Regulator #1 enable
1IN	5, 6	I	Regulator #1 input supply voltage
2GND	9		Regulator #2 ground
2EN	10	I	Regulator #2 enable
2IN	11, 12	I	Regulator #2 input supply voltage
2OUT	17, 18	O	Regulator #2 output voltage
2RESET	22	O	Regulator #2 reset signal
1OUT	23, 24	O	Regulator #1 output voltage
1FB/NC	25	I	Regulator #1 output voltage feedback for adjustable and no connect for fixed output
1RESET	28	O	Regulator #1 reset signal
NC	1, 2, 7, 8, 13–16, 19, 20, 21, 26, 27		No connection

timing diagram



† V_{res} is the minimum input voltage for a valid \overline{RESET} . The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT-} Trip voltage is typically 5% lower than the output voltage ($95\%V_O$)

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range‡, V_I	-0.3 V to 13.5 V
Input voltage range, V_I (1IN, 2IN, \overline{EN})	-0.3 V to $V_I + 0.3$ V
Output voltage, V_O (1OUT, 2OUT)	7 V
Output voltage, V_O (RESET)	16.5 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
		POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
PWP†	0	3.58 W	35.8 mW/°C	1.97 W	1.43 W
	250	5.07 W	50.7 mW/°C	2.79 W	2.03 W

† This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on 4-in x 4-in ground layer. For more information, refer to TI technical brief literature number SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I # (1IN, 2IN)	2.7	10	V
Output current for each LDO, I_O (Note 1)	0	1.0	A
Output voltage range, V_O (1OUT, 2OUT)	1.5	5.5	V
Operating virtual junction temperature, T_J	-40	125	°C

To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics, $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (see Note 2)	Adjustable	$1.5\text{ V} \leq V_O \leq 5.5\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	V_O			V
			$T_J = -40^\circ\text{C}$ to 125°C	$0.98V_O$	$1.02V_O$		
	1.8 V Output	$2.8\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	1.8			
			$T_J = -40^\circ\text{C}$ to 125°C	1.764	1.836		
	2.5 V Output	$3.5\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	2.5			
			$T_J = -40^\circ\text{C}$ to 125°C	2.45	2.55		
3.3 V Output	$4.3\text{ V} < V_I < 10\text{ V}$, $10\text{ }\mu\text{A} < I_O < 1\text{ A}$	$T_J = 25^\circ\text{C}$	3.3				
		$T_J = -40^\circ\text{C}$ to 125°C	3.234	3.366			
Quiescent current (GND current) for each LDO (see Note 2)		$10\text{ }\mu\text{A} < I_O < 1\text{ A}$, $T_J = 25^\circ\text{C}$	$\overline{EN} = 0\text{V}$,	85			μA
		$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C	$\overline{EN} = 0\text{V}$,	125			
Output voltage line regulation for each LDO ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1\text{ V} < V_I \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$		0.01			%/V
Output noise voltage		BW = 300 Hz to 50 kHz, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$		190			μVrms
Output current Limit for each LDO		$V_O = 0\text{ V}$		1.7	2		A
Thermal shutdown junction temperature				150			$^\circ\text{C}$
Standby current for each LDO		$2.7 < V_I < 10\text{V}$, $T_J = 25^\circ\text{C}$	$\overline{EN} = V_I$,	1			μA
			$\overline{EN} = V_I$,	10			μA
FB input current	Adjustable	FB = 1.5 V		2			nA
High level enable input voltage				2.0			V
Low level enable input voltage				0.8			V
Power supply ripple rejection (see Note 2)		f = 1 KHz, $T_J = 25^\circ\text{C}$, $C_O = 10\text{ }\mu\text{F}$		60			dB
Reset	Minimum input voltage for valid RESET		$I_O(\text{RESET}) = 300\mu\text{A}$		1.1		V
	Trip threshold voltage		V_O decreasing		92	98	% V_O
	Hysteresis voltage		Measured at V_O		0.5		% V_O
	Output low voltage		$V_I = 2.7\text{ V}$, $I_O(\text{RESET}) = 1\text{ mA}$		0.15	0.4	V
	Leakage current		$V(\text{RESET}) = 7\text{ V}$		1		μA
	RESET time-out delay				200		mA

NOTES: 2. Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1\text{ V}$, whichever is greater, maximum IN voltage 10V.

3. If $V_O \leq 1.8\text{ V}$, $V_{\text{imin}} = 2.7\text{ V}$, and $V_{\text{imax}} = 10\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7\text{ V})}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$, $V_{\text{imin}} = V_O + 1\text{ V}$, and $V_{\text{imax}} = 10\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1\text{ V}))}{100} \times 1000$$



TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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**electrical characteristics, $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{EN} = 0$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)
(continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current (EN)	$\overline{EN} = 0\text{ V}$	-1	0	1	μA
	$\overline{EN} = V_I$	-1		1	
Load regulation			3		mV
Dropout voltage (see Note 4)	$V_O = 3.3\text{ V}$, $I_O = 1\text{ A}$	$T_J = 25^\circ\text{C}$	350		mV
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		575	

NOTE 4: I_N voltage equals $V_O(\text{Typ}) - 100\text{ mV}$; Adjustable output voltage set to 3.3V nominal with external resistor divider. 1.8V, and 2.5V dropout voltage is limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	vs Output current	2, 3, 4
	vs Free-air temperature	5, 6, 7
Ground current	vs Free-air temperature	8, 9
Power supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
Dropout voltage	vs Free-air temperature	13
Line transient response		14, 16
Load transient response		15, 17
Output voltage	vs Time	18
Dropout voltage	vs Input voltage	19
Equivalent series resistance (ESR)	vs Output current, $T_A = 25^\circ\text{C}$	21
	vs Output current, $T_J = 125^\circ\text{C}$	22
	vs Output Current, $T_A = 25^\circ\text{C}$	23
	vs Output current, $T_J = 125^\circ\text{C}$	24

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

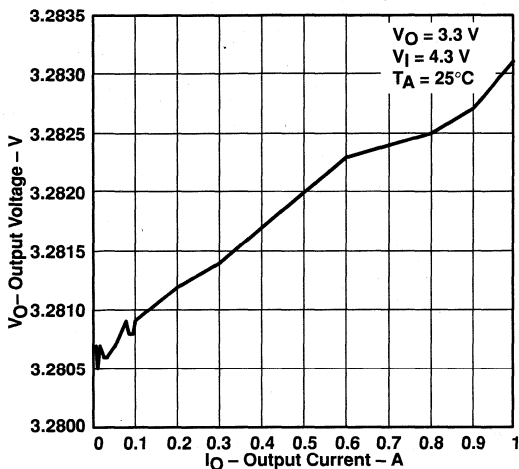


Figure 2

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

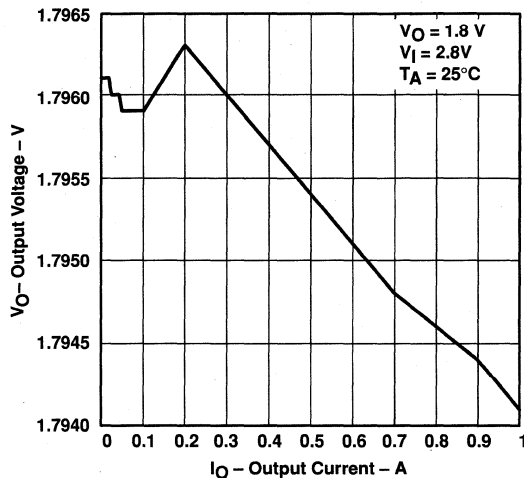


Figure 3

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

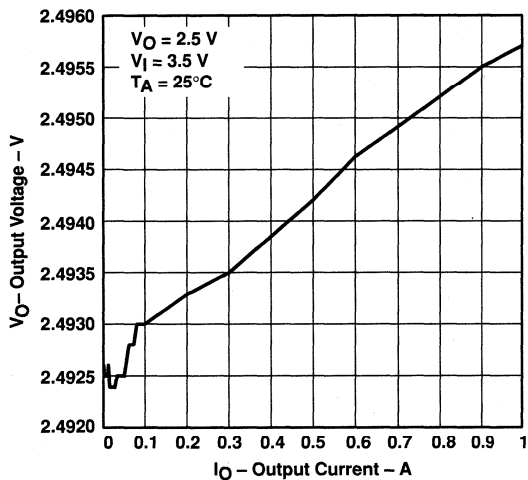


Figure 4

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

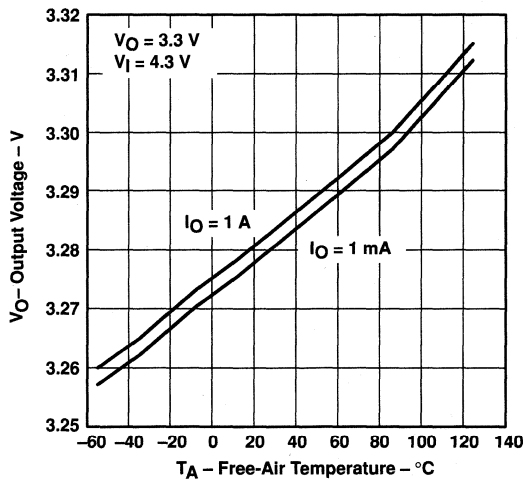


Figure 5

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

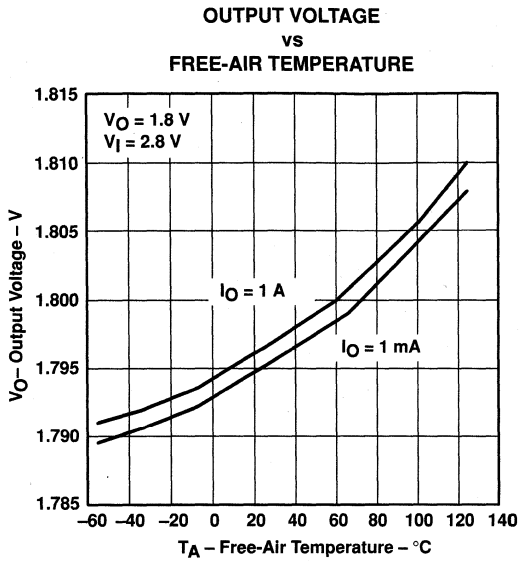


Figure 6

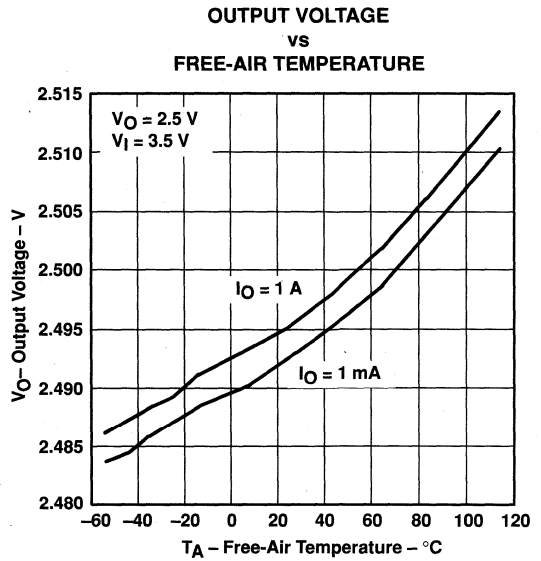


Figure 7

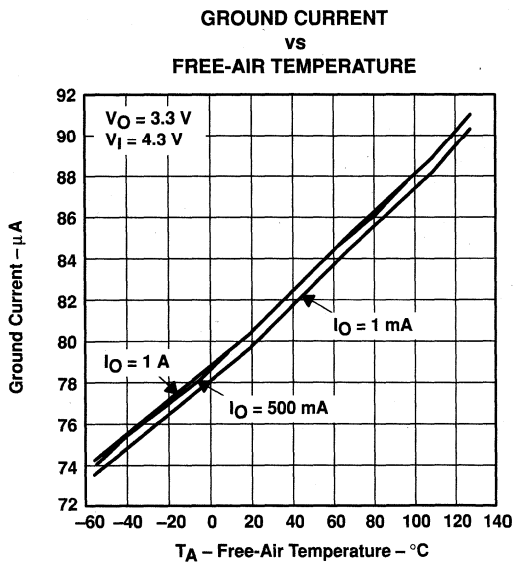


Figure 8

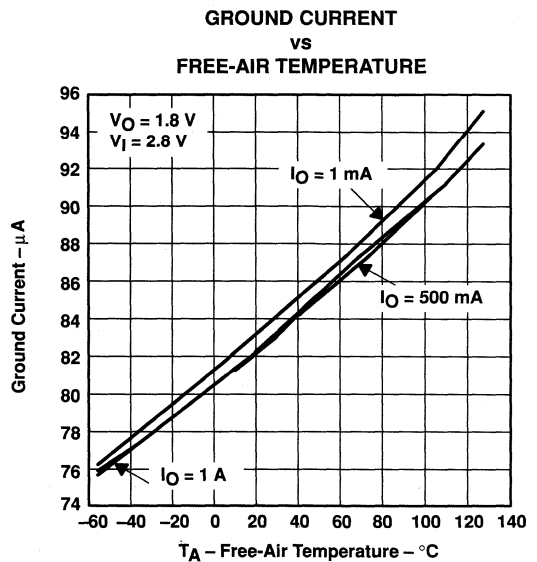


Figure 9

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY**

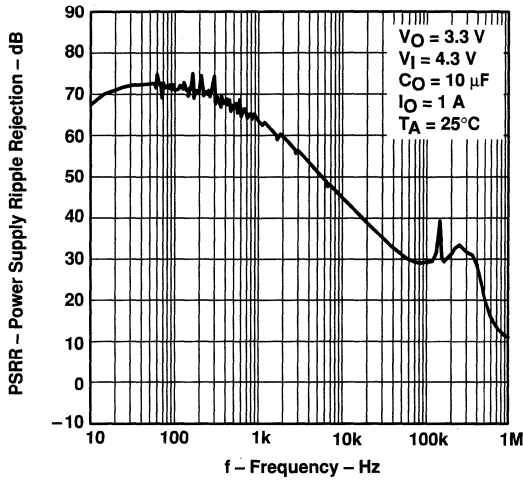


Figure 10

**OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

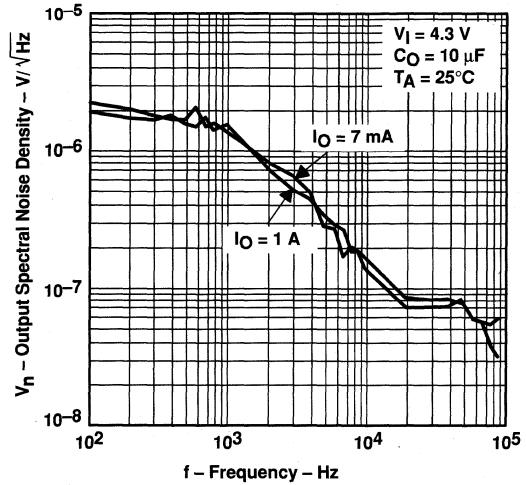


Figure 11

**OUTPUT IMPEDANCE
vs
FREQUENCY**

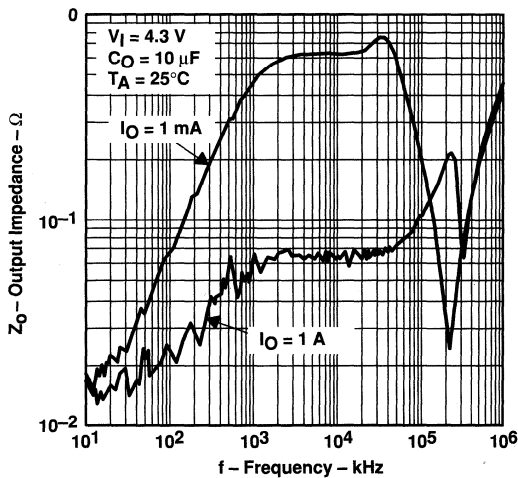


Figure 12

**DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

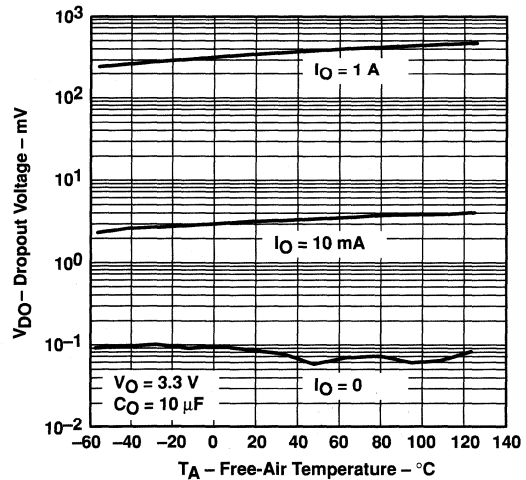


Figure 13

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

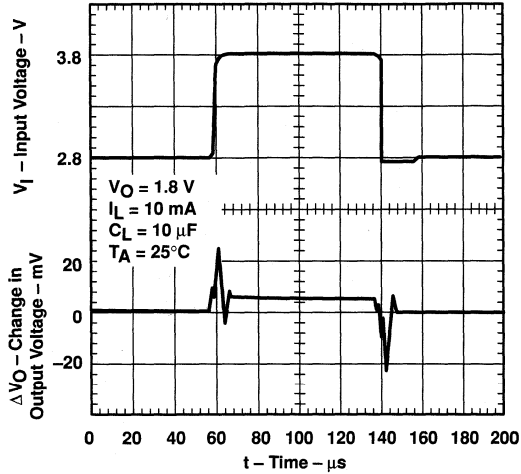


Figure 14

LOAD TRANSIENT RESPONSE

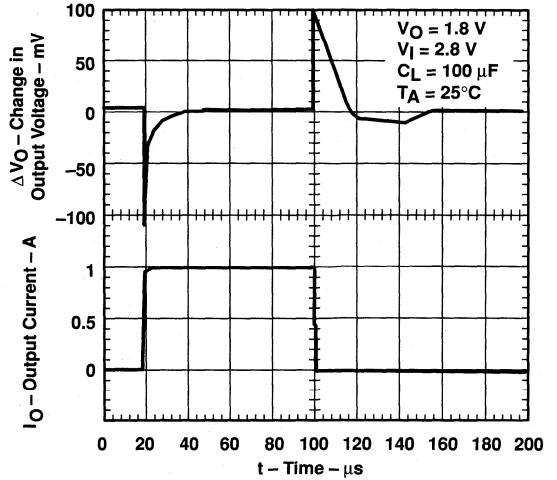


Figure 15

LINE TRANSIENT RESPONSE

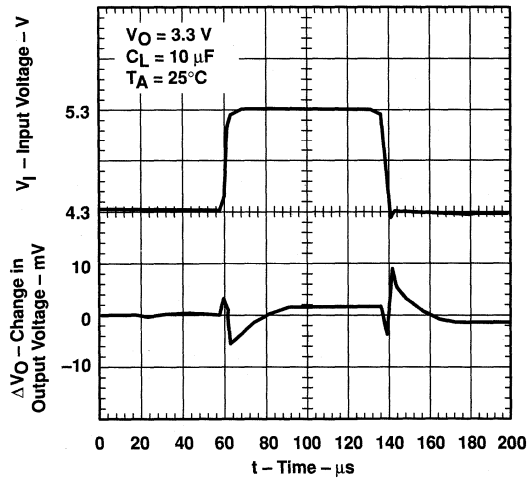


Figure 16

LOAD TRANSIENT RESPONSE

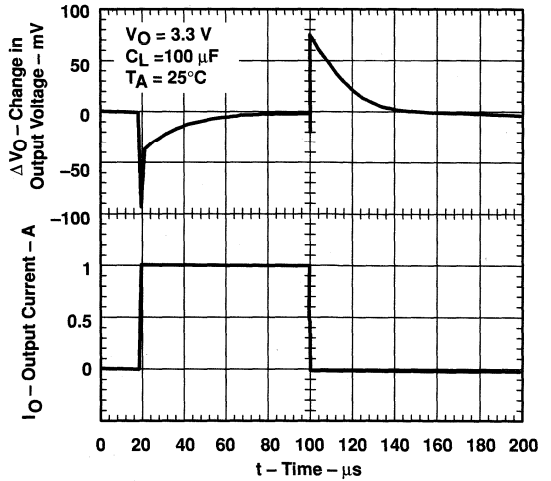


Figure 17

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

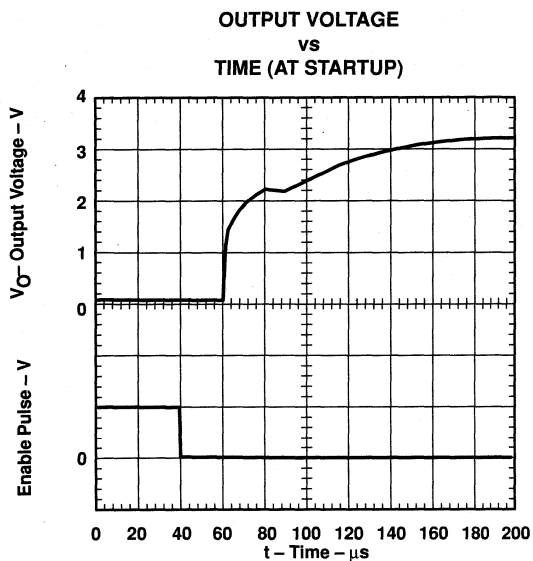


Figure 18

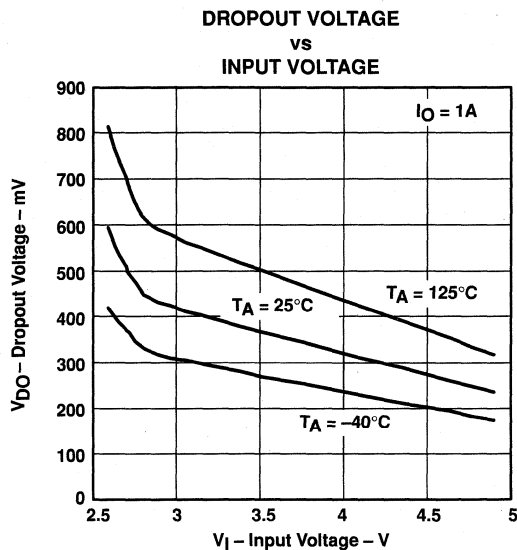


Figure 19

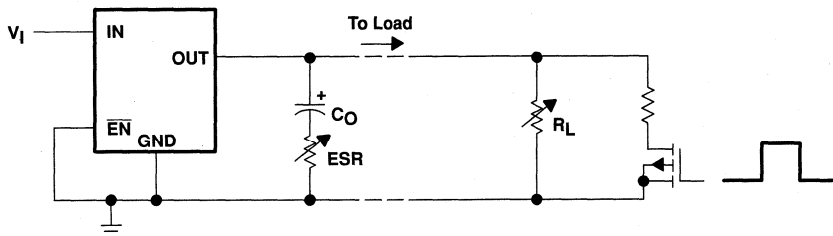


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (fixed output options)

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

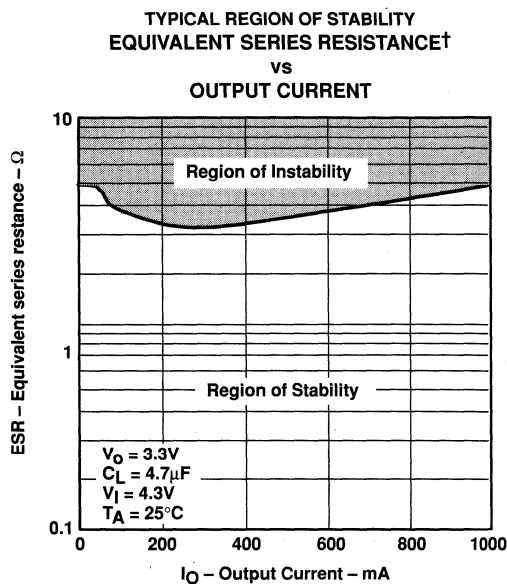


Figure 21

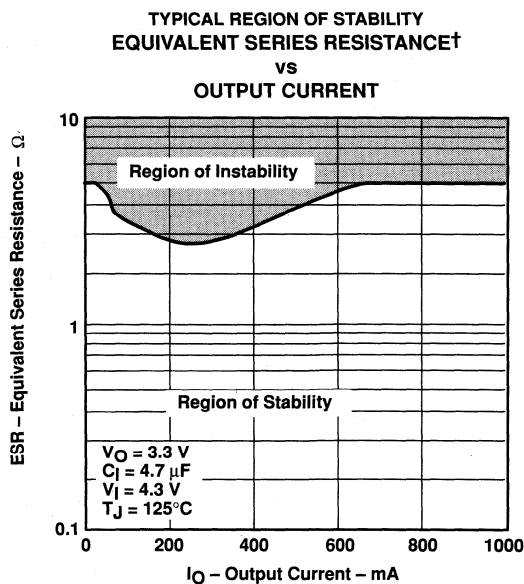


Figure 22

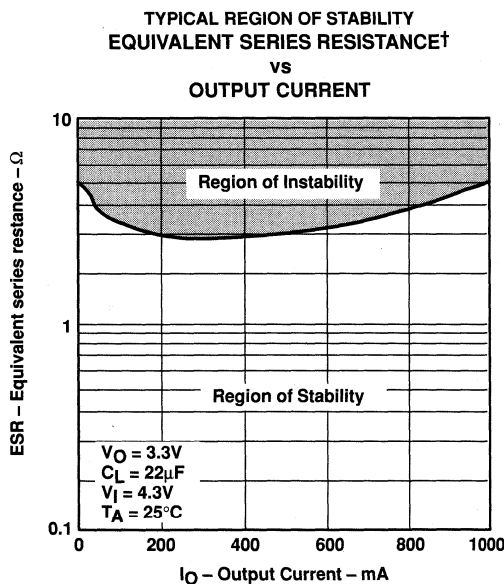


Figure 23

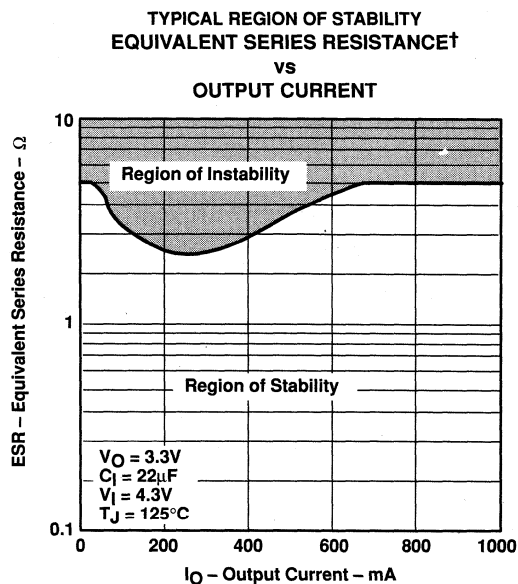


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

The features of the TPS767D3xx family (low-dropout voltage, ultra-low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package have enabled the integration of the dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 25 shows a typical dual-voltage DSP application.

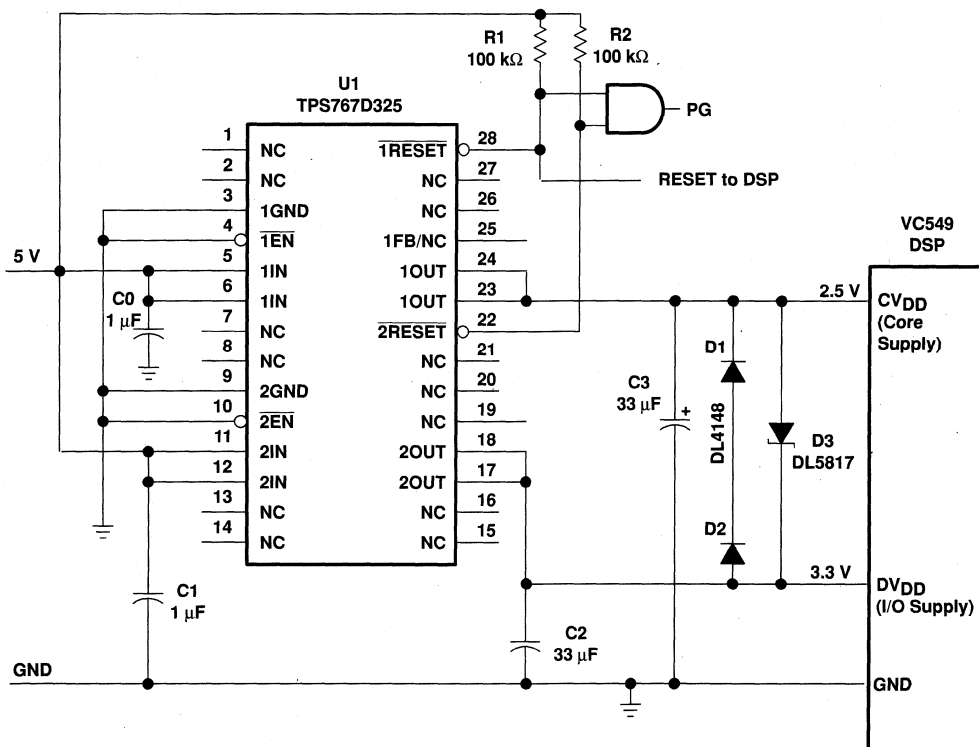


Figure 25. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents.

device operation

The TPS767D3xx features very low quiescent current, which remain virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that these devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS767D3xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range. The TPS767D3xx specifications reflect actual performance under load condition.

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767D3xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767D3xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA . If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μs .

minimum load requirements

The TPS767D3xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network as is shown in Figure 27 to close the loop. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential. In fixed output options this pin is a no connect.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS767D3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767D3xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.



TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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external capacitor requirements (continued)

When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

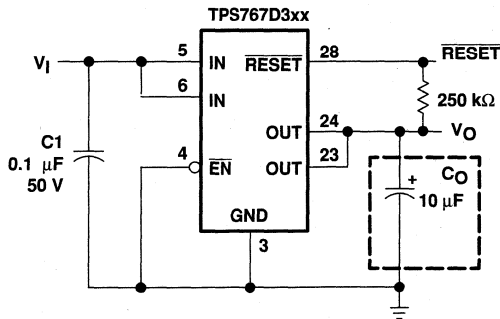


Figure 26. Typical Application Circuit (Fixed Versions) for Single Channel

programming the TPS767D301 adjustable LDO regulator

The output voltage of the TPS767D301 adjustable regulator is programmed using an external resistor divider as shown in Figure 27. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

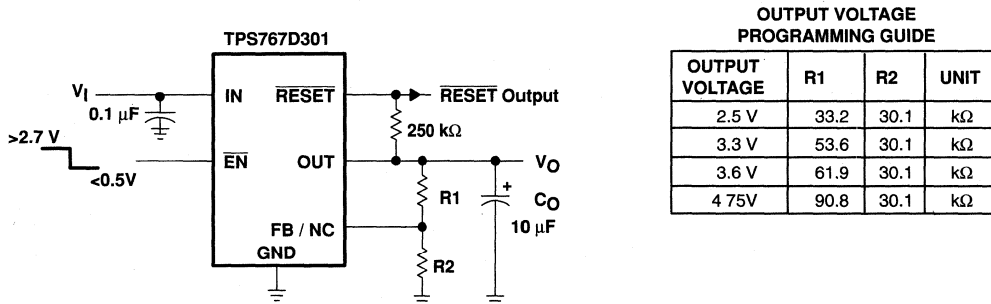


Figure 27. TPS767D301 Adjustable LDO Regulator Programming

TPS767D301, TPS767D318, TPS767D325 DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

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Reset indicator

The TPS767D3xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to 95% (typical) of its regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator.

regulator protection

The TPS767D3xx PMOS-pass transistor has a built-in back-gate diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767D3xx also features internal current limiting and thermal protection. During normal operation, the TPS767D3xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(\max)} = \frac{T_{J\max} - T_A}{R_{\theta JA}}$$

Where

$T_{J\max}$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 27.9°C/W for the 28-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

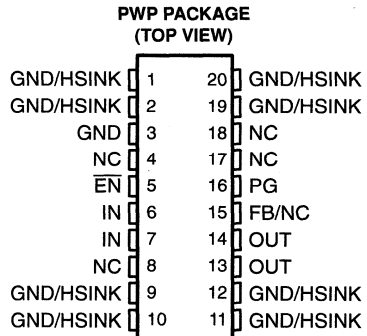
TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS

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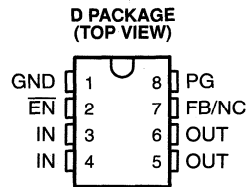
- 1 A Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions
- Dropout Voltage Down to 230 mV at 1 A (TPS76850)
- Ultra Low 85 μ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open Drain Power Good (See TPS767xx for Power-On Reset With 200-ms Delay Option)
- 8-Pin SOIC and 20-Pin TSSOP (PWP) Package
- Thermal Shutdown Protection

description

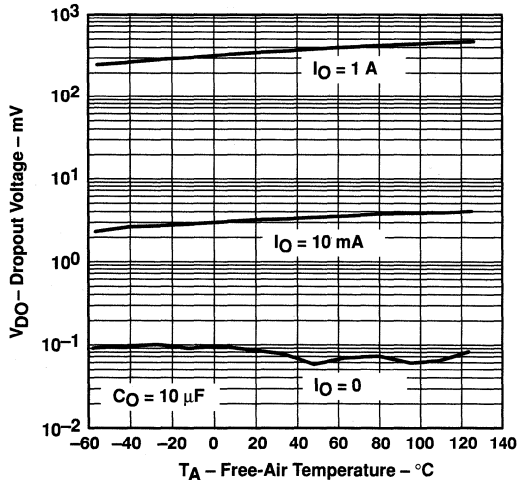
This device is designed to have a fast transient response and be stable with 10- μ F low ESR capacitors. This combination provides high performance at a reasonable cost.



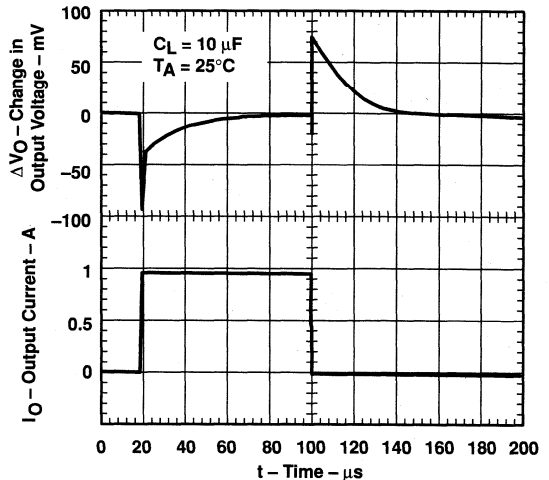
NC – No internal connection



**TPS76833
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



LOAD TRANSIENT RESPONSE



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A at $T_J = 25^\circ\text{C}$.

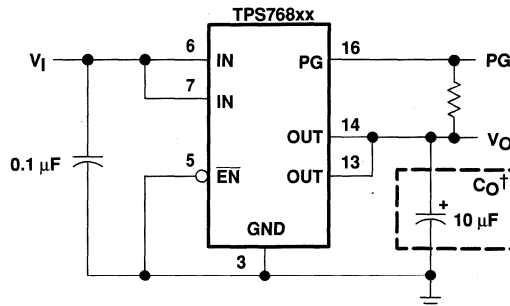
Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS768xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS768xx family is available in 8 pin SOIC and 20 pin PWP packages.

AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES	
	TYP	TSSOP (PWP)	SOIC (D)
-40°C to 125°C	5.0	TPS76850Q	TPS76850Q
	3.3	TPS76833Q	TPS76833Q
	3.0	TPS76830Q	TPS76830Q
	2.8	TPS76828Q	TPS76828Q
	2.7	TPS76827Q	TPS76827Q
	2.5	TPS76825Q	TPS76825Q
	1.8	TPS76818Q	TPS76818Q
	1.5	TPS76815Q	TPS76815Q
	Adjustable 1.2 V to 5.5 V	TPS76801Q	TPS76801Q

The TPS76801 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76801QDR).



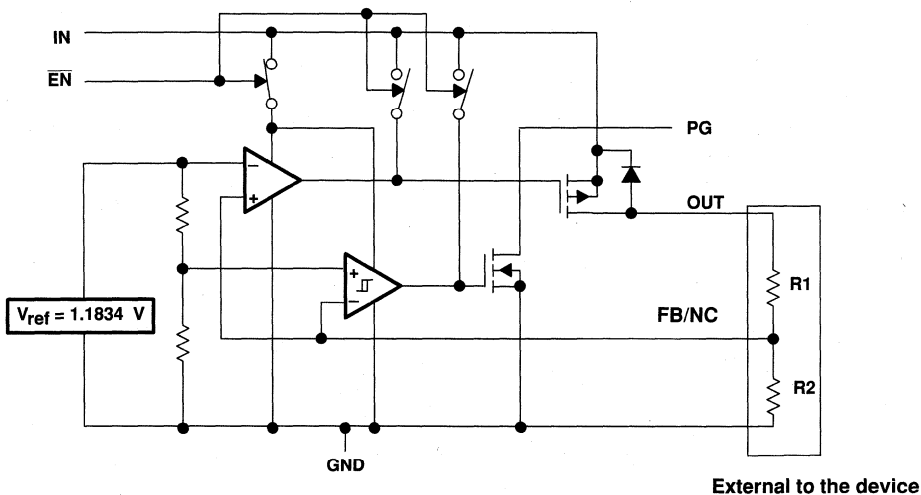
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

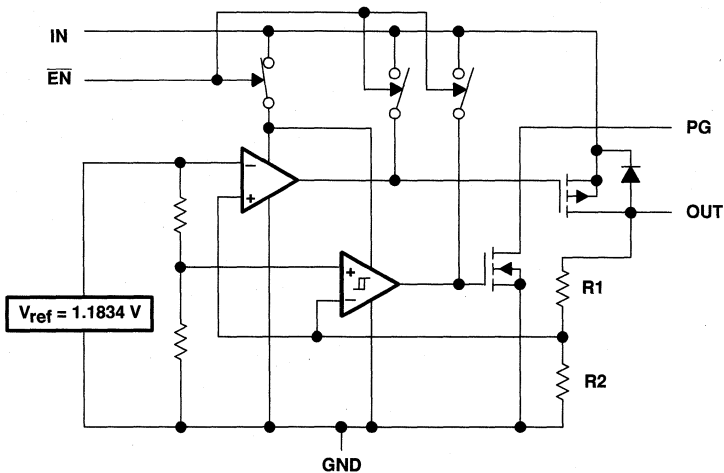


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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



**TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
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Terminal Functions – SOIC Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	1		Regulator ground
\overline{EN}	2	I	Enable input
IN	3	I	Input voltage
IN	4	I	Input voltage
OUT	5	O	Regulated output voltage
OUT	6	O	Regulated output voltage
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
PG	8	O	PG output

Terminal Functions – PWP Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND/HSINK	1		Ground/heatsink
GND/HSINK	2		Ground/heatsink
GND	3		LDO ground
NC	4		No connect
\overline{EN}	5	I	Enable input
IN	6	I	Input
IN	7	I	Input
NC	8		No connect
GND/HSINK	9		Ground/heatsink
GND/HSINK	10		Ground/heatsink
GND/HSINK	11		Ground/heatsink
GND/HSINK	12		Ground/heatsink
OUT	13	O	Regulated output voltage
OUT	14	O	Regulated output voltage
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
PG	16	O	PG output
NC	17		No connect
NC	18		No connect
GND/HSINK	19		Ground/heatsink
GND/HSINK	20		Ground/heatsink



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	-0.3 V to 13.5 V
Voltage range at EN	-0.3 V to $V_I + 0.3$ V
Maximum PG voltage	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See dissipation rating tables
Output voltage, V_O (OUT, FB)	7 V
Operating virtual junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568.18 mW	5.6818 mW/°C	312.5 mW	227.27 mW
	250	904.15 mW	9.0415 mW/°C	497.28 mW	361.66 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

|| This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I ☆	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	1.0	A
Operating virtual junction temperature, T_J (Note 1)	-40	125	°C

☆ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



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**electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_O(\text{typ}) + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 10\text{ }\mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 1 A load) (see Note 2)	TPS76801	$5.5\text{ V} \geq V_O \geq 1.2\text{ V}$, $T_J = 25^\circ\text{C}$	V_O			V
		$5.5\text{ V} \geq V_O \geq 1.2\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	$0.98V_O$		$1.02V_O$	
	TPS76815	$T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_{IN} < 10\text{ V}$		1.5		
	TPS76818	$T_J = -40^\circ\text{C}$ to 125°C , $2.7\text{ V} < V_{IN} < 10\text{ V}$	1.470		1.530	
		$T_J = 25^\circ\text{C}$, $2.8\text{ V} < V_{IN} < 10\text{ V}$		1.8		
	TPS76825	$T_J = -40^\circ\text{C}$ to 125°C , $2.8\text{ V} < V_{IN} < 10\text{ V}$	1.764		1.836	
		$T_J = 25^\circ\text{C}$, $3.5\text{ V} < V_{IN} < 10\text{ V}$		2.5		
	TPS76827	$T_J = -40^\circ\text{C}$ to 125°C , $3.5\text{ V} < V_{IN} < 10\text{ V}$	2.450		2.550	
		$T_J = 25^\circ\text{C}$, $3.7\text{ V} < V_{IN} < 10\text{ V}$		2.7		
	TPS76828	$T_J = -40^\circ\text{C}$ to 125°C , $3.7\text{ V} < V_{IN} < 10\text{ V}$	2.646		2.754	
		$T_J = 25^\circ\text{C}$, $3.8\text{ V} < V_{IN} < 10\text{ V}$		2.8		
	TPS76830	$T_J = -40^\circ\text{C}$ to 125°C , $3.8\text{ V} < V_{IN} < 10\text{ V}$	2.744		2.856	
		$T_J = 25^\circ\text{C}$, $4.0\text{ V} < V_{IN} < 10\text{ V}$		3.0		
	TPS76833	$T_J = -40^\circ\text{C}$ to 125°C , $4.0\text{ V} < V_{IN} < 10\text{ V}$	2.940		3.060	
$T_J = 25^\circ\text{C}$, $4.3\text{ V} < V_{IN} < 10\text{ V}$			3.3			
TPS76850	$T_J = -40^\circ\text{C}$ to 125°C , $4.3\text{ V} < V_{IN} < 10\text{ V}$	3.234		3.366		
	$T_J = 25^\circ\text{C}$, $6.0\text{ V} < V_{IN} < 10\text{ V}$		5.0			
Quiescent current (GND current) $\overline{\text{EN}} = 0\text{ V}$, (see Note 2)	$10\text{ }\mu\text{A} < I_O < 1\text{ A}$, $T_J = 25^\circ\text{C}$		85		μA	
	$I_O = 1\text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C			125		
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)	$V_O + 1\text{ V} < V_i \leq 10\text{ V}$, $T_J = 25^\circ\text{C}$		0.01		%/V	
Load regulation			3		mV	
Output noise voltage	BW = 300 Hz to 50 kHz, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$		190		μVrms	
Output current Limit	$V_O = 0\text{ V}$		1.7	2	A	
Thermal shutdown junction temperature			150		$^\circ\text{C}$	
Standby current	$\overline{\text{EN}} = V_i$, $T_J = 25^\circ\text{C}$, $2.7\text{ V} < V_i < 10\text{ V}$		1		μA	
	$\overline{\text{EN}} = V_i$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7\text{ V} < V_i < 10\text{ V}$			10	μA	
FB input current	TPS76801 $\text{FB} = 1.5\text{ V}$		2		nA	
High level enable input voltage			1.7		V	
Low level enable input voltage				0.9	V	
Power supply ripple rejection (see Note 2)	$f = 1\text{ KHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$		60		dB	
PG	Minimum input voltage for valid PG	$I_O(\text{PG}) = 300\text{ }\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_i = 2.7\text{ V}$, $I_O(\text{PG}) = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{PG}) = 5\text{ V}$			1	μA
Input current (EN)	$\overline{\text{EN}} = 0\text{ V}$		-1	0	1	μA
	$\overline{\text{EN}} = V_i$		-1		1	

NOTE: 2. Minimum IN operating voltage is 2.7 V or $V_O(\text{typ}) + 1\text{ V}$, whichever is greater. Maximum IN voltage 10 V.



**TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
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electrical characteristics over recommended operating free-air temperature range, $V_i = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\text{EN} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage (See Note 4)	TPS76828	$I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$			500		mV
		$I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C				825	
	TPS76830	$I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$			450		
		$I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C				675	
	TPS76833	$I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$			350		
		$I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C				575	
	TPS76850	$I_O = 1 \text{ A}$, $T_J = 25^\circ\text{C}$			230		
		$I_O = 1 \text{ A}$, $T_J = -40^\circ\text{C}$ to 125°C				380	

NOTES: 3. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imax}} = 10 \text{ V}$, $V_{\text{imin}} = 2.7 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imax}} = 10 \text{ V}$, $V_{\text{imin}} = V_O + 1 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

4. IN voltage equals $V_O(\text{Typ}) - 100 \text{ mV}$; TPS76801 output voltage set to 3.3 V nominal with external resistor divider. TPS76815, TPS76818, TPS76825, and TPS76827 dropout voltage limited by input voltage range limitations (i.e., TPS76830 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8, 9
	Power supply ripple rejection	vs Frequency	10
	Output noise	vs Frequency	11
Z_o	Output impedance	vs Frequency	12
V_{DO}	Dropout voltage	vs Free-air temperature	13
	Line transient response		14, 16
	Load transient response		15, 17
	Output voltage	vs Time	18
	Dropout voltage	vs Input voltage	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24

TYPICAL CHARACTERISTICS

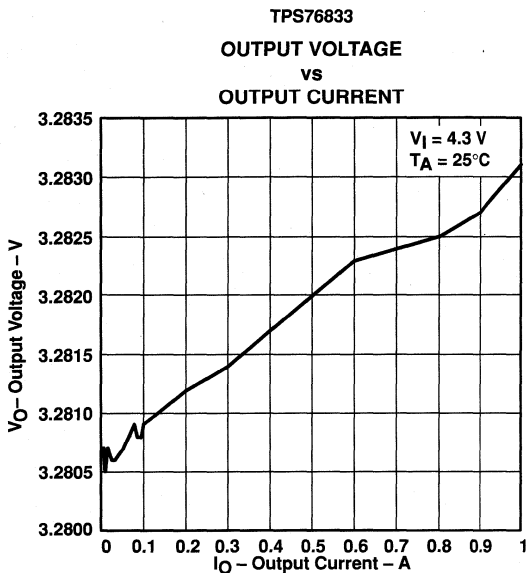


Figure 2

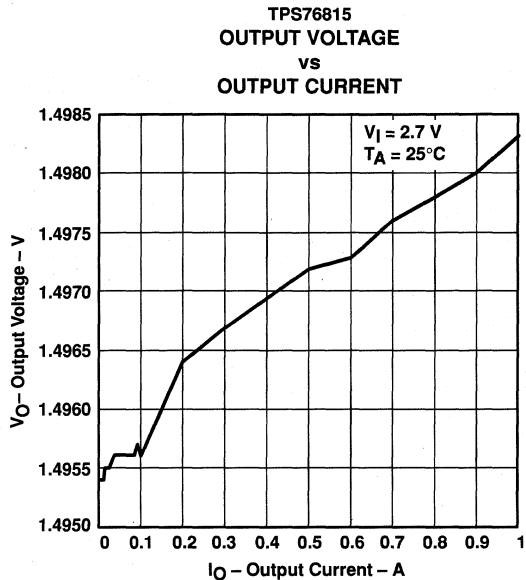


Figure 3

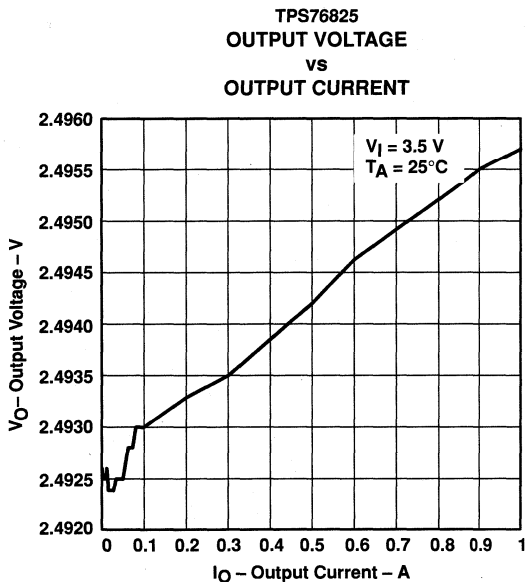


Figure 4

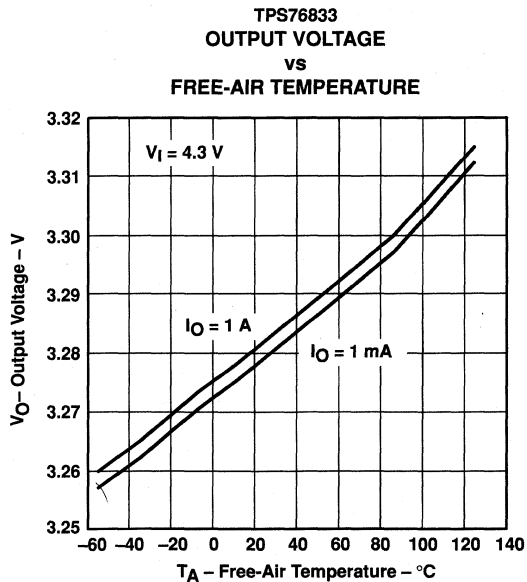


Figure 5

**TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
 TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
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TYPICAL CHARACTERISTICS

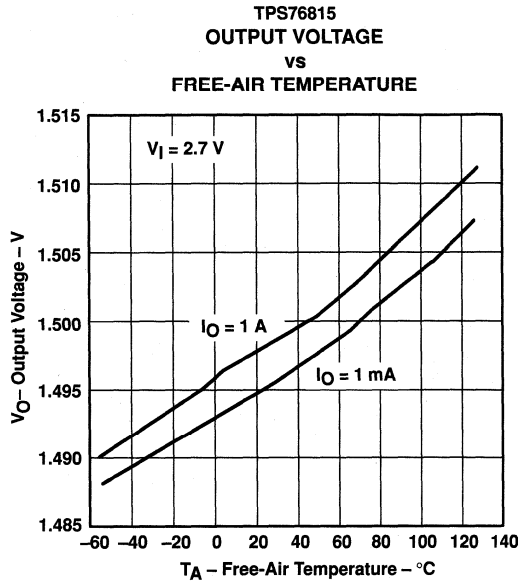


Figure 6

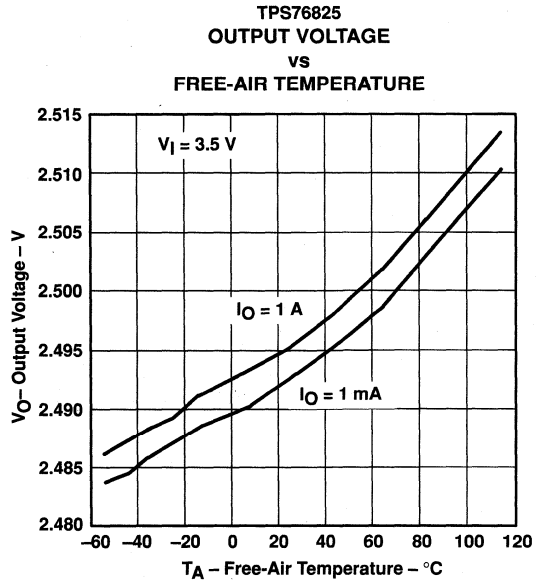


Figure 7

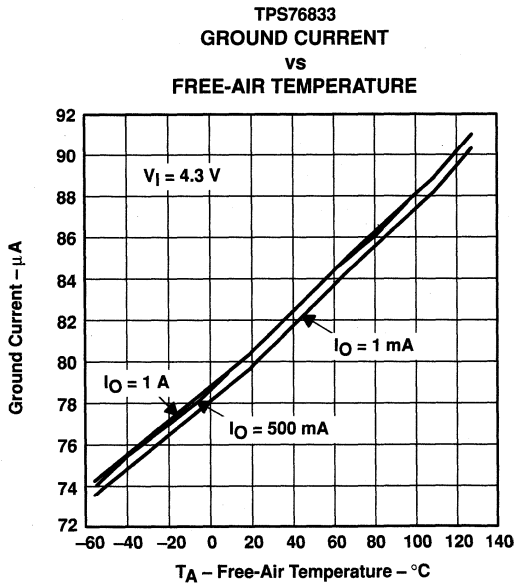


Figure 8

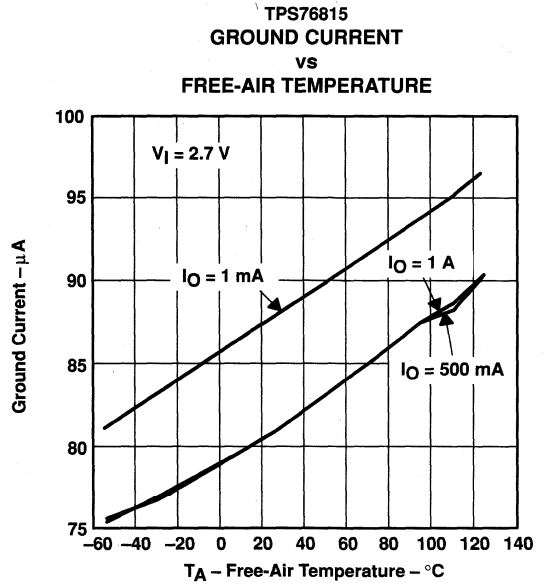


Figure 9

TYPICAL CHARACTERISTICS

TPS76833
POWER SUPPLY RIPPLE REJECTION
 vs
FREQUENCY

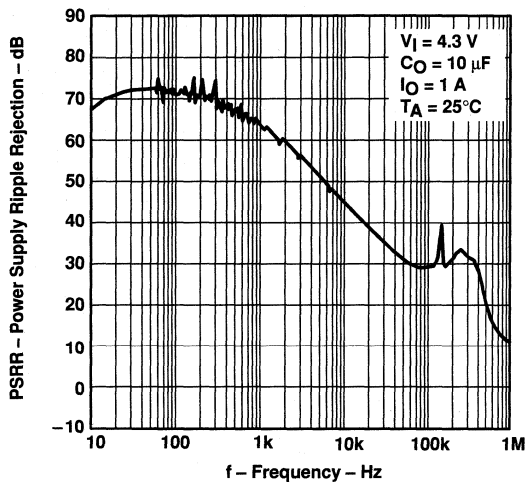


Figure 10

TPS76833
OUTPUT SPECTRAL NOISE DENSITY
 vs
FREQUENCY

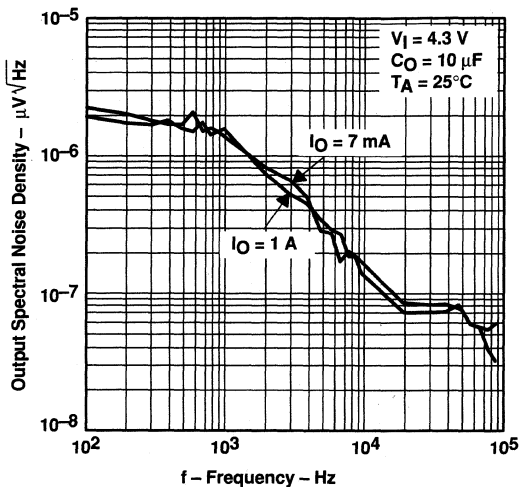


Figure 11

TPS76833
OUTPUT IMPEDANCE
 vs
FREQUENCY

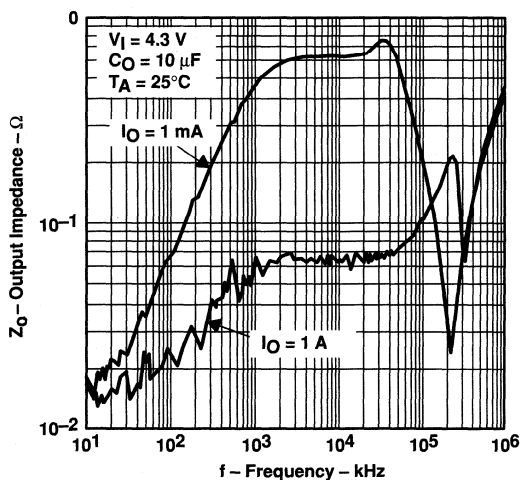


Figure 12

TPS76833
DROPOUT VOLTAGE
 vs
FREE-AIR TEMPERATURE

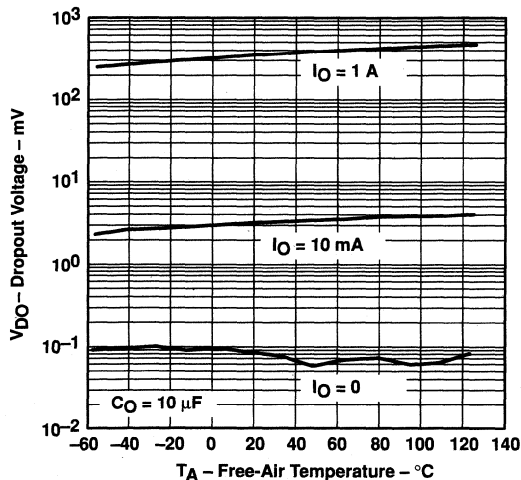


Figure 13

**TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
 TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
 FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**
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TYPICAL CHARACTERISTICS

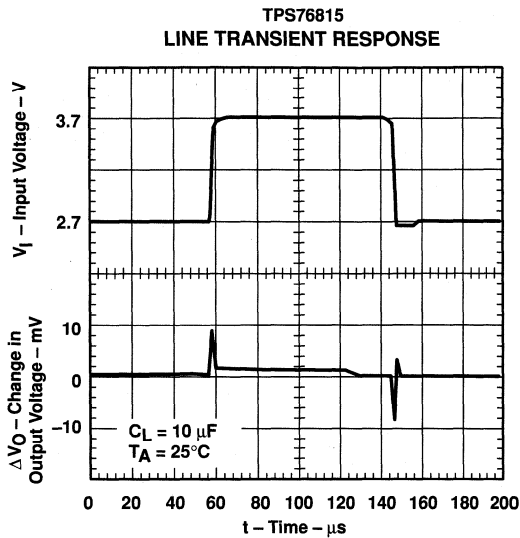


Figure 14

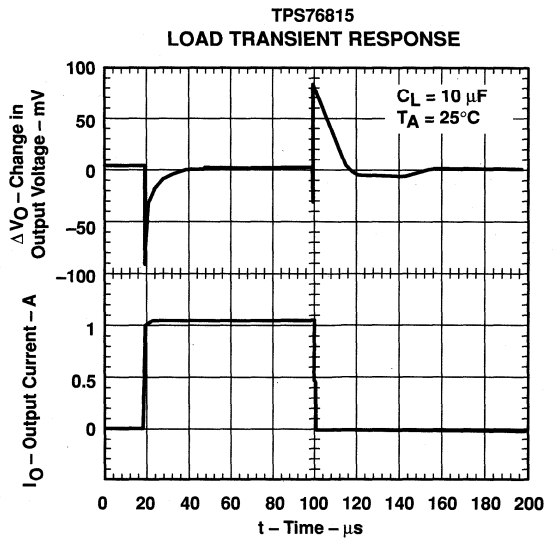


Figure 15

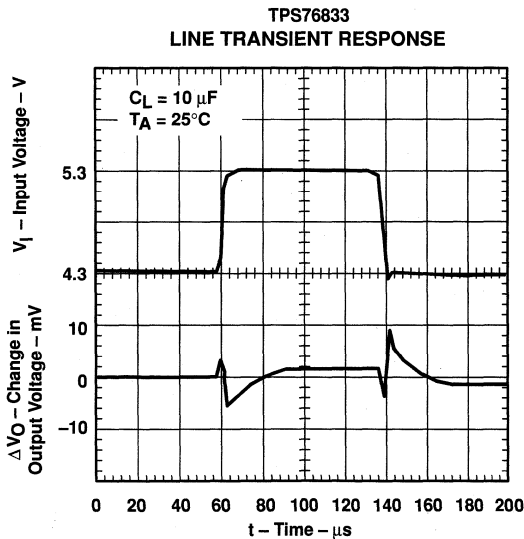


Figure 16

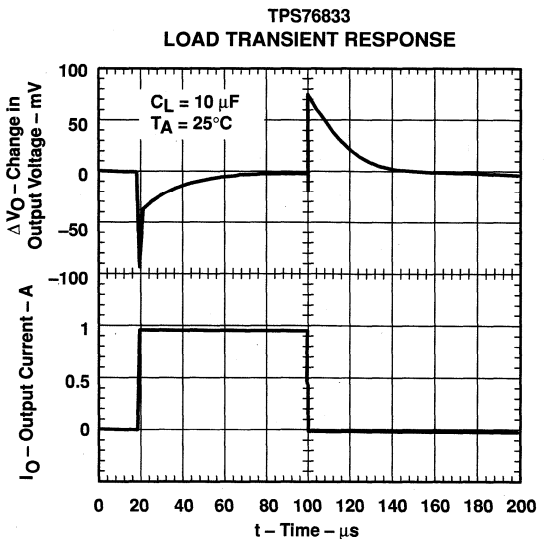


Figure 17

TYPICAL CHARACTERISTICS

TPS76833
**OUTPUT VOLTAGE
 vs
 TIME (AT STARTUP)**

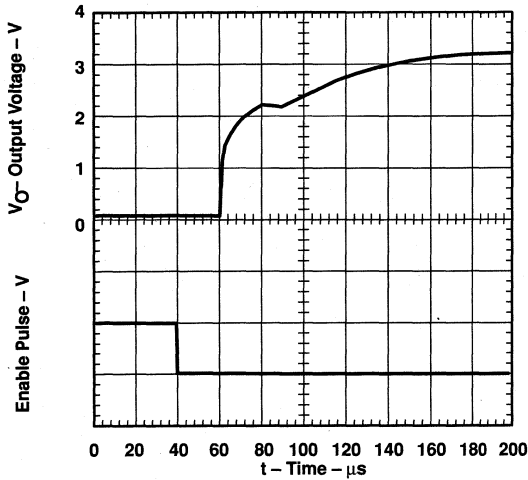


Figure 18

TPS76801
**DROPOUT VOLTAGE
 vs
 INPUT VOLTAGE**

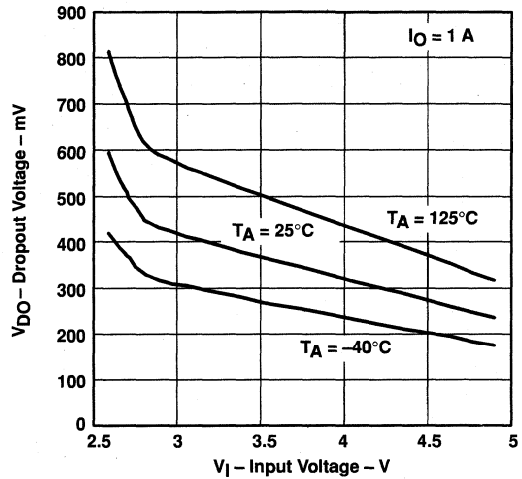


Figure 19

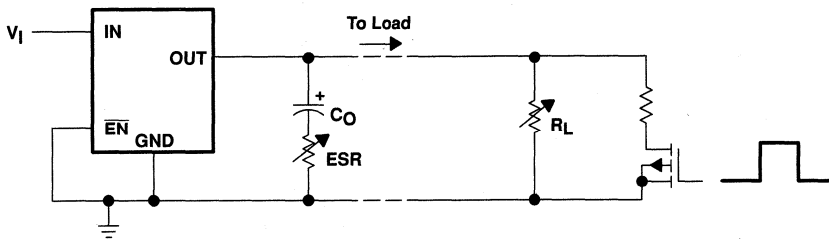


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
 TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
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TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

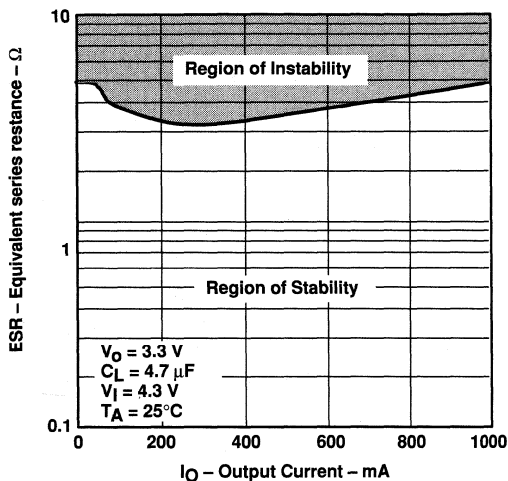


Figure 21

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

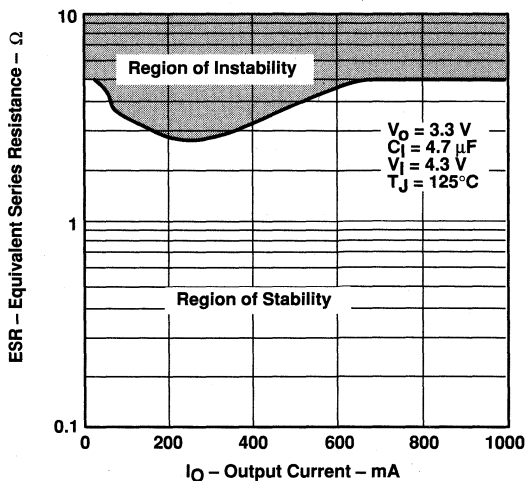


Figure 22

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

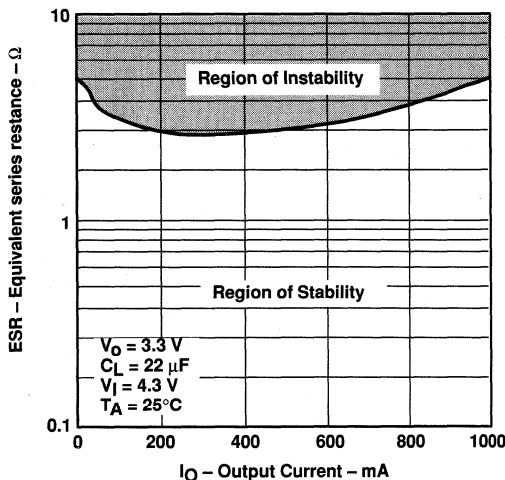


Figure 23

TYPICAL REGION OF STABILITY
 EQUIVALENT SERIES RESISTANCE†
 vs
 OUTPUT CURRENT

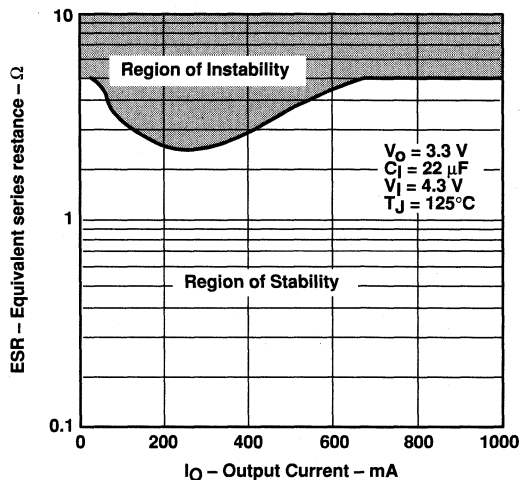


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS76815Q, TPS76818Q, TPS76825Q, TPS76827Q
TPS76828Q, TPS76830Q, TPS76833Q, TPS76850Q, TPS76801Q
FAST-TRANSIENT-RESPONSE 1-A LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

The TPS768xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and offers an adjustable device, the TPS76801 (adjustable from 1.2 V to 5.5 V).

device operation

The TPS768xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS768xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS768xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS768xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μ A. If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μ s.

minimum load requirements

The TPS768xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS768xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS768xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μ F and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μ F or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 μ F surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

APPLICATION INFORMATION

external capacitor requirements (continued)

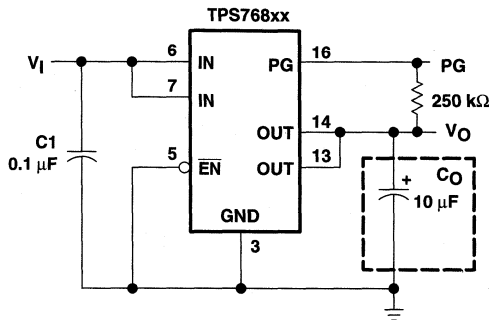


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS76801 adjustable LDO regulator

The output voltage of the TPS76801 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

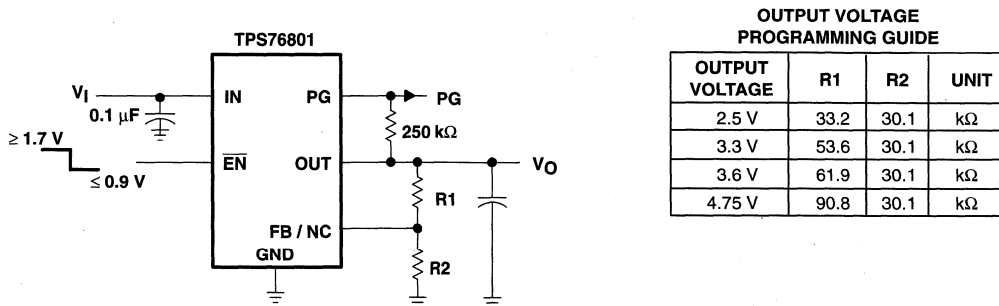
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



**OUTPUT VOLTAGE
PROGRAMMING GUIDE**

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ
4.75 V	90.8	30.1	kΩ

Figure 26. TPS76801 Adjustable LDO Regulator Programming

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power-good indicator

The TPS768xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS768xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS768xx also features internal current limiting and thermal protection. During normal operation, the TPS768xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

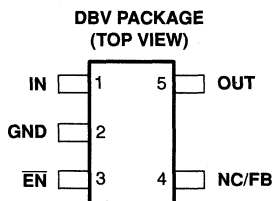
$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

**TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
TPS76927, TPS76928, TPS76930, TPS76933, TPS76950**
ULTRA LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS

SLVS203C – JUNE 1999 – REVISED SEPTEMBER 1999

- 100-mA Low-Dropout Regulator
- Available in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V Fixed-Output and Adjustable Versions
- Only 17 μA Quiescent Current at 100 mA
- 1 μA Quiescent Current in Standby Mode
- Dropout Voltage Typically 71 mV @ 100mA
- Over Current Limitation
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



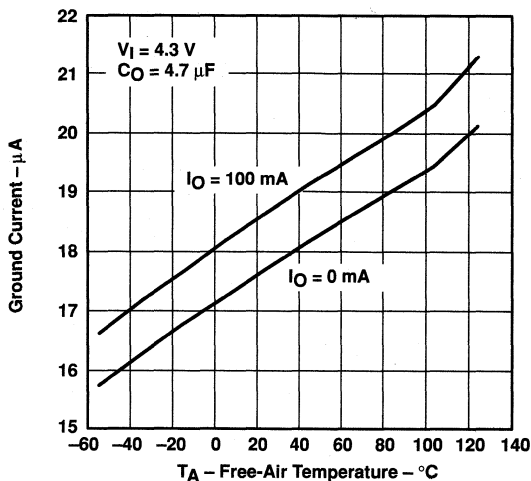
description

The TPS769xx family of low-dropout (LDO) voltage regulators offers the benefits of low dropout voltage, ultra low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and ultra low quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS769xx series devices are ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 71 mV at 100 mA of load current (TPS76950), and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultra low (28 μA maximum) and is stable over the entire range of output load current (0 mA to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultra low-dropout voltage feature and ultra low-power operation result in a significant increase in system battery operating life.

The TPS769xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at $T_J = 25^{\circ}\text{C}$. The TPS769xx is offered in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.2 V to 5.5 V).

**TPS76933
GROUND CURRENT
vs
FREE-AIR TEMPERATURE**



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
TPS76927, TPS76928, TPS76930, TPS76933, TPS76950
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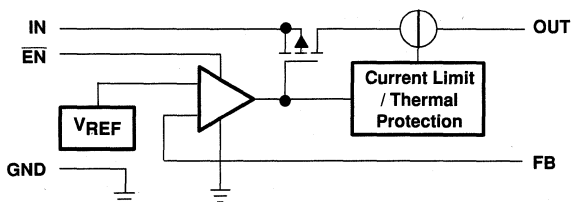
AVAILABLE OPTIONS

T _J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	Variable 1.2V to 5.5V	SOT-23 (DBV)	TPS76901DBVT†	TPS76901DBVR‡	PCFI
	1.2 V		TPS76912DBVT†	TPS76912DBVR‡	PCGI
	1.5 V		TPS76915DBVT†	TPS76915DBVR‡	PCHI
	1.8 V		TPS76918DBVT†	TPS76918DBVR‡	PCII
	2.5 V		TPS76925DBVT†	TPS76925DBVR‡	PCJI
	2.7 V		TPS76927DBVT†	TPS76927DBVR‡	PCKI
	2.8 V		TPS76928DBVT†	TPS76928DBVR‡	PCLI
	3.0 V		TPS76930DBVT†	TPS76930DBVR‡	PCMI
	3.3 V		TPS76933DBVT†	TPS76933DBVR‡	PCNI
	5.0 V		TPS76950DBVT†	TPS76950DBVR‡	PCOI

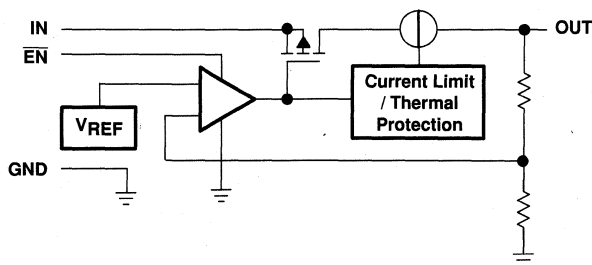
† The DBVT indicates tape and reel of 250 parts.
 ‡ The DBVR indicates tape and reel of 3000 parts.

functional block diagram

TPS76901



TPS76912/15/18/25/27/28/30/33/50



**TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
TPS76927, TPS76928, TPS76930, TPS76933, TPS76950**
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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	2		Ground
EN	3	I	Enable input
FB	4	I	Feedback voltage (TPS76901 only)
IN	1	I	Input supply voltage
NC	4		No connection (Fixed options only)
OUT	5	O	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1)	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Absolute Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 2)	2.7		10	V
Output voltage range, V_O	1.2		5.5	V
Continuous output current, I_O (see Note 3)	0		100	mA
Operating junction temperature, T_J	–40		125	°C

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_I(\text{min}) = V_O(\text{max}) + V_{DO}(\text{max load})$$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

**TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
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electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(\text{typ})} + 1$ V, $I_O = 100$ mA, $\overline{\text{EN}} = 0$ V, $C_O = 4.7$ μ F (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μ A to 100 mA Load) (See Note 4)	TPS76901	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$	V_O		V
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$	0.97 V_O	1.03 V_O	
	TPS76912	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.224		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.187	1.261	
	TPS76915	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.5		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $2.7 \text{ V} < V_{IN} < 10 \text{ V}$	1.455	1.545	
	TPS76918	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.8		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $2.8 \text{ V} < V_{IN} < 10 \text{ V}$	1.746	1.854	
	TPS76925	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.5		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $3.5 \text{ V} < V_{IN} < 10 \text{ V}$	2.425	2.575	
	TPS76927	$T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.7		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $3.7 \text{ V} < V_{IN} < 10 \text{ V}$	2.619	2.781	
	TPS76928	$T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.8		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $3.8 \text{ V} < V_{IN} < 10 \text{ V}$	2.716	2.884	
	TPS76930	$T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{IN} < 10 \text{ V}$	3.0		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $4.0 \text{ V} < V_{IN} < 10 \text{ V}$	2.910	3.090	
	TPS76933	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.3		
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $4.3 \text{ V} < V_{IN} < 10 \text{ V}$	3.201	3.399	
TPS76950	$T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{IN} < 10 \text{ V}$	5.0			
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $6.0 \text{ V} < V_{IN} < 10 \text{ V}$	4.850	5.150		
Quiescent current (GND current) (See Note 4 and Note 5)	$\overline{\text{EN}} = 0$ V, $T_J = 25^\circ\text{C}$, $0 \text{ mA} < I_O < 100 \text{ mA}$	17		μ A	
	$\overline{\text{EN}} = 0$ V, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $I_O = 100 \text{ mA}$	28			
Load regulation	$\overline{\text{EN}} = 0$ V, $T_J = 25^\circ\text{C}$, $I_O = 0$ to 100 mA	12		mV	
Output voltage line regulation ($\Delta V_O/V_O$) (See Note 5)	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$, See Note 4	0.04		%V	
	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = -40^\circ\text{C to } 125^\circ\text{C}$, See Note 4	0.1			
Output noise voltage	BW = 300 Hz to 50 kHz, $C_O = 10 \mu$ F, $T_J = 25^\circ\text{C}$	190		μ Vrms	
Output current limit	$V_O = 0$ V, See Note 4	350	750	mA	
Standby current	$\overline{\text{EN}} = V_I$, $2.7 < V_I < 10 \text{ V}$	1		μ A	
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	2		μ A	

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1$ V, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μ A, maximum output current 100 mA.

5. If $V_O \leq 1.8$ V then $V_{\text{imin}} = 2.7$ V, $V_{\text{imax}} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5$ V then $V_{\text{imin}} = V_O + 1$ V, $V_{\text{imax}} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



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electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1\text{ V}$, $I_O = 100\text{ mA}$, $EN = 0\text{V}$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
FB input current		FB = 1.224 V (TPS76901)	-1		1	μA	
High level enable input voltage		$2.7\text{ V} < V_I < 10\text{ V}$	1.7			V	
Low level enable input voltage		$2.7\text{ V} < V_I < 10\text{ V}$			0.9	V	
Power supply ripple rejection		f = 1 kHz, $T_J = 25^\circ\text{C}$, $C_O = 10\text{ }\mu\text{F}$, See Note 4		60		dB	
Input current (EN)		EN = 0 V	-1	0	1	μA	
		EN = V_I	-1		1	μA	
Dropout voltage (See Note 6)	TPS76928	$I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$		60		mV	
		$I_O = 50\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			125		
		$I_O = 100\text{ mA}$, $T_J = 25^\circ\text{C}$			122		
		$I_O = 100\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			245		
	TPS76930	$I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$			57		
		$I_O = 50\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					115
		$I_O = 100\text{ mA}$, $T_J = 25^\circ\text{C}$					115
		$I_O = 100\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					230
	TPS76933	$I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$			48		
		$I_O = 50\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					100
		$I_O = 100\text{ mA}$, $T_J = 25^\circ\text{C}$					98
		$I_O = 100\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					200
	TPS76950	$I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$			35		
		$I_O = 50\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					85
		$I_O = 100\text{ mA}$, $T_J = 25^\circ\text{C}$					71
		$I_O = 100\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C					170

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_{O(typ)} + 1\text{ V}$, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 100 mA.

6. IN voltage equals $V_{O(typ)} - 100\text{mV}$; TPS76901 output voltage set to 3.3V nominal with external resistor divider. TPS76912, TPS76915, TPS76918, TPS76925, and TPS76927 dropout voltage limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
V_O	Output voltage	vs Output current	1, 2, 3
		vs Free-air temperature	4, 5, 6
	Ground current	vs Free-air temperature	7
	Output spectral noise density	vs Frequency	8
Z_O	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Free-air temperature	10
		Ripple rejection	vs Frequency
	LDO startup time		12
	Line transient response		13, 15
	Load transient response		14, 16
	Equivalent series resistance (ESR)	vs Output current	17, 19
		vs Added ceramic capacitance	18, 20



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TYPICAL CHARACTERISTICS

**TPS76925
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

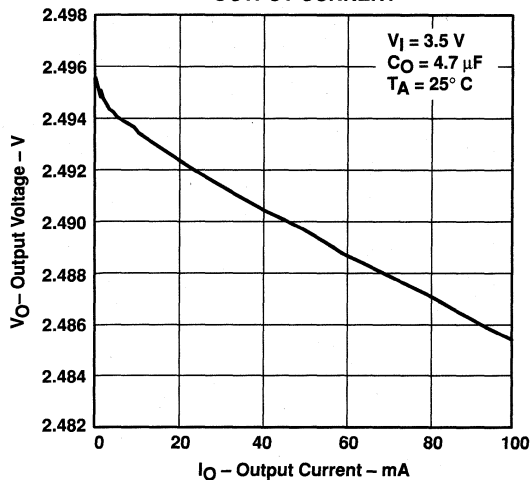


Figure 1

**TPS76915
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

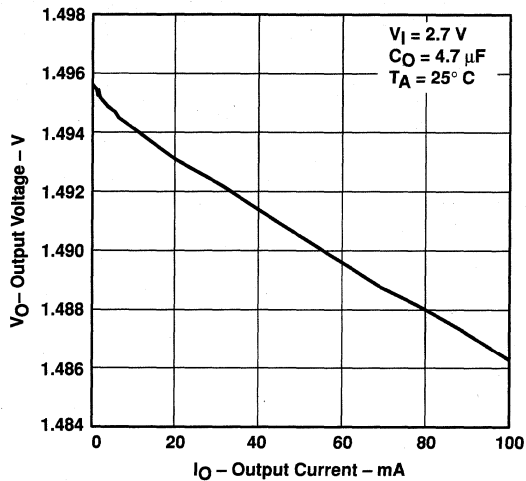


Figure 2

**TPS76933
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

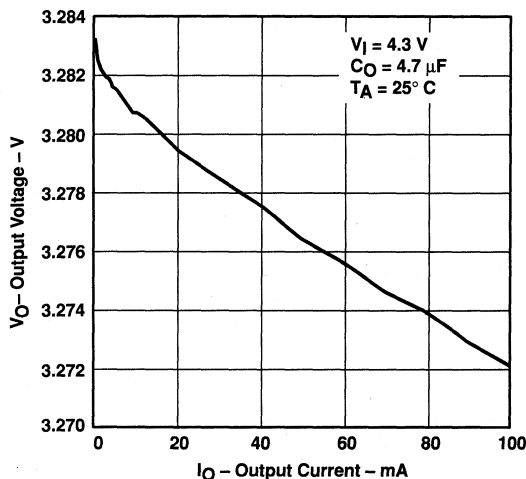


Figure 3

**TPS76915
 OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE**

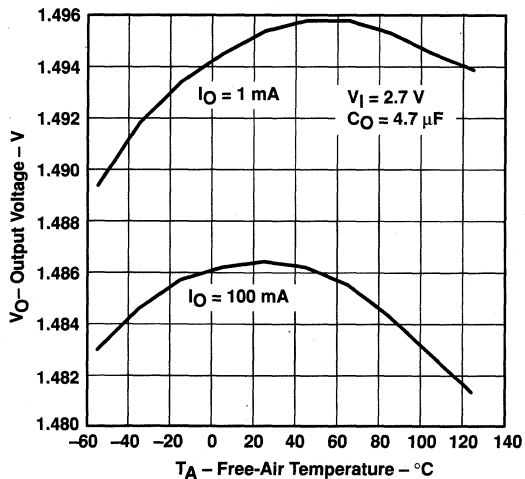


Figure 4



TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
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TYPICAL CHARACTERISTICS

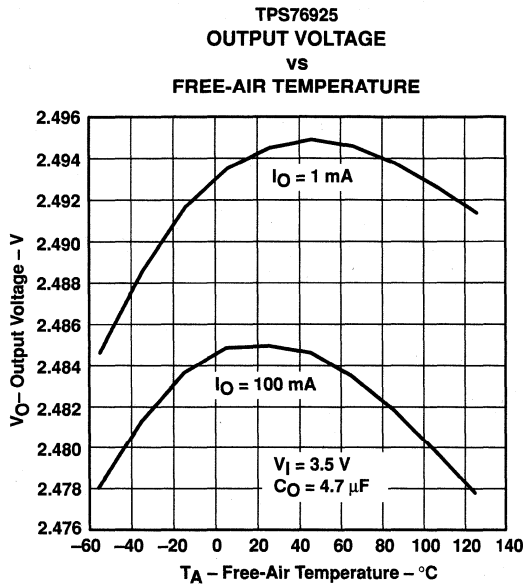


Figure 5

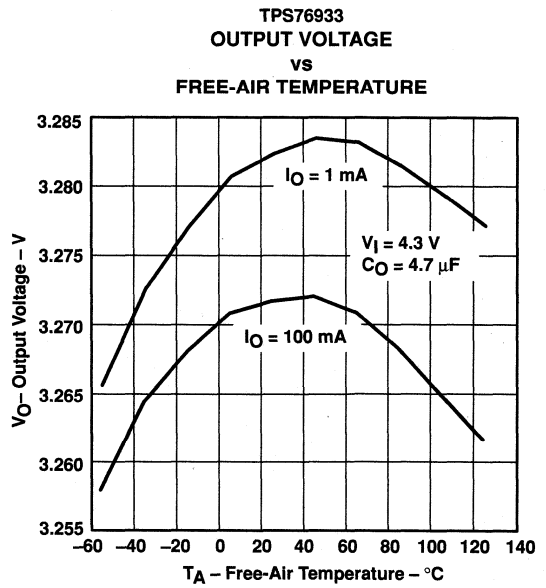


Figure 6

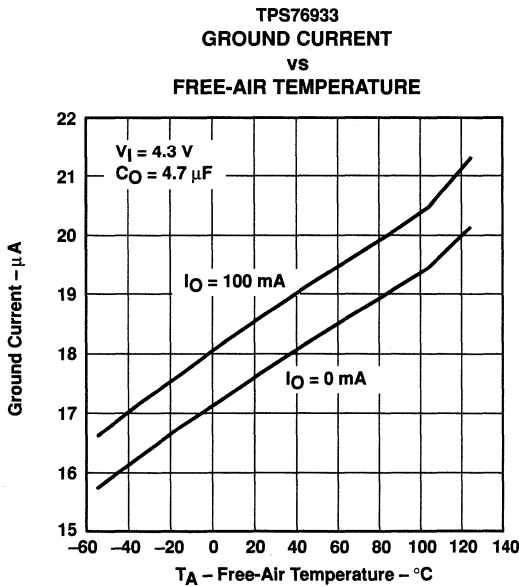


Figure 7

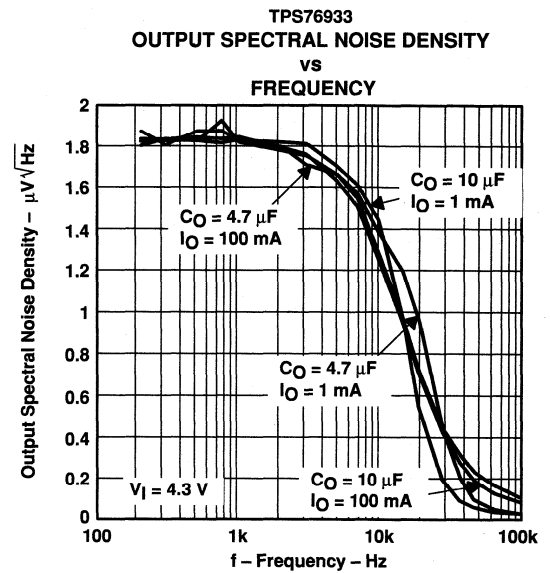


Figure 8

TYPICAL CHARACTERISTICS

**OUTPUT IMPEDANCE
vs
FREQUENCY**

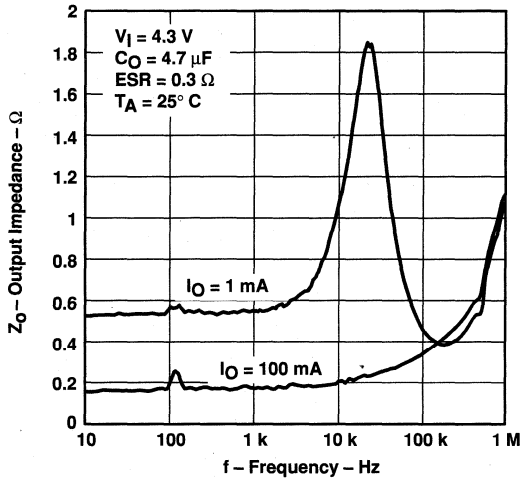


Figure 9

**TPS76933
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

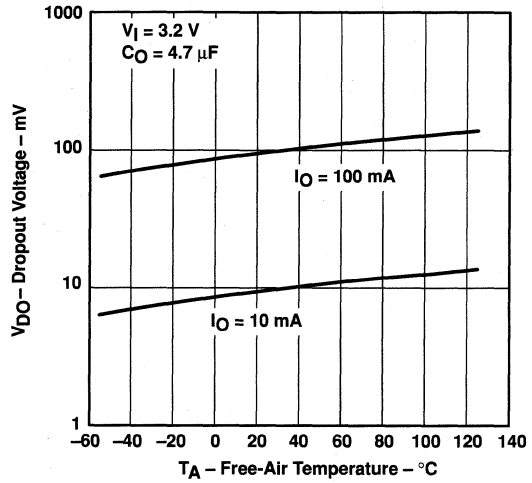


Figure 10

**TPS76933
RIPPLE REJECTION
vs
FREQUENCY**

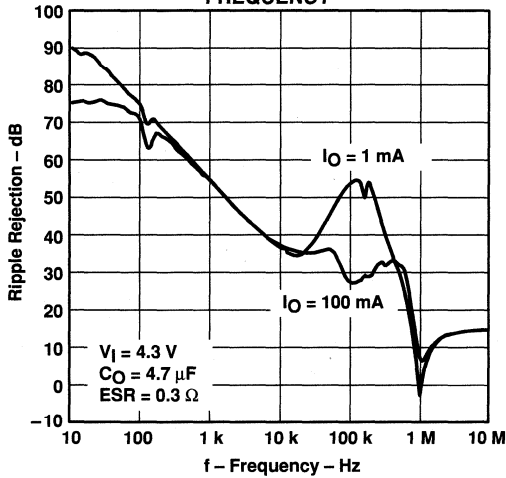


Figure 11

LDO STARTUP TIME

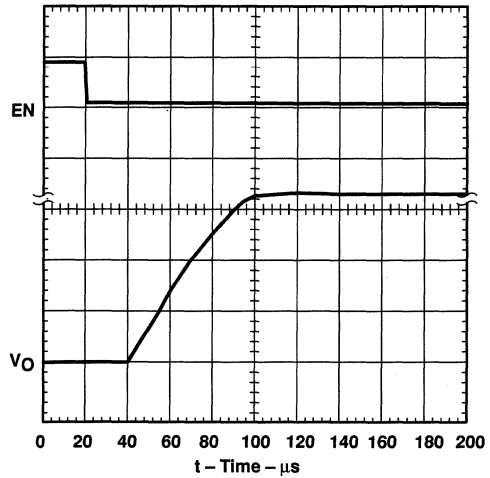


Figure 12

TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
 TPS76927, TPS76928, TPS76930, TPS76933, TPS76950
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TYPICAL CHARACTERISTICS

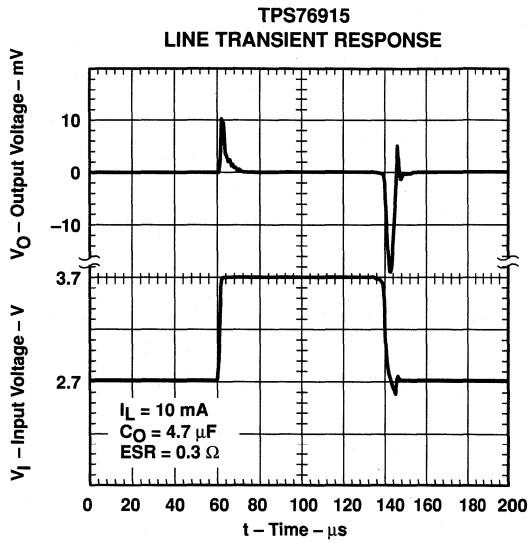


Figure 13

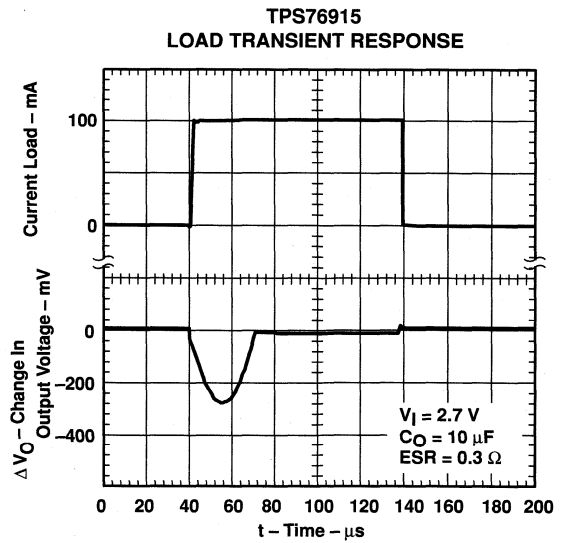


Figure 14

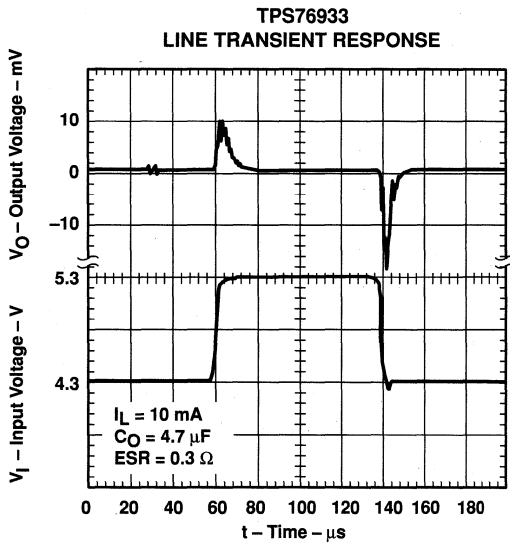


Figure 15

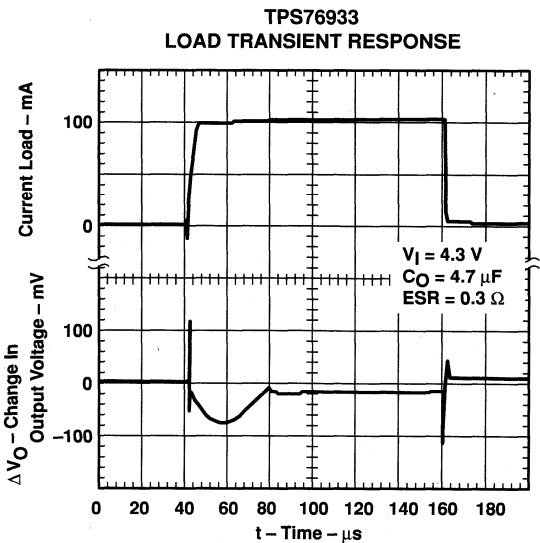


Figure 16

TYPICAL CHARACTERISTICS

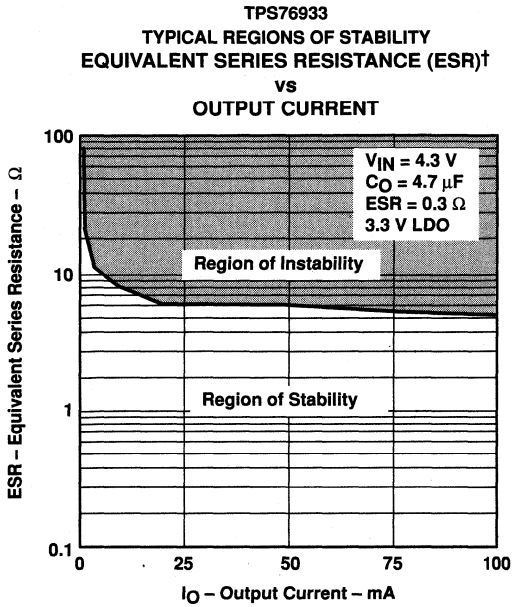


Figure 17

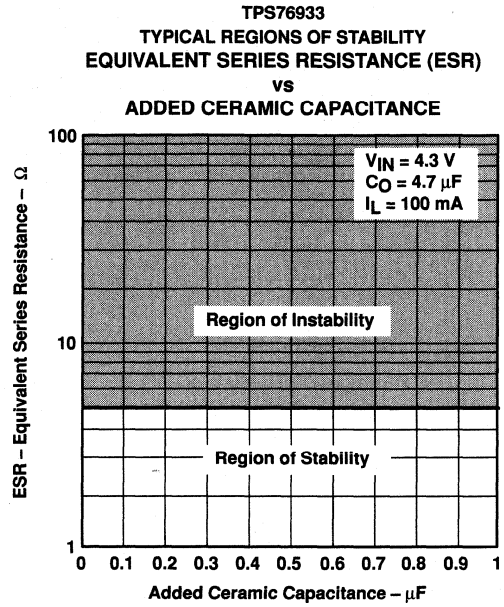


Figure 18

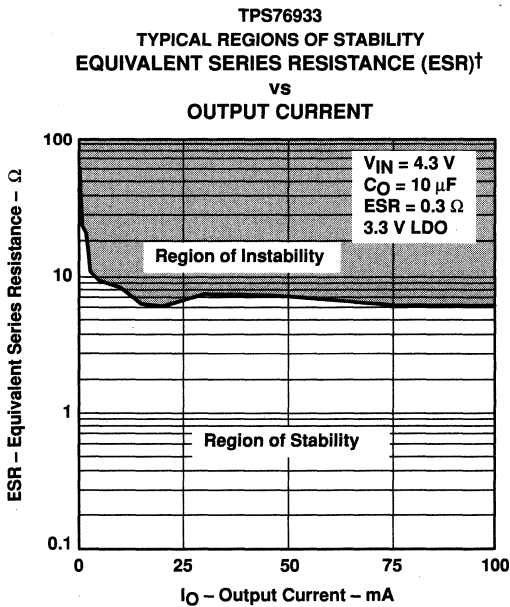


Figure 19

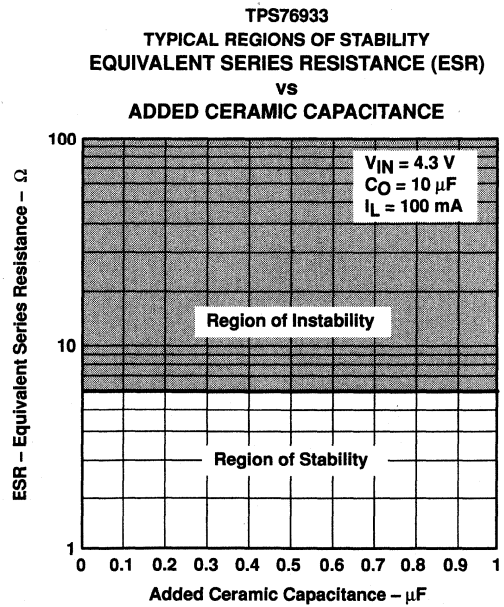


Figure 20

APPLICATION INFORMATION

The TPS769xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low quiescent current (17 μA nominally), and enable inputs to reduce supply currents to 1 μA when the regulators are turned off.

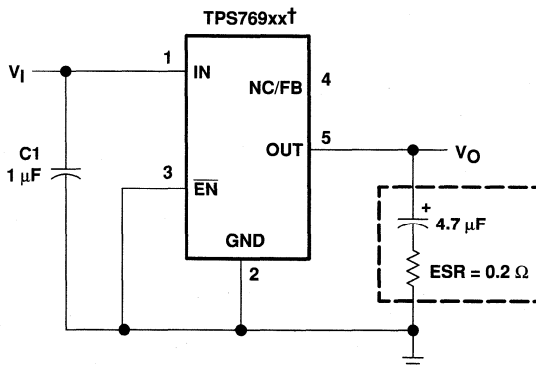
device operation

The TPS769xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS769xx is essentially constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the $\overline{\text{EN}}$ input will disable the TPS769xx internal circuitry, reducing the supply current to 1 μA . A voltage of less than 0.9 V on the $\overline{\text{EN}}$ input will enable the TPS769xx and will enable normal operation to resume. The $\overline{\text{EN}}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in Figure 21.



† TPS76912, TPS76915, TPS76918, TPS76925, TPS76927, TPS76928, TPS76930, TPS76933, TPS76950 (fixed-voltage options).

Figure 21. Typical Application Circuit

**TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
TPS76927, TPS76928, TPS76930, TPS76933, TPS76950
ULTRA LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047- μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS769xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS769xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μ F. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω to ensure stability. Capacitor values larger than 4.7 μ F are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μ F are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
T494B475K016AS	KEMET	4.7 μ F	1.5 Ω	1.9 \times 3.5 \times 2.8
195D106x0016x2T	SPRAGUE	10 μ F	1.5 Ω	1.3 \times 7.0 \times 2.7
695D106x003562T	SPRAGUE	10 μ F	1.3 Ω	2.5 \times 7.6 \times 2.5
TPSC475K035R0600	AVX	4.7 μ F	0.6 Ω	2.6 \times 6.0 \times 3.2

† Size is in mm. ESR is maximum resistance in Ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Contact manufacturer for minimum ESR values.

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS76901 adjustable regulator is programmed using an external resistor divider as shown in Figure 22. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

$$V_{ref} = 1.224 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 k Ω to set the divider current at 7 μ A and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

**OUTPUT VOLTAGE
PROGRAMMING GUIDE**

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (k Ω) [‡]	
	R1	R2
2.5	174	169
3.3	287	169
3.6	324	169
4.0	383	169
5.0	523	169

[‡] 1% values shown.

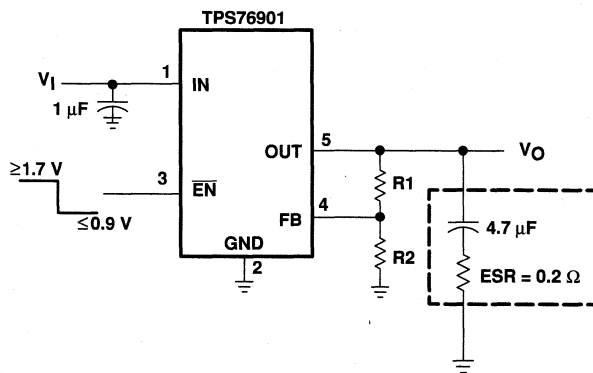


Figure 22. TPS76901 Adjustable LDO Regulator Programming

**TPS76901, TPS76912, TPS76915, TPS76918, TPS76925
TPS76927, TPS76928, TPS76930, TPS76933, TPS76950
ULTRA LOW-POWER 100-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

regulator protection

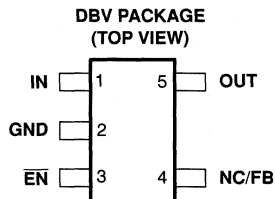
The TPS769xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS769xx features internal current limiting and thermal protection. During normal operation, the TPS769xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

TPS77001, TPS77012, TPS77015, TPS77018, TPS77025 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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- 50-mA Low-Dropout Regulator
- Available in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V Fixed-Output and Adjustable Versions
- Only 17 μA Quiescent Current at 50 mA
- 1 μA Quiescent Current in Standby Mode
- Dropout Voltage Typically 35 mV @ 50mA
- Over Current Limitation
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



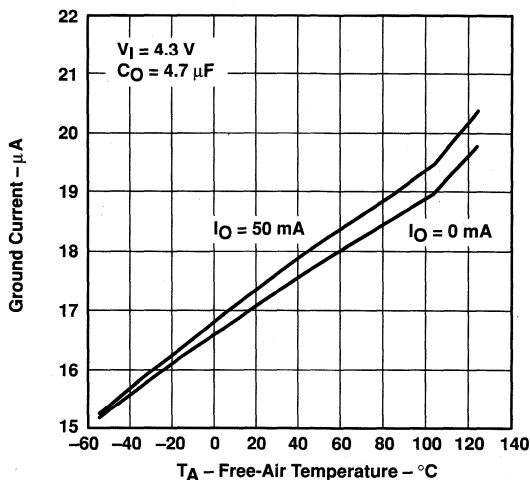
description

The TPS770xx family of low-dropout (LDO) voltage regulators offers the benefits of low dropout voltage, ultra low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and ultra low quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS770xx series devices are ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low — typically 35 mV at 50 mA of load current (TPS77050) — and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultra low (28 μA maximum) and is stable over the entire range of output load current (0 mA to 50 mA). Intended for use in portable systems such as laptops and cellular phones, the ultra low-dropout voltage feature and ultra low-power operation result in a significant increase in system battery operating life.

The TPS770xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at $T_J = 25^{\circ}\text{C}$. The TPS770xx is offered in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.2 V to 5.5 V).

TPS77033
GROUND CURRENT
vs
FREE-AIR TEMPERATURE



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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AVAILABLE OPTIONS

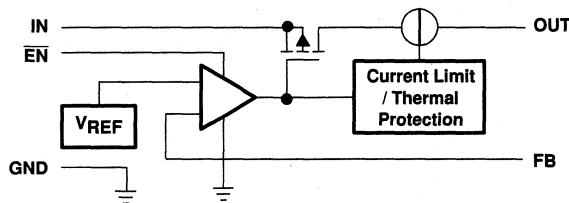
T _J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	Variable 1.2V to 5.5V	SOT-23 (DBV)	TPS77001DBVT†	TPS77001DBVR‡	PCPI
	1.2 V		TPS77012DBVT†	TPS77012DBVR‡	PCQI
	1.5 V		TPS77015DBVT†	TPS77015DBVR‡	PCRI
	1.8 V		TPS77018DBVT†	TPS77018DBVR‡	PCSI
	2.5 V		TPS77025DBVT†	TPS77025DBVR‡	PCTI
	2.7 V		TPS77027DBVT†	TPS77027DBVR‡	PCUI
	2.8 V		TPS77028DBVT†	TPS77028DBVR‡	PCVI
	3.0 V		TPS77030DBVT†	TPS77030DBVR‡	PCWI
	3.3 V		TPS77033DBVT†	TPS77033DBVR‡	PCXI
	5.0 V		TPS77050DBVT†	TPS77050DBVR‡	PCYI

† The DBVT indicates tape and reel of 250 parts.

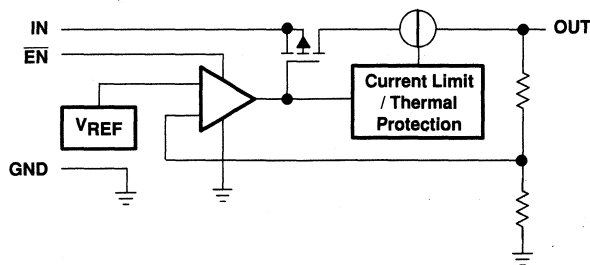
‡ The DBVR indicates tape and reel of 3000 parts.

functional block diagram

TPS77001



TPS77012/15/18/25/27/28/30/33/50



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	2		Ground
EN	3	I	Enable input
FB	4	I	Feedback voltage (TPS77001 only)
IN	1	I	Input supply voltage
NC	4		No connection (Fixed options only)
OUT	5	O	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1)	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

	PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Absolute Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 2)	2.7		10	V
Output voltage range, V_O	1.2		5.5	V
Continuous output current, I_O (see Note 3)	0		50	mA
Operating junction temperature, T_J	–40		125	°C

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_I(\text{min}) = V_O(\text{max}) + V_{DO}(\text{max load})$$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 50 \text{ mA}$, $\overline{\text{EN}} = 0\text{V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output voltage (10 μA to 50 mA Load) (See Note 4)	TPS77001 $1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$ $1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	V _O		0.97V _O	1.03V _O	
	TPS77012 $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.187	1.224	1.261		
	TPS77015 $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.455	1.545			
	TPS77018 $T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.746	1.854			
	TPS77025 $T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.425	2.575			
	TPS77027 $T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.619	2.781			
	TPS77028 $T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.716	2.884			
	TPS77030 $T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.910	3.090			
	TPS77033 $T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.201	3.399			
	TPS77050 $T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	4.850	5.150			
	Quiescent current (GND current) (See Note 4)	$\overline{\text{EN}} = 0\text{V}$, $T_J = 25^\circ\text{C}$, $0 \text{ mA} < I_O < 50\text{mA}$	17			μA
		$\overline{\text{EN}} = 0\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C , $I_O = 50\text{mA}$	28			
	Output voltage line regulation ($\Delta V_O/V_O$) (See Notes 4 and 5)	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$	0.04			%V
		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	0.1			
	Load regulation	$\overline{\text{EN}} = 0\text{V}$, $T_J = 25^\circ\text{C}$, $I_O = 0$ to 50 mA	8			mV
	Output noise voltage	BW = 300 Hz to 50 kHz, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	190			μVrms
	Output current limit	$V_O = 0\text{V}$, See Note 4	350 750			mA
	Standby current	$\overline{\text{EN}} = V_I$, $2.7 < V_I < 10 \text{ V}$	1			μA
$T_J = -40^\circ\text{C}$ to 125°C		2			μA	

NOTES: 4. Minimum IN operating voltage is 2.7 V or V_O (typ) + 1 V, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 50 mA.

5. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imin}} = 2.7 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imin}} = V_O + 1 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1\text{ V}$, $I_O = 50\text{ mA}$, $\text{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FB input current		FB = 1.224 V (TPS77001)		-1		1	μA
High level enable input voltage		2.7 V < V_I < 10 V		1.7			V
Low level enable input voltage		2.7 V < V_I < 10 V				0.9	V
Power supply ripple rejection		f = 1 kHz, $T_J = 25^\circ\text{C}$,	$C_O = 10\text{ }\mu\text{F}$, See Note 4		60		dB
Input current (EN)		$\text{EN} = 0\text{ V}$		-1	0	1	μA
		$\text{EN} = V_I$		-1		1	μA
Dropout voltage (See Note 6)	TPS77028	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		60		mV
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			125	
	TPS77030	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		57		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			115	
	TPS77033	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		48		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			100	
	TPS77050	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		35		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			85	

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_O(\text{typ}) + 1\text{ V}$, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 50 mA.

6. IN voltage equals $V_O(\text{Typ}) - 100\text{mV}$; TPS77001 output voltage set to 3.3 V nominal with external resistor divider. TPS77012, TPS77015, TPS77018, TPS77025, and TPS77027 dropout voltage limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	1, 2, 3
		vs Free-air temperature	4, 5, 6
	Ground current	vs Free-air temperature	7
	Output spectral noise density	vs Frequency	8
Z_O	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Free-air temperature	10
		Ripple rejection	vs Frequency
	LDO startup time		12
	Line transient response		13, 15
	Load transient response		14, 16
	Equivalent series resistance (ESR)	vs Output current	17, 19
		vs Added ceramic capacitance	18, 20

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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TYPICAL CHARACTERISTICS

**TPS77025
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

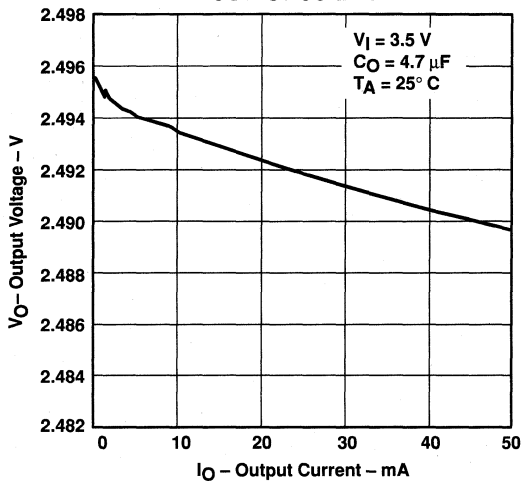


Figure 1

**TPS77015
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

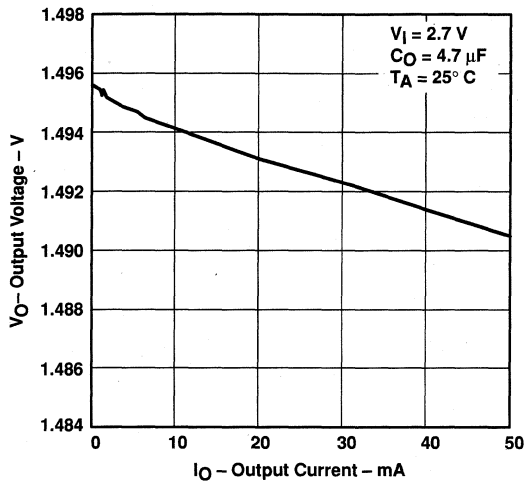


Figure 2

**TPS77033
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT**

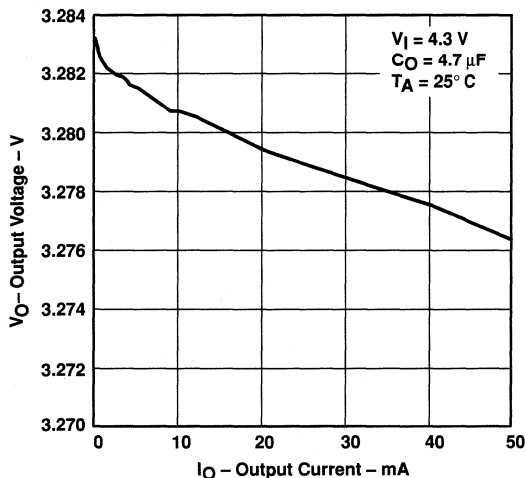


Figure 3

**TPS77015
 OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE**

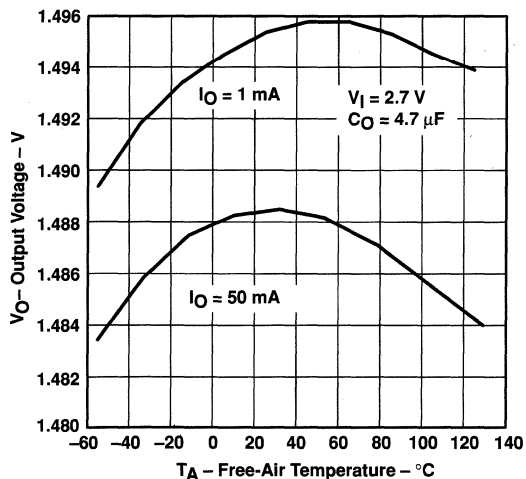


Figure 4



TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

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TYPICAL CHARACTERISTICS

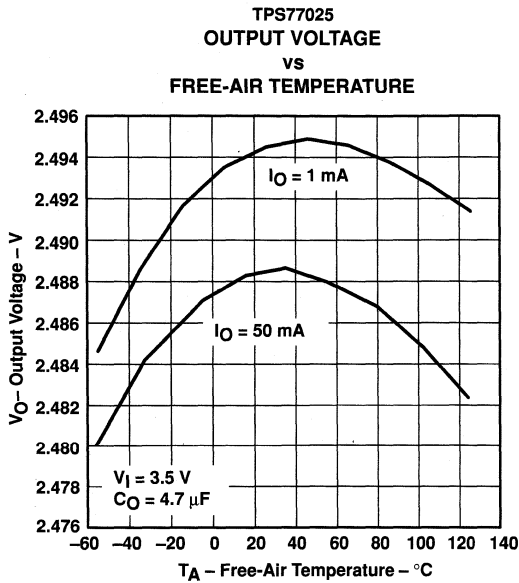


Figure 5

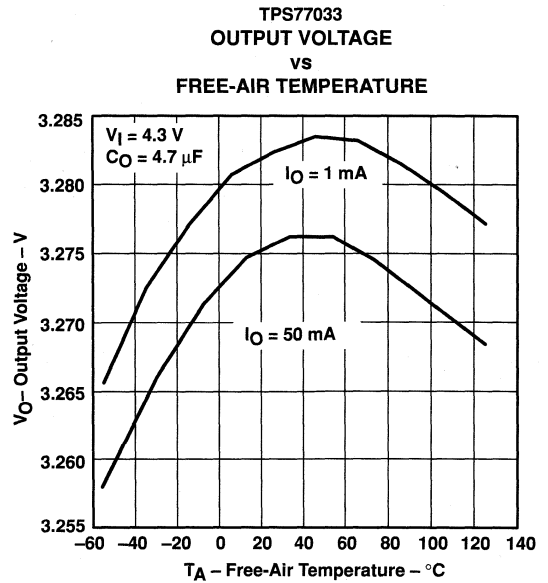


Figure 6

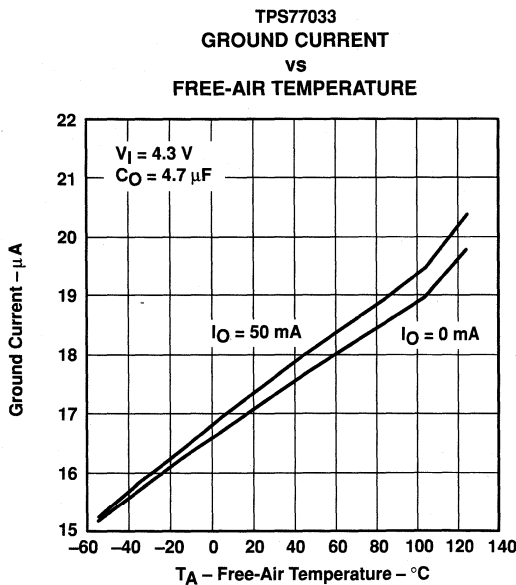


Figure 7

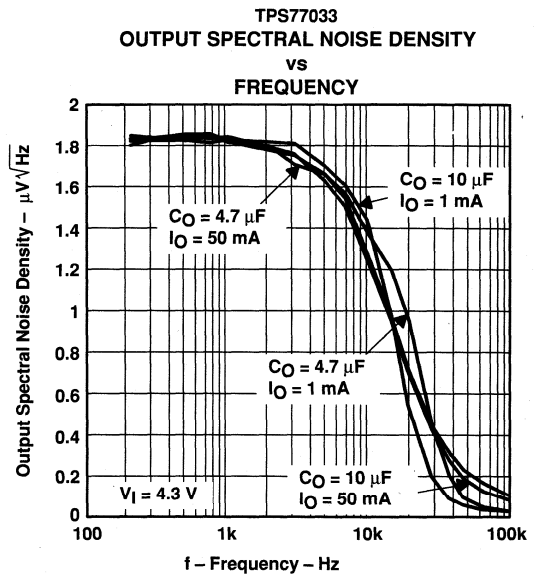


Figure 8

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
 vs
 FREQUENCY

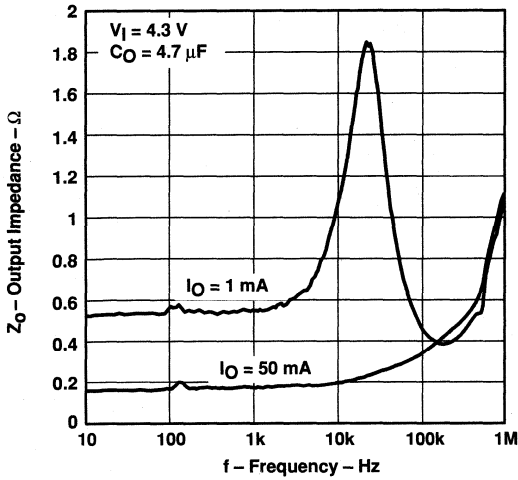


Figure 9

TPS77033
 DROPOUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

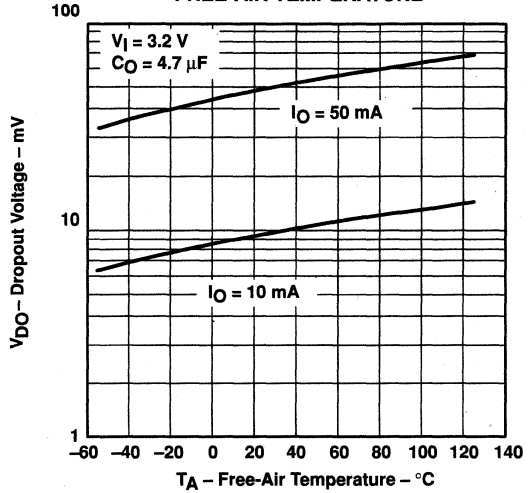


Figure 10

TPS77033
 RIPPLE REJECTION
 vs
 FREQUENCY

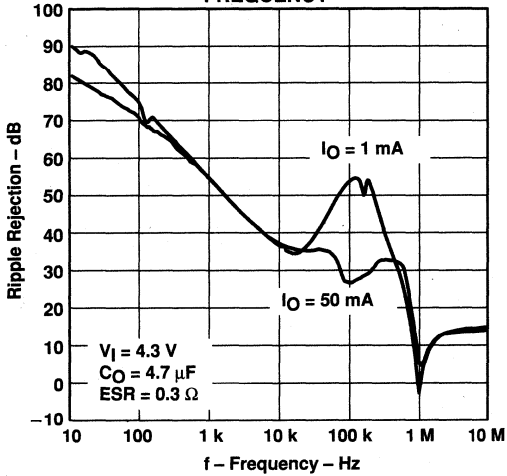


Figure 11

LDO STARTUP TIME

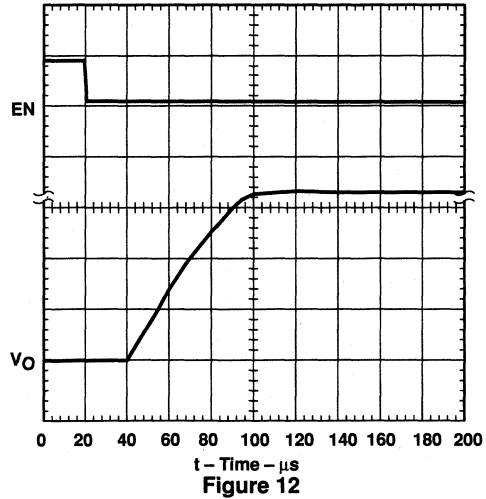


Figure 12

TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS
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TYPICAL CHARACTERISTICS

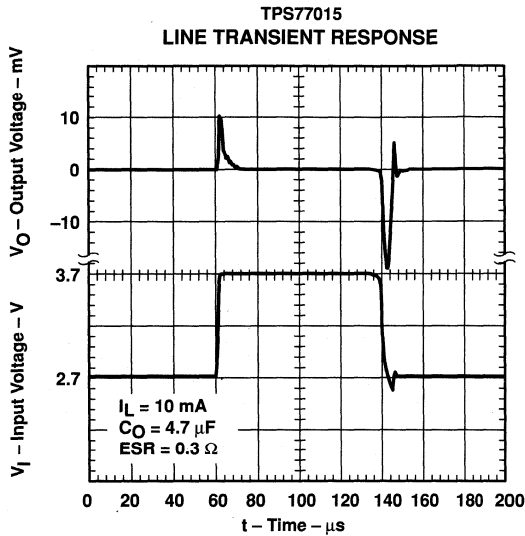


Figure 13

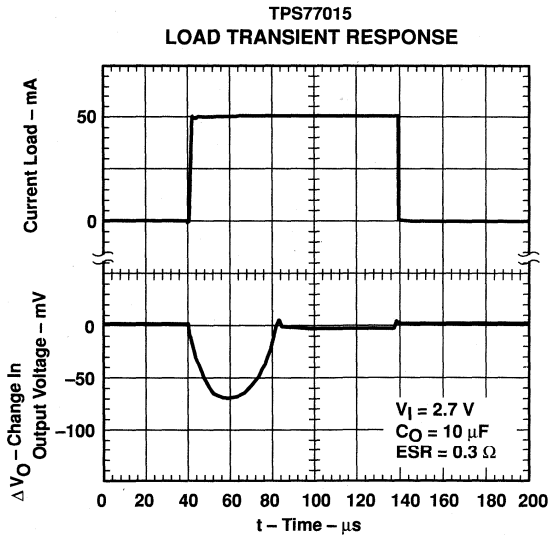


Figure 14

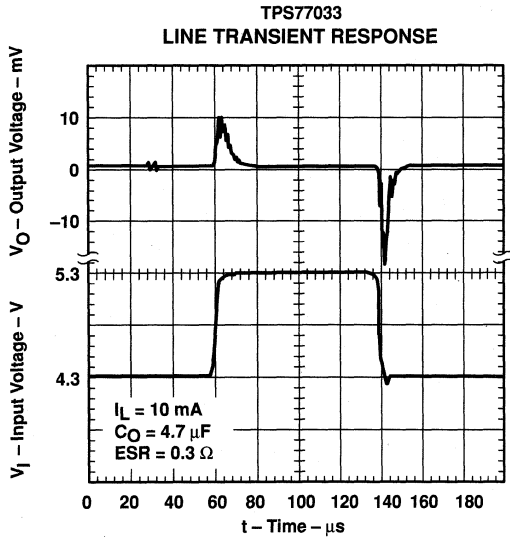


Figure 15

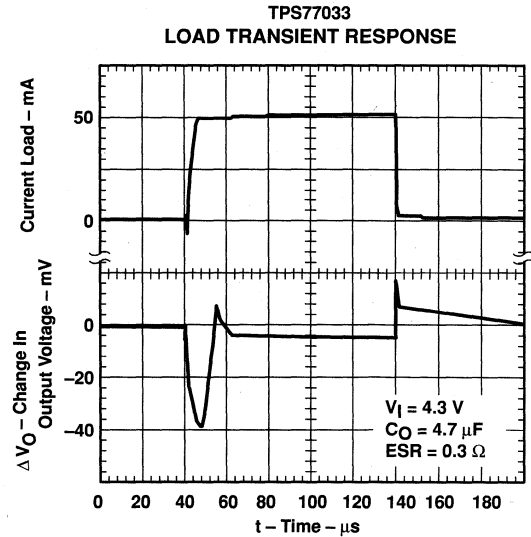


Figure 16

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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TYPICAL CHARACTERISTICS

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)[†]
 vs
 OUTPUT CURRENT

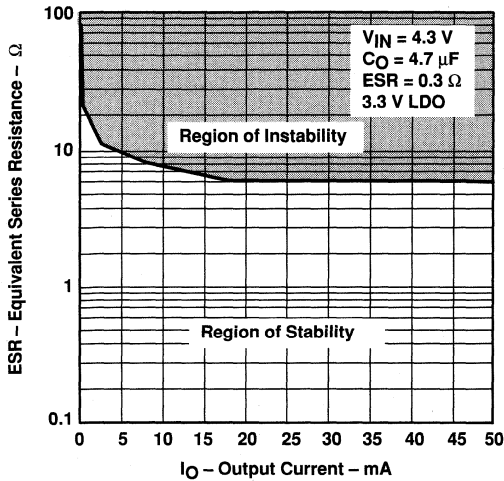


Figure 17

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)
 vs
 ADDED CERAMIC CAPACITANCE

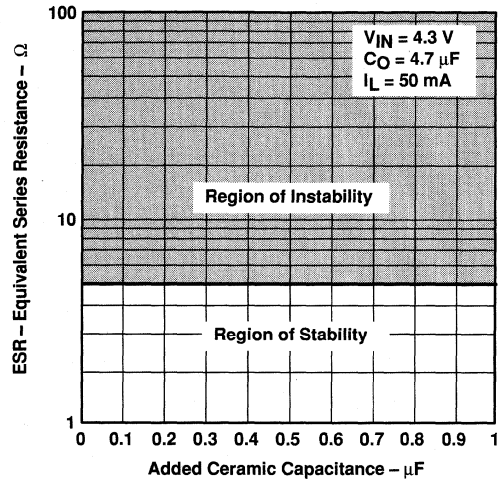


Figure 18

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)[†]
 vs
 OUTPUT CURRENT

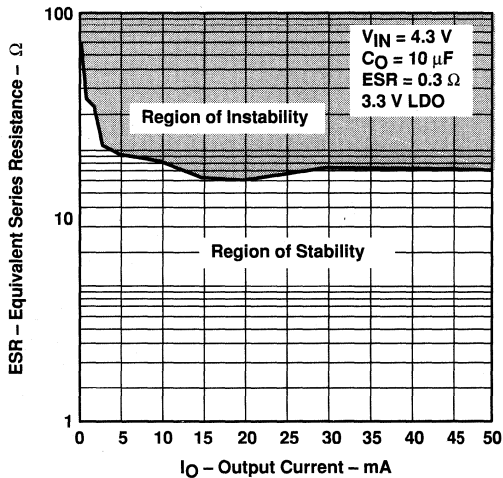


Figure 19

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)
 vs
 ADDED CERAMIC CAPACITANCE

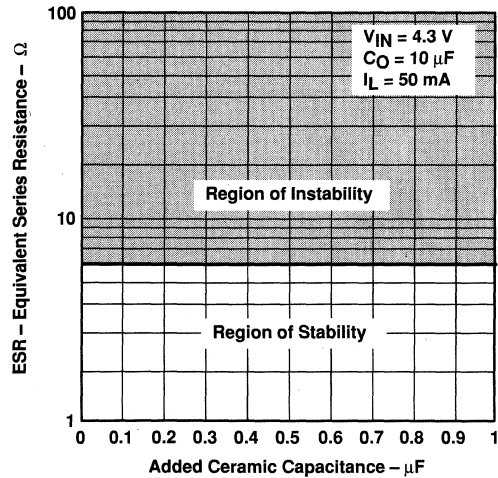


Figure 20



APPLICATION INFORMATION

The TPS770xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low quiescent current (17 μA nominally), and enable inputs to reduce supply currents to less than 1 μA when the regulators are turned off.

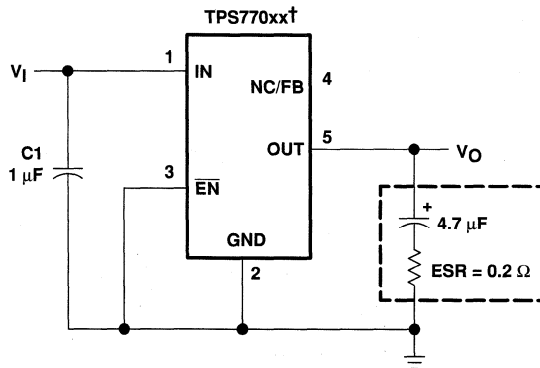
device operation

The TPS770xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS770xx is essentially constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the EN input will disable the TPS770xx internal circuitry, reducing the supply current to 1 μA . A voltage of less than 0.9 V on the $\overline{\text{EN}}$ input will enable the TPS770xx and will enable normal operation to resume. The $\overline{\text{EN}}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in Figure 21.



† TPS77012, TPS77015, TPS77018, TPS77025, TPS77027, TPS77028, TPS77030, TPS77033, TPS77050 (fixed-voltage options).

Figure 21. Typical Application Circuit

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047- μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS770xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS770xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μF . The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω to ensure stability. Capacitor values larger than 4.7 μF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H \times L \times W)†
T494B475K016AS	KEMET	4.7 μF	1.5 Ω	1.9 \times 3.5 \times 2.8
195D106x0016x2T	SPRAGUE	10 μF	1.5 Ω	1.3 \times 7.0 \times 2.7
695D106x003562T	SPRAGUE	10 μF	1.3 Ω	2.5 \times 7.6 \times 2.5
TPSC475K035R0600	AVX	4.7 μF	0.6 Ω	2.6 \times 6.0 \times 3.2

† Size is in mm. ESR is maximum resistance in Ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Contact manufacturer for minimum ESR values.



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APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS77001 adjustable regulator is programmed using an external resistor divider as shown in Figure 22. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

$$V_{ref} = 1.224 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 k Ω to set the divider current at 7 μ A and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

OUTPUT VOLTAGE PROGRAMMING GUIDE		
OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (k Ω) [‡]	
	R1	R2
2.5	174	169
3.3	287	169
3.6	324	169
4.0	383	169
5.0	523	169

[‡] 1% values shown.

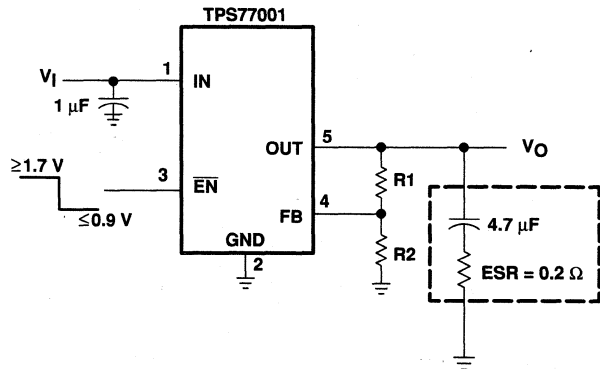


Figure 22. TPS77001 Adjustable LDO Regulator Programming

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRA LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

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APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 285°C/W for the 5-terminal SOT23.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

regulator protection

The TPS770xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS770xx features internal current limiting and thermal protection. During normal operation, the TPS770xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

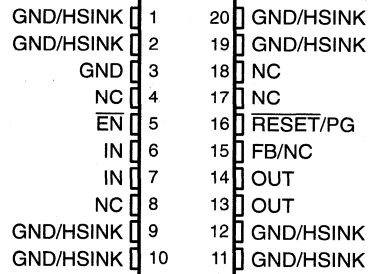
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- Open Drain Power-On Reset With 200-ms Delay (TPS775xx)
- Open Drain Power Good (TPS776xx)
- 500-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V Fixed Output and Adjustable Versions
- Dropout Voltage to 169 mV (Typ) at 500 mA (TPS77x33)
- Ultra Low 85 μ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

description

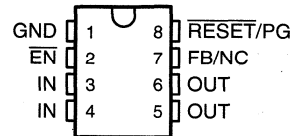
The TPS775xx and TPS776xx devices are designed to have a fast transient response and be stable with a 10- μ F low ESR capacitors. This combination provides high performance at a reasonable cost.

**PWP PACKAGE
(TOP VIEW)**

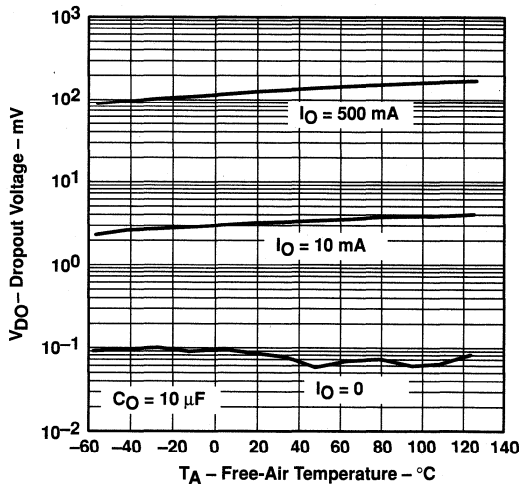


NC – No internal connection

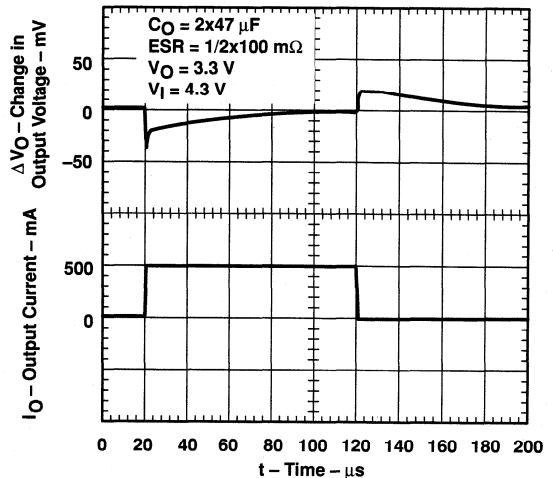
**D PACKAGE
(TOP VIEW)**



**TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



**TPS77x33
LOAD TRANSIENT RESPONSE**



PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 169 mV at an output current of 500 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = 25^\circ\text{C}$.

The \overline{RESET} output of the TPS775xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS775xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

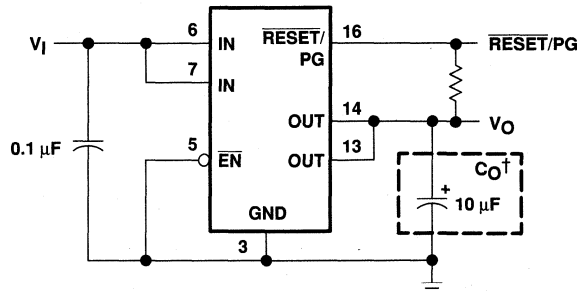
Power good (PG) of the TPS776xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS775xx and TPS776xx are offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for TPS77501 option and 1.2 V to 5.5 V for TPS77601 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS775xx and TPS776xx families are available in 8 pin SOIC and 20 pin TSSOP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES			
	TYP	TSSOP (PWP)		SOIC (D)	
-40°C to 125°C	3.3	TPS77533PWP	TPS77633PWP	TPS77533D	TPS77633D
	2.5	TPS77525PWP	TPS77625PWP	TPS77525D	TPS77625D
	1.8	TPS77518PWP	TPS77618PWP	TPS77518D	TPS77618D
	1.5	TPS77515PWP	TPS77615PWP	TPS77515D	TPS77615D
	Adjustable 1.2 V to 5.5 V	—	TPS77601PWP	—	TPS77601D
	Adjustable 1.5 V to 5.5 V	TPS77501PWP	—	TPS77501D	—

The TPS77x01 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS77501DR).



† See application information section for capacitor selection details.

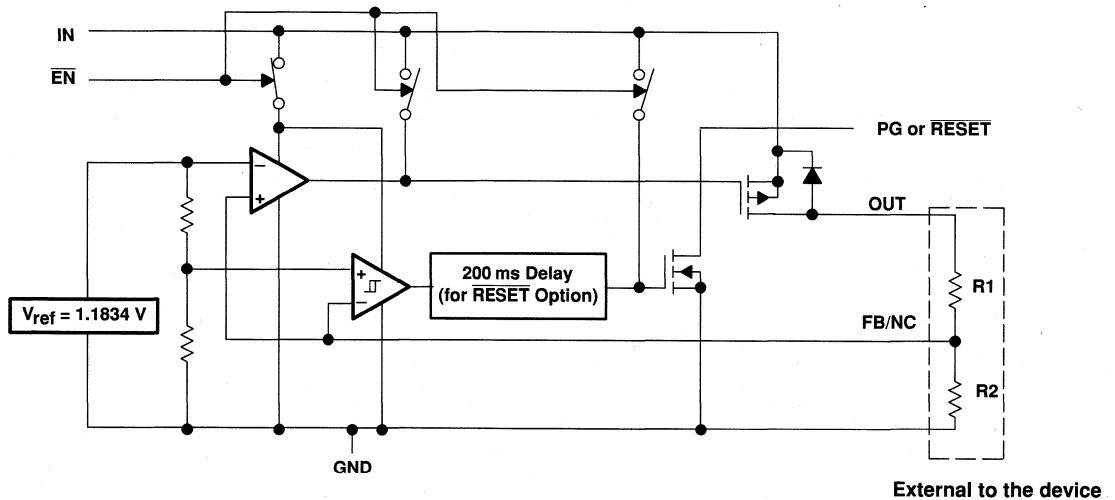
Figure 1. Typical Application Configuration for Fixed Output Options



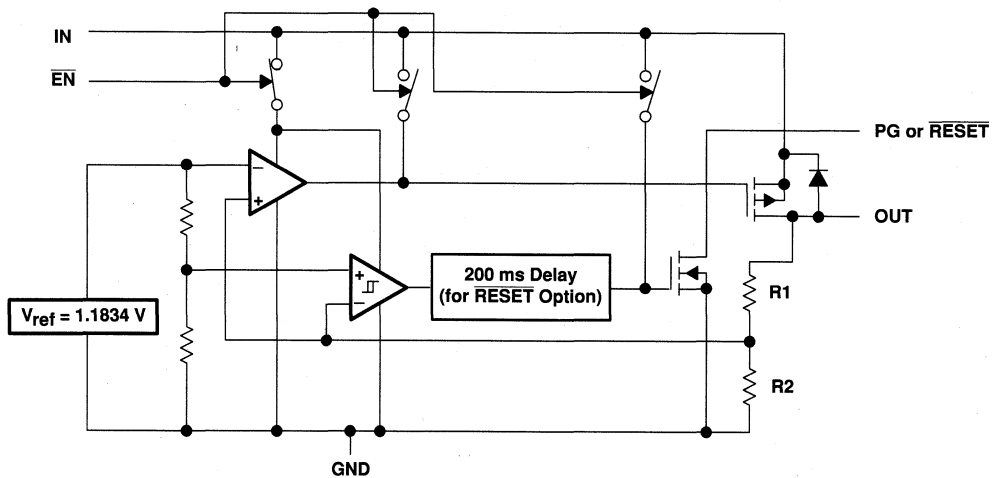
TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
 TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



**TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
 TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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Terminal Functions – SOIC Package (TPS775xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
RESET	8	O	RESET output

Terminal Functions – TSSOP Package (TPS775xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
RESET	16	O	RESET output

Terminal Functions – SOIC Package (TPS776xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
PG	8	O	PG output

Terminal Functions – TSSOP Package (TPS776xx)

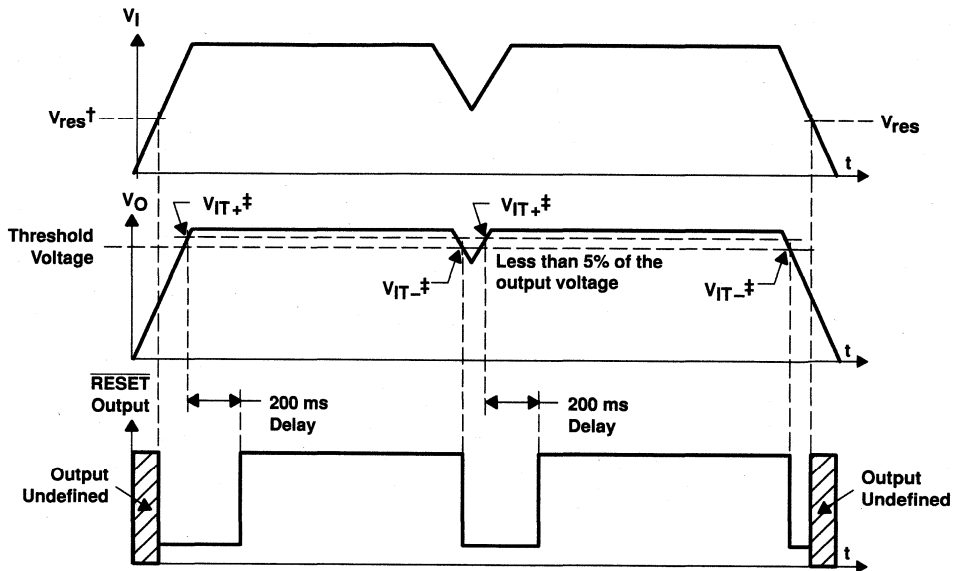
TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output



TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH $\overline{\text{RESET}}$ OUTPUT
 TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
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TPS775xx $\overline{\text{RESET}}$ timing diagram



† V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ $V_{\text{IT-}}$ Trip voltage is typically 5% lower than the output voltage ($95\%V_{\text{O}}$). $V_{\text{IT-}}$ to $V_{\text{IT+}}$ is the hysteresis voltage.

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	-0.3 V to 13.5 V
Voltage range at \overline{EN}	-0.3 V to 16.5 V
Maximum \overline{RESET} voltage (TPS775xx)	16.5 V
Maximum PG voltage (TPS776xx)	16.5 V
Peak output current	Internally limited
Output voltage, V_O (OUT, FB)	7 V
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWPll	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

ll This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to T1 technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT	
Input voltage, V_I ★	2.7	10	V	
Output voltage range, V_O	TPS77501	1.5	5.5	V
	TPS77601	1.2	5.5	
Output current, I_O (Note 1)	0	500	mA	
Operating virtual junction temperature, T_J (Note 1)	-40	125	°C	

★ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_I(\text{min}) = V_O(\text{max}) + V_{DO}(\text{max load})$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 500 mA load) (see Note 2)	TPS77501	$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$		V_O		V
		$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	0.98 V_O		1.02 V_O	
	TPS77601	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$		V_O		
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	0.98 V_O		1.02 V_O	
	TPS77x15	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.470		1.530	
	TPS77x18	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.8		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.764		1.836	
	TPS77x25	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.450		2.550	
TPS77x33	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.3			
	$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.234		3.366		
Quiescent current (GND current) $\overline{\text{EN}} = 0 \text{ V}$, (see Note 2)		$10 \mu\text{A} < I_O < 500 \text{ mA}$, $T_J = 25^\circ\text{C}$		85		μA
		$I_O = 500 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			125	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$		0.01		%/V
Load regulation				3		mV
Output noise voltage		BW = 300 Hz to 50 kHz, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		190		μV_{rms}
Output current Limit		$V_O = 0 \text{ V}$		1.7	2	A
Thermal shutdown junction temperature				150		$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_I$, $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_I < 10 \text{ V}$		1		μA
		$\overline{\text{EN}} = V_I$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_I < 10 \text{ V}$			10	μA
FB input current	TPS77x01	FB = 1.5 V		2		nA
High level enable input voltage				1.7		V
Low level enable input voltage					0.9	V
Power supply ripple rejection (see Note 2)		$f = 1 \text{ KHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		60		dB
Reset (TPS775xx)	Minimum input voltage for valid RESET	$I_O(\text{RESET}) = 300\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7 \text{ V}$, $I_O(\text{RESET}) = 1 \text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{RESET}) = 5 \text{ V}$			1	μA
	RESET time-out delay			200		ms
PG (TPS776xx)	Minimum input voltage for valid PG	$I_O(\text{PG}) = 300\mu\text{A}$		1.1		V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$V_I = 2.7 \text{ V}$, $I_O(\text{PG}) = 1 \text{ mA}$		0.15	0.4	V
	Leakage current	$V(\text{PG}) = 5 \text{ V}$			1	μA

NOTE 2: Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10V.



TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
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electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input current (EN)		$\overline{\text{EN}} = 0 \text{ V}$		-1	0	1	μA
		$\overline{\text{EN}} = V_i$		-1		1	
Dropout voltage (See Note 4)		TPS77533	$I_O = 500 \text{ mA}$, $T_J = 25^\circ\text{C}$			169	mV
			$I_O = 500 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			287	
		TPS77633	$I_O = 500 \text{ mA}$, $T_J = 25^\circ\text{C}$			169	mV
			$I_O = 500 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			287	

NOTES: 3. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imin}} = 2.7 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imin}} = V_O + 1 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

4. IN voltage equals $V_{O(\text{Typ})} - 100 \text{ mV}$; TPS77x15, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
Z_O	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Line transient response		14, 16
	Load transient response		15, 17
	Output voltage	vs Time	18
	Equivalent series resistance (ESR)	vs Output current	20 – 23

**TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
 TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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TYPICAL CHARACTERISTICS

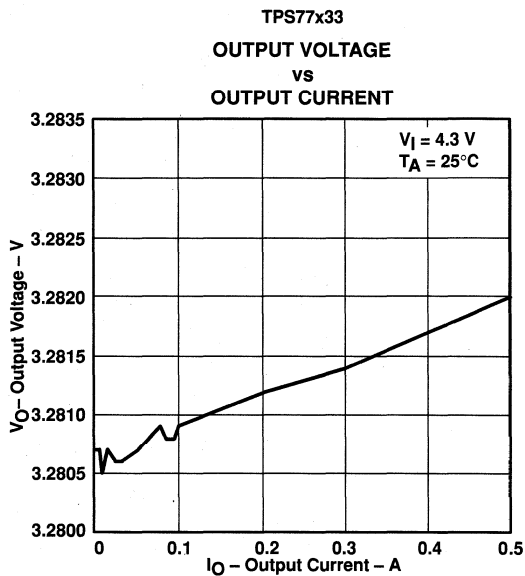


Figure 2

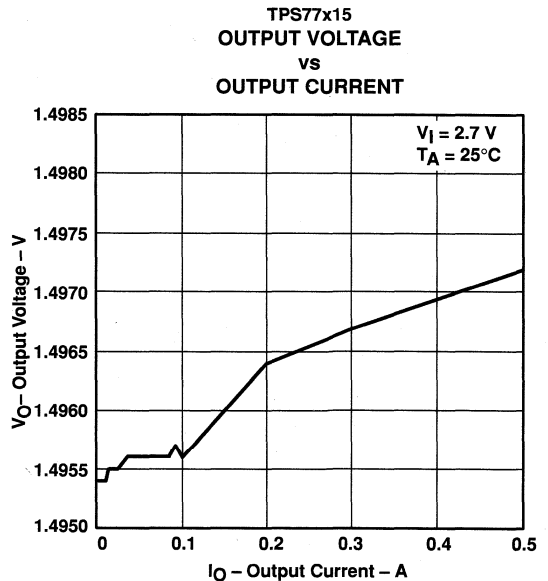


Figure 3

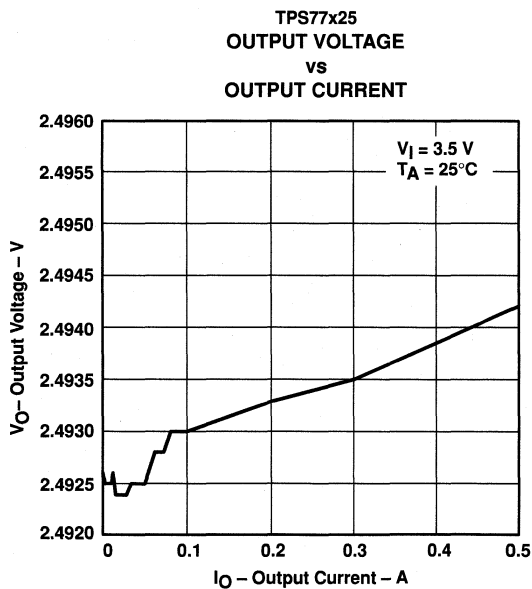


Figure 4

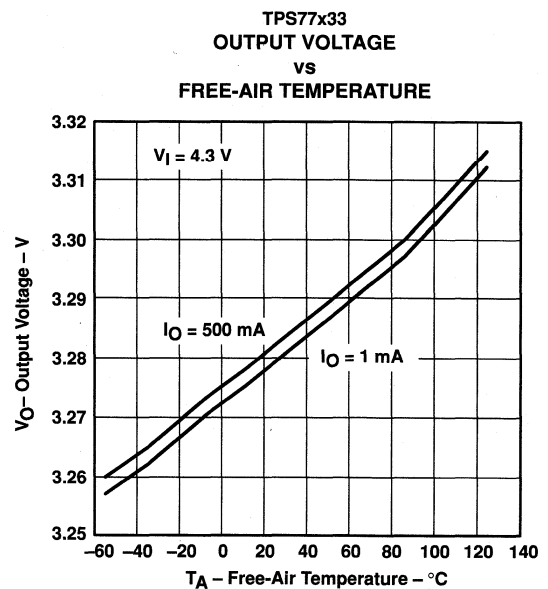


Figure 5



TYPICAL CHARACTERISTICS

TPS77x15
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

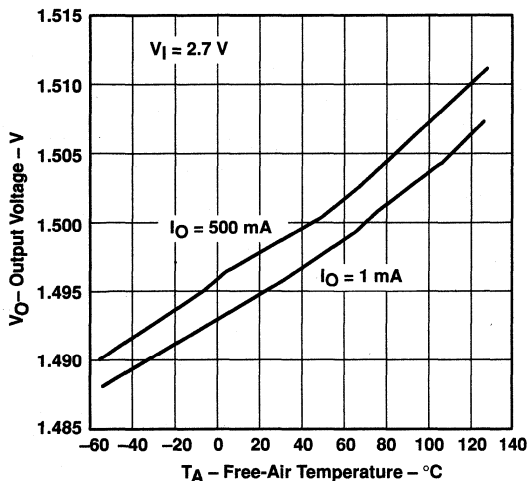


Figure 6

TPS77x25
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

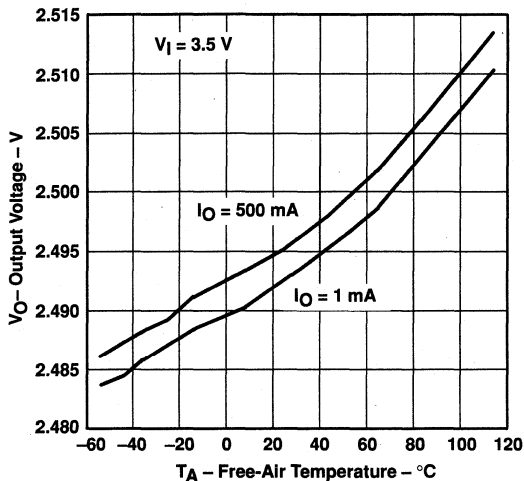


Figure 7

TPS77xxx
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

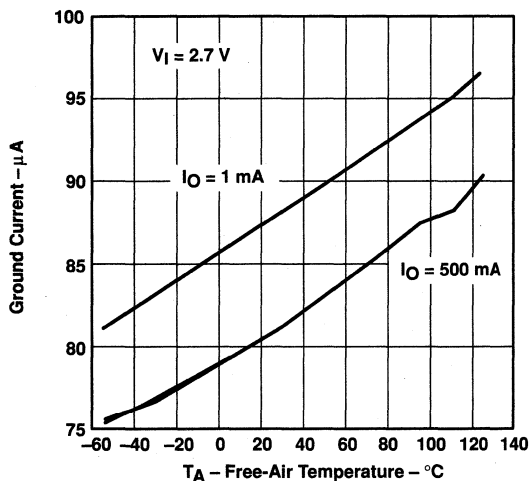


Figure 8

TPS77x33
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

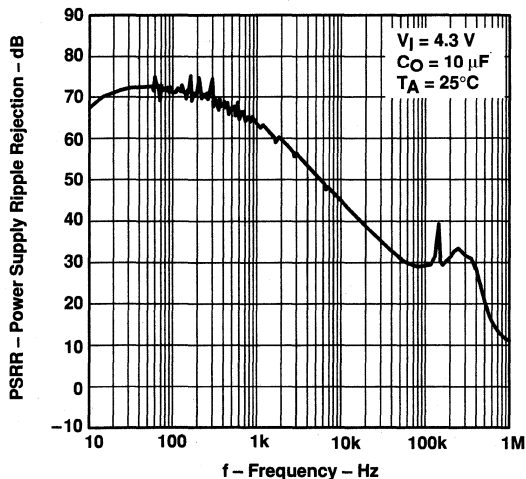


Figure 9

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
 TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

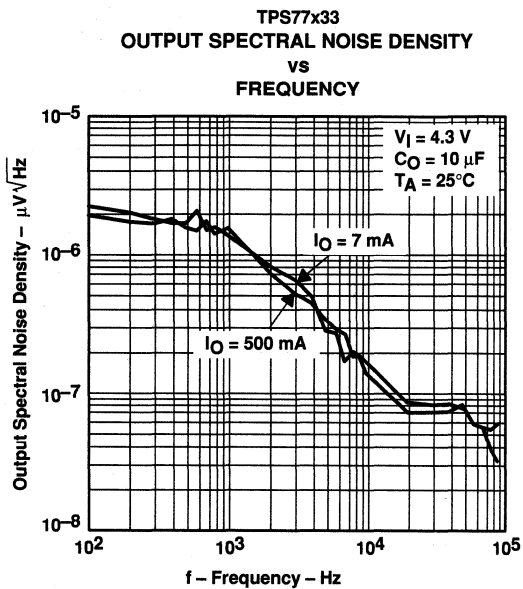


Figure 10

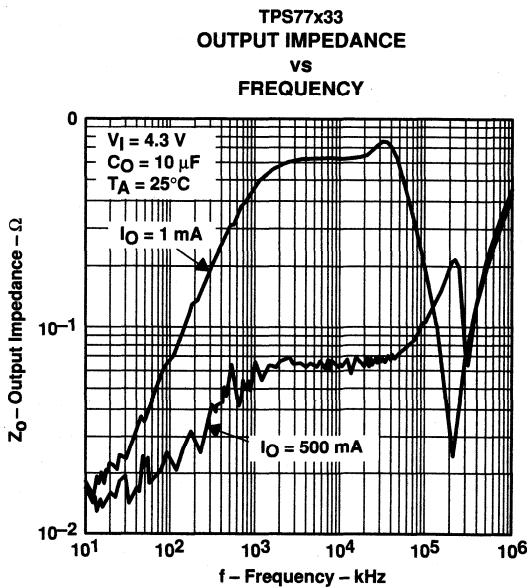


Figure 11

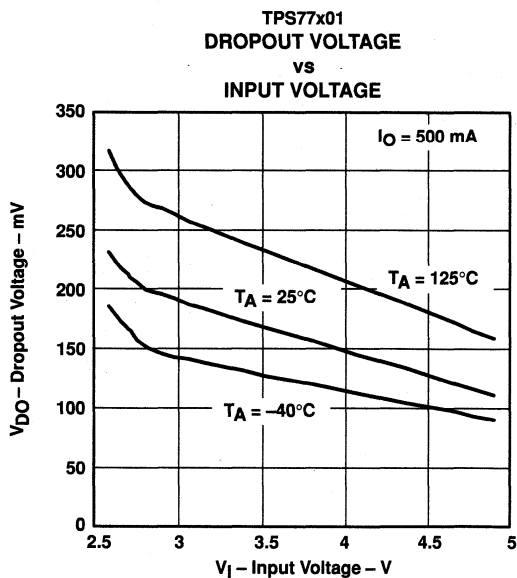


Figure 12

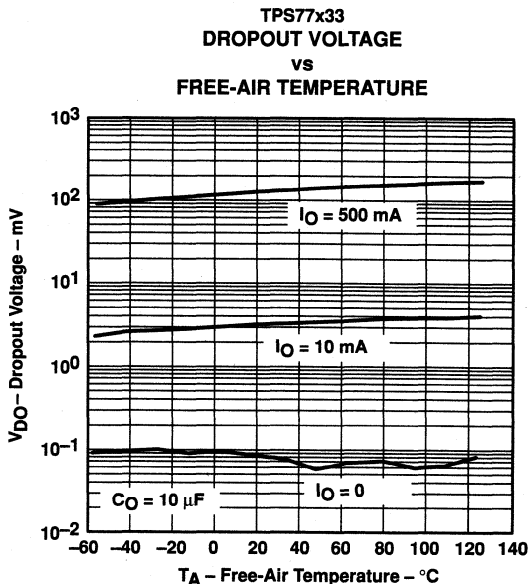


Figure 13

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TPS77x15
LINE TRANSIENT RESPONSE

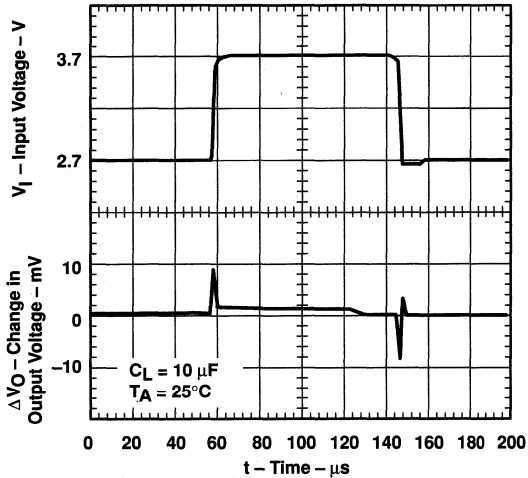


Figure 14

TPS77x15
LOAD TRANSIENT RESPONSE

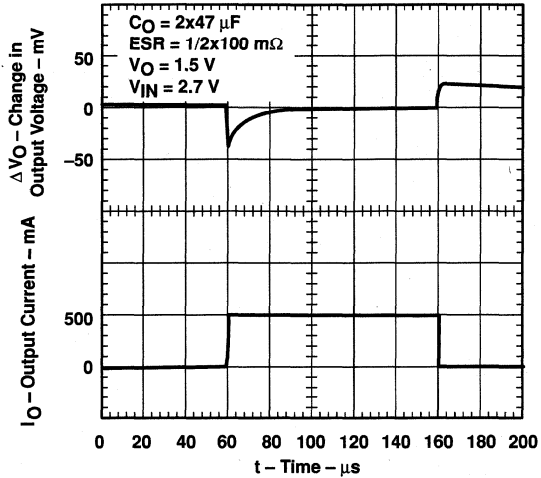


Figure 15

TPS77x33
LINE TRANSIENT RESPONSE

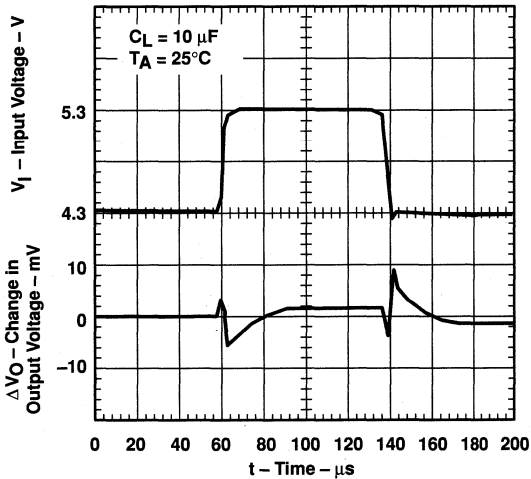


Figure 16

TPS77x33
LOAD TRANSIENT RESPONSE

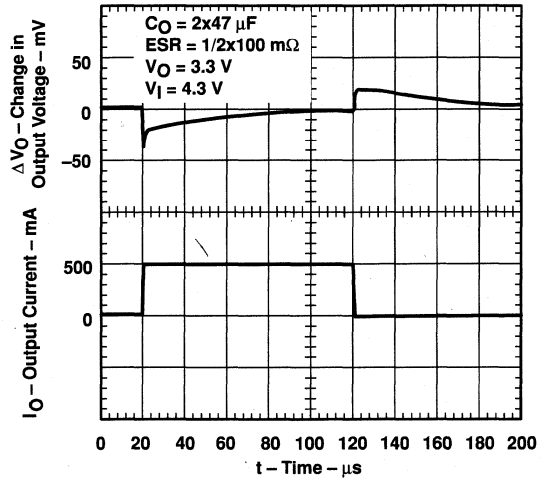


Figure 17



**TEXAS
INSTRUMENTS**

TYPICAL CHARACTERISTICS

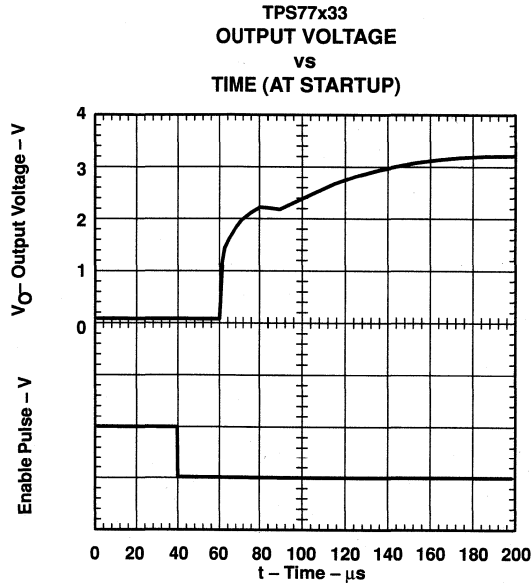


Figure 18

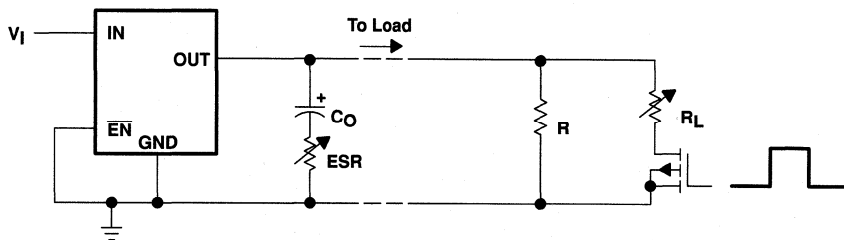


Figure 19. Test Circuit for Typical Regions of Stability (Figures 20 through 23) (Fixed Output Options)

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

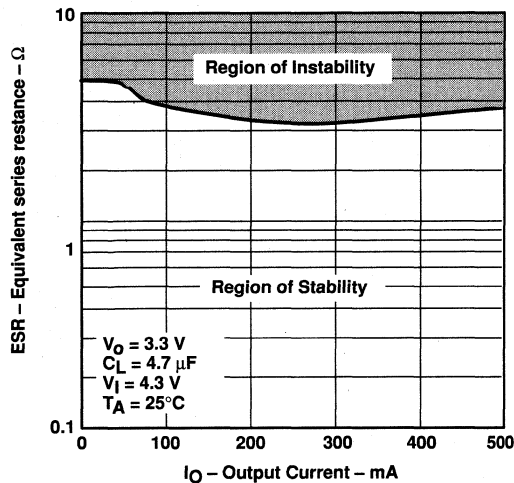


Figure 20

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

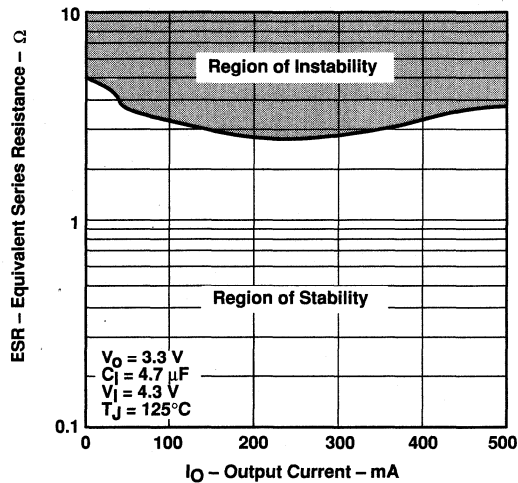


Figure 21

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

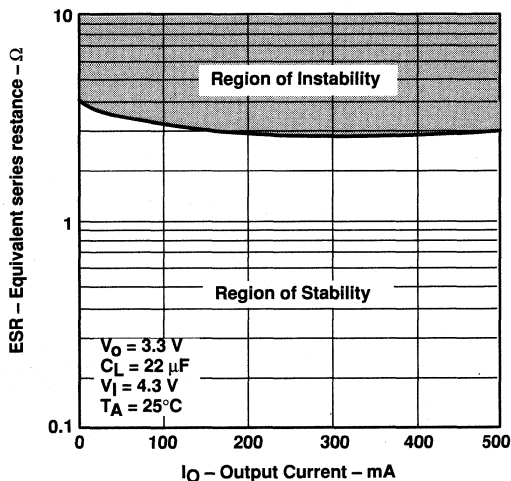


Figure 22

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

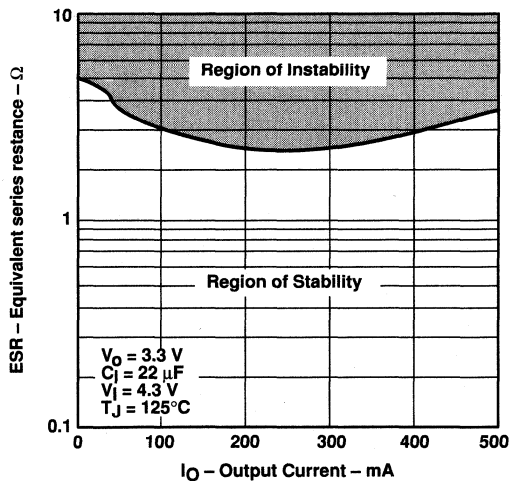


Figure 23

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

The TPS775xx and TPS776xx families include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77x01 (adjustable from 1.5 V to 5.5 V for TPS77501 option and 1.2 V to 5.5 V for TPS77601 option).

device operation

The TPS775xx and TPS776xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS775xx and TPS776xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS775xx and TPS776xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS775xx and TPS776xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μ A. If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μ s.

minimum load requirements

The TPS775xx and TPS776xx families are stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 25. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS775xx or TPS776xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS775xx and TPS776xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μ F and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μ F or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
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APPLICATION INFORMATION

external capacitor requirements (continued)

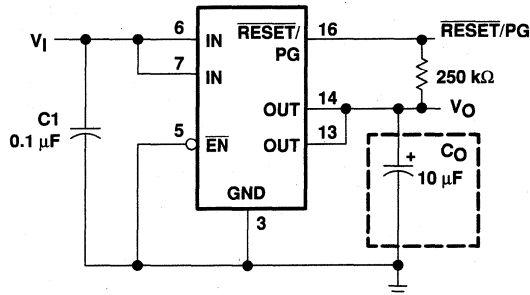


Figure 24. Typical Application Circuit (Fixed Versions)

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 110 kΩ to set the divider current at approximately 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

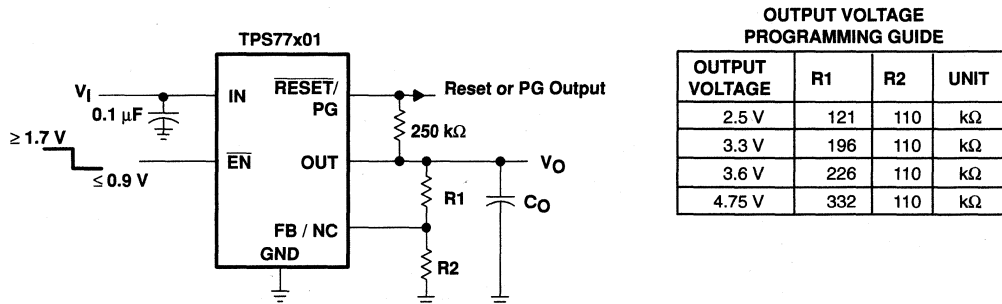


Figure 25. TPS77x01 Adjustable LDO Regulator Programming

**TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH $\overline{\text{RESET}}$ OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 500-mA LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

reset indicator

The TPS775xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

power-good indicator

The TPS776xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS775xx and TPS776xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS775xx and TPS776xx also feature internal current limiting and thermal protection. During normal operation, the TPS775xx and TPS776xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

TPS77501, TPS77515, TPS77518, TPS77525, TPS77533 WITH RESET OUTPUT
TPS77601, TPS77615, TPS77618, TPS77625, TPS77633 WITH PG OUTPUT
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APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

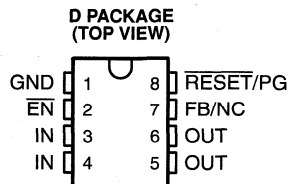
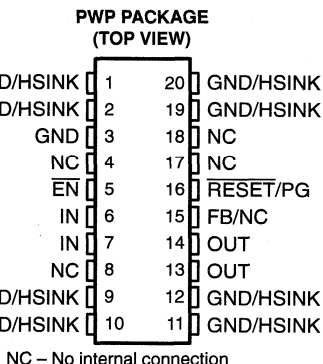
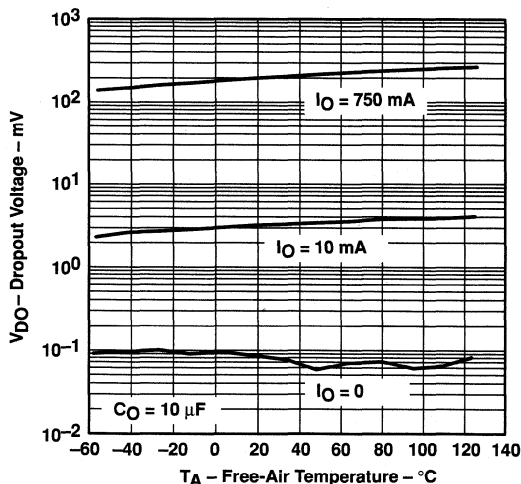
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- Open Drain Power-On Reset With 200-ms Delay (TPS777xx)
- Open Drain Power Good (TPS778xx)
- 750-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V Fixed Output and Adjustable Versions
- Dropout Voltage to 260 mV (Typ) at 750 mA (TPS77x33)
- Ultra Low 85 μ A Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- 8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package
- Thermal Shutdown Protection

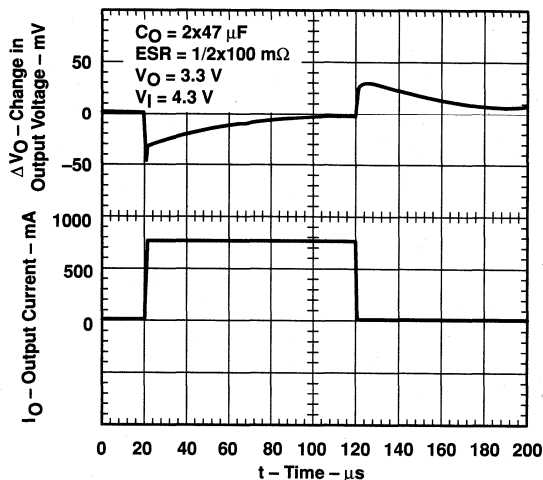
description

TPS777xx and TPS778xx are designed to have a fast transient response and be stable with a 10- μ F low ESR capacitors. This combination provides high performance at a reasonable cost.

**TPS77x33
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE**



**TPS77x33
LOAD TRANSIENT RESPONSE**



PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 260 mV at an output current of 750 mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μ A over the full range of output current, 0 mA to 750 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to \overline{EN} (enable) shuts down the regulator, reducing the quiescent current to 1 μ A at $T_J = 25^\circ\text{C}$.

The \overline{RESET} output of the TPS777xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS777xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

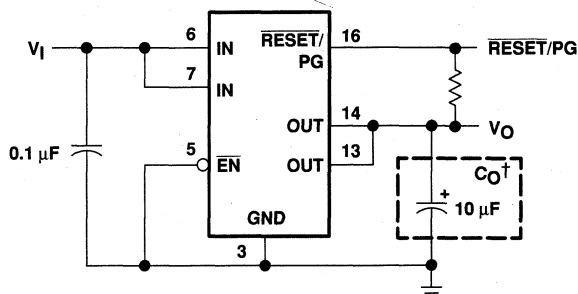
Power good (PG) of the TPS778xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS777xx and TPS778xx are offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V for TPS77701 option and 1.2 V to 5.5 V for TPS77801 option). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS777xx and TPS778xx families are available in 8 pin SOIC and 20 pin PWP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES			
		TYP	TSSOP (PWP)		SOIC (D)
-40°C to 125°C	3.3	TPS77733PWP	TPS77833PWP	TPS77733D	TPS77833D
	2.5	TPS77725PWP	TPS77825PWP	TPS77725D	TPS77825D
	1.8	TPS77718PWP	TPS77818PWP	TPS77718D	TPS77818D
	1.5	TPS77715PWP	TPS77815PWP	TPS77715D	TPS77815D
	Adjustable 1.5 V to 5.5 V	TPS77701PWP	—	TPS77701D	—
	Adjustable 1.2 V to 5.5 V	—	TPS77801PWP	—	TPS77801D

The TPS77x01 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS77701DR).



† See application information section for capacitor selection details.

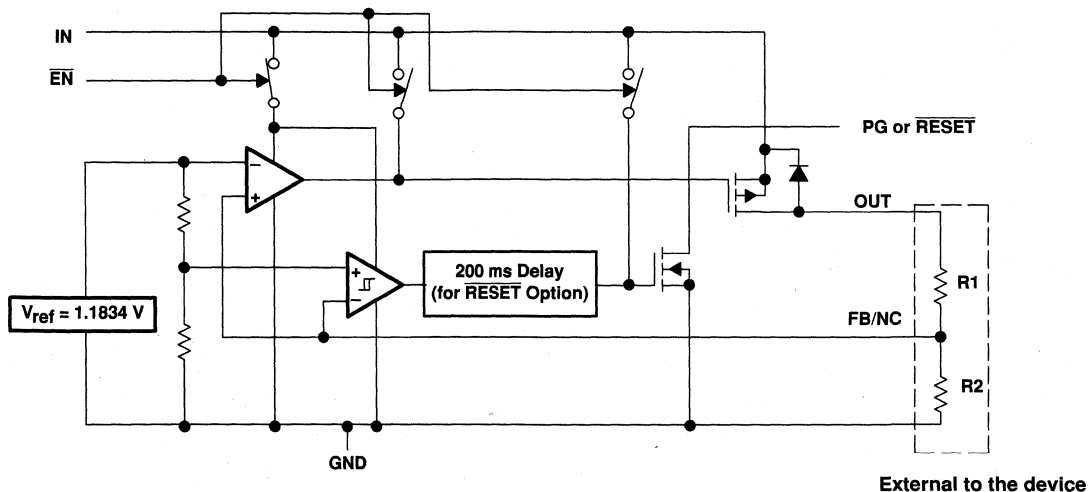
Figure 1. Typical Application Configuration for Fixed Output Options



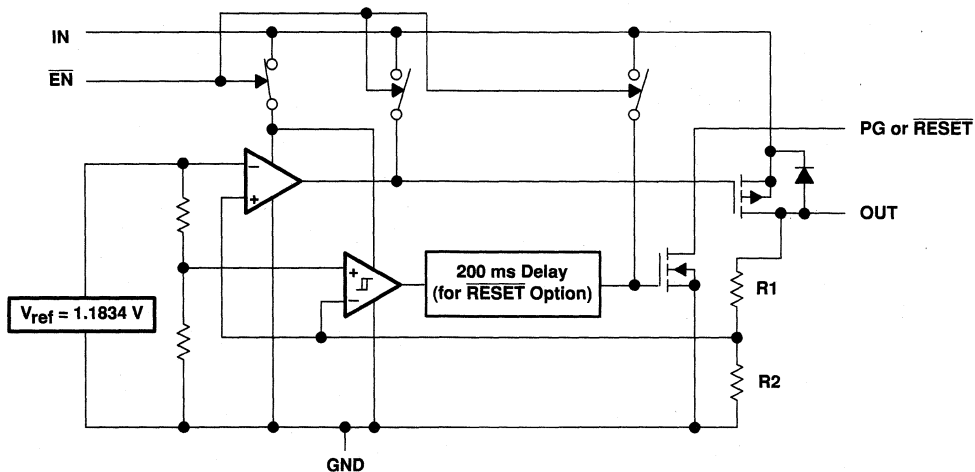
TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
 TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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functional block diagram—adjustable version



functional block diagram—fixed-voltage version



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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Terminal Functions – SOIC Package (TPS777xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
RESET	8	O	RESET output

Terminal Functions – TSSOP Package (TPS777xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
RESET	16	O	RESET output

Terminal Functions – SOIC Package (TPS778xx)

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
PG	8	O	PG output

Terminal Functions – TSSOP Package (TPS778xx)

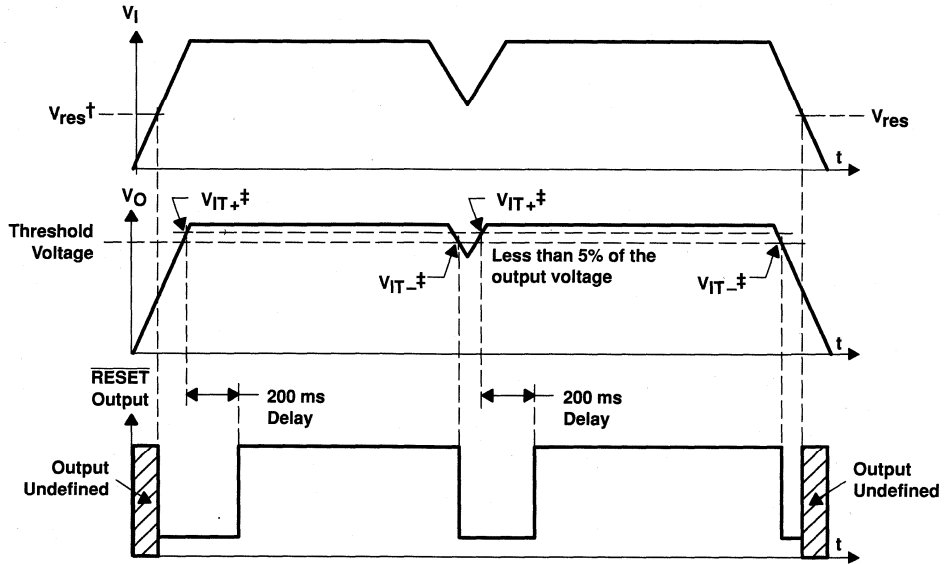
TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	PG output



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH $\overline{\text{RESET}}$ OUTPUT
 TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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TPS777xx $\overline{\text{RESET}}$ timing diagram



† V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ V_{IT-} Trip voltage is typically 5% lower than the output voltage ($95\%V_o$). V_{IT-} to V_{IT+} is the hysteresis voltage.

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I	-0.3 V to 13.5 V
Voltage range at \overline{EN}	-0.3 V to 16.5 V
Maximum RESET voltage (TPS777xx)	16.5 V
Maximum PG voltage (TPS778xx)	16.5 V
Peak output current	Internally limited
Output voltage, V_O (OUT, FB)	7 V
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
ESD rating, HBM	2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in x 5-in PCB, 1 oz. copper, 2-in x 2-in coverage (4 in²).

|| This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in x 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I ★	2.7	10	V
Output voltage range, V_O	TPS77701	1.5	5.5
	TPS77801	1.2	5.5
Output current, I_O (Note 1)	0	750	mA
Operating virtual junction temperature, T_J (Note 1)	-40	125	°C

★ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max load)}$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 750 mA load) (see Note 2)	TPS77701	$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$	V_O			
		$1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	$0.98V_O$		$1.02V_O$	
	TPS77801	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$	V_O			
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	$0.98V_O$		$1.02V_O$	
	TPS77x15	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.470		1.530	
	TPS77x18	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.8			
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.764		1.836	
	TPS77x25	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.5			
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.450		2.550	
TPS77x33	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.3				
	$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.234		3.366		
Quiescent current (GND current) (see Note 2)		$10 \mu\text{A} < I_O < 750 \text{ mA}$, $T_J = 25^\circ\text{C}$	85			μA
		$I_O = 750 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C	125			
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		$V_O + 1 \text{ V} < V_i \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$	0.01			%/V
Load regulation			3			mV
Output noise voltage		BW = 300 Hz to 50 kHz, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	190			μVrms
Output current Limit		$V_O = 0 \text{ V}$	1.7		2	A
Thermal shutdown junction temperature			150			$^\circ\text{C}$
Standby current		$\overline{\text{EN}} = V_i$, $T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_i < 10 \text{ V}$	1			μA
		$\overline{\text{EN}} = V_i$, $T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_i < 10 \text{ V}$	10			μA
FB input current	TPS77x01	FB = 1.5 V	2			nA
High level enable input voltage			1.7			V
Low level enable input voltage			0.9			V
Power supply ripple rejection (see Note 2)		$f = 1 \text{ KHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$	60			dB
Reset (TPS777xx)	Minimum input voltage for valid RESET	$I_{O(\text{RESET})} = 300 \mu\text{A}$	1.1			V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O	0.5			% V_O
	Output low voltage	$V_i = 2.7 \text{ V}$, $I_{O(\text{RESET})} = 1 \text{ mA}$	0.15		0.4	V
	Leakage current	$V(\text{RESET}) = 5 \text{ V}$			1	μA
	RESET time-out delay		200			ms
PG (TPS778xx)	Minimum input voltage for valid PG	$I_{O(\text{PG})} = 300 \mu\text{A}$	1.1			V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O	0.5			% V_O
	Output low voltage	$V_i = 2.7 \text{ V}$, $I_{O(\text{PG})} = 1 \text{ mA}$	0.15		0.4	V
	Leakage current	$V(\text{PG}) = 5 \text{ V}$			1	μA

NOTE 2: Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10V.



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 10 \mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current (EN)		$\overline{\text{EN}} = 0 \text{ V}$	-1	0	1	μA
		$\overline{\text{EN}} = V_I$	-1		1	
Dropout voltage (See Note 4)	TPS77733	$I_O = 750 \text{ mA}$, $T_J = 25^\circ\text{C}$		260		mV
		$I_O = 750 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			427	
	TPS77833	$I_O = 750 \text{ mA}$, $T_J = 25^\circ\text{C}$		260		
		$I_O = 750 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			427	

NOTES: 3. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{imin}} = 2.7 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O (V_{\text{imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imin}} = V_O + 1 \text{ V}$, $V_{\text{imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O (V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

4. IN voltage equals $V_{O(\text{Typ})} - 100 \text{ mV}$; TPS77x01 output voltage set to 3.3 V nominal with external resistor divider. TPS77x15, TPS77x18, and TPS77x25 dropout voltage limited by input voltage range limitations (i.e., TPS77x33 input voltage needs to drop to 3.2 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8
	Power supply ripple rejection	vs Frequency	9
	Output spectral noise density	vs Frequency	10
Z_O	Output impedance	vs Frequency	11
V_{DO}	Dropout voltage	vs Input voltage	12
		vs Free-air temperature	13
	Line transient response		14, 16
	Load transient response		15, 17
	Output voltage	vs Time	18
	Equivalent series resistance (ESR)	vs Output current	20 – 23

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

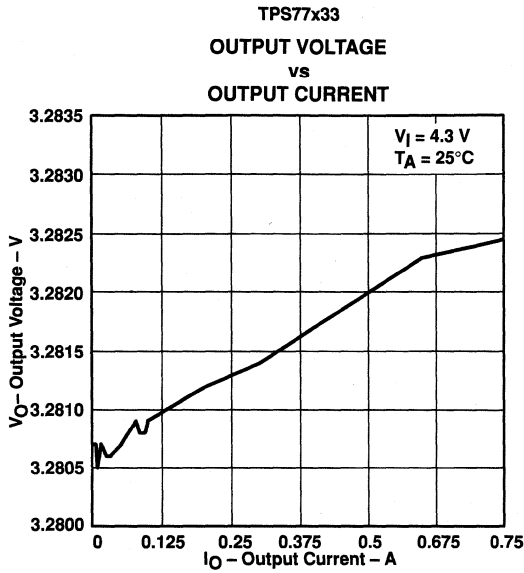


Figure 2

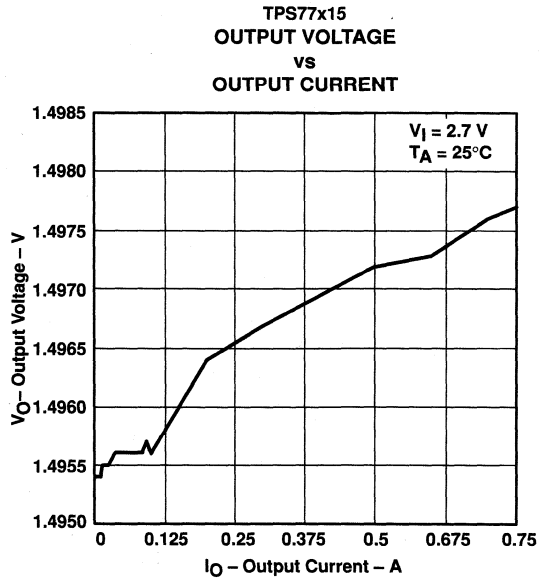


Figure 3

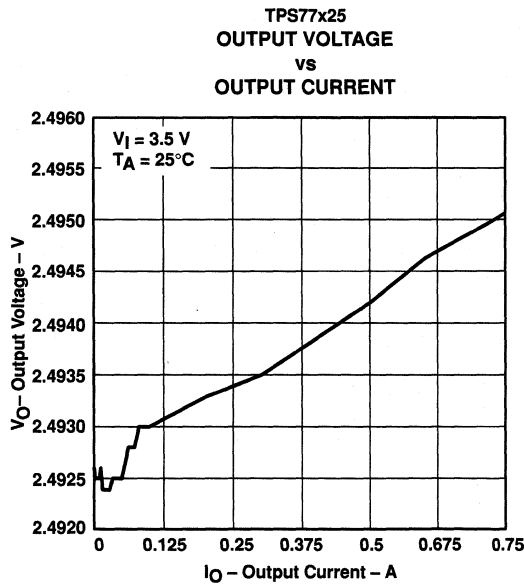


Figure 4

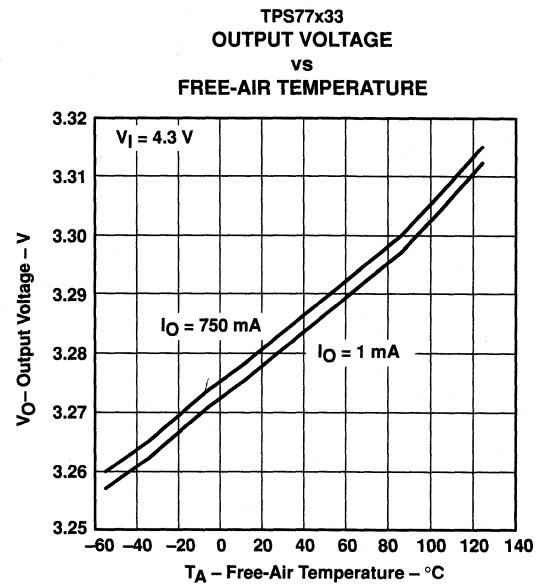


Figure 5

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS

TPS77x15
OUTPUT VOLTAGE
 vs
FREE-AIR TEMPERATURE

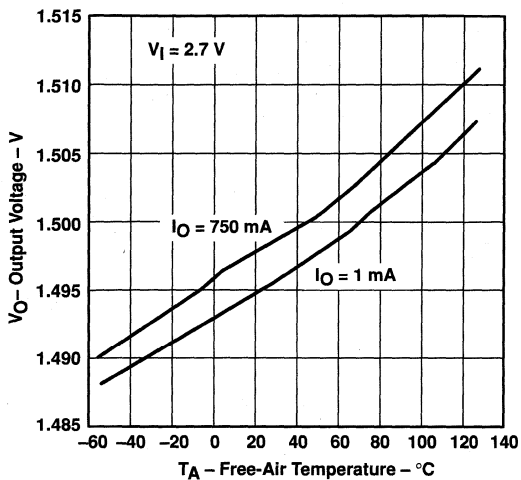


Figure 6

TPS77x25
OUTPUT VOLTAGE
 vs
FREE-AIR TEMPERATURE

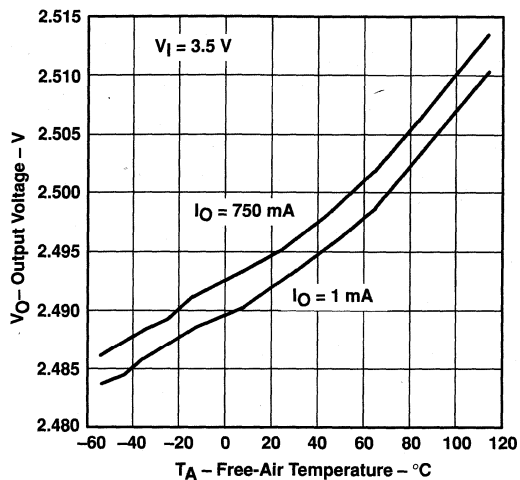


Figure 7

TPS77xxx
GROUND CURRENT
 vs
FREE-AIR TEMPERATURE

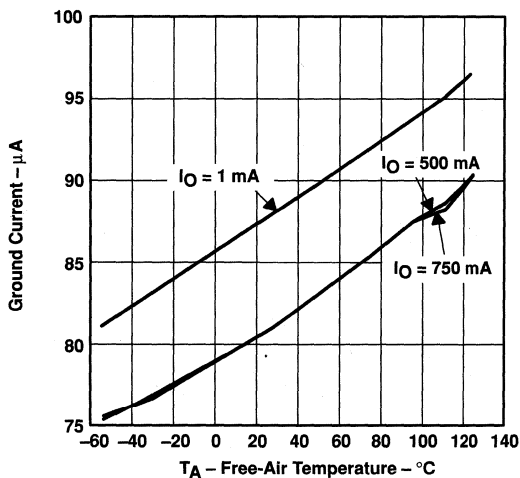


Figure 8

TPS77x33
POWER SUPPLY RIPPLE REJECTION
 vs
FREQUENCY

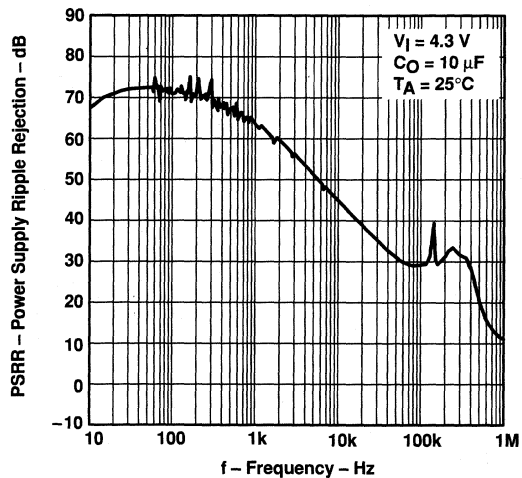


Figure 9

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
 TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS
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TYPICAL CHARACTERISTICS

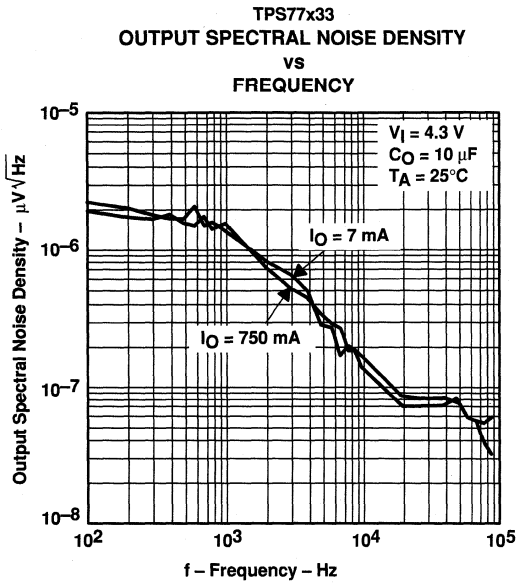


Figure 10

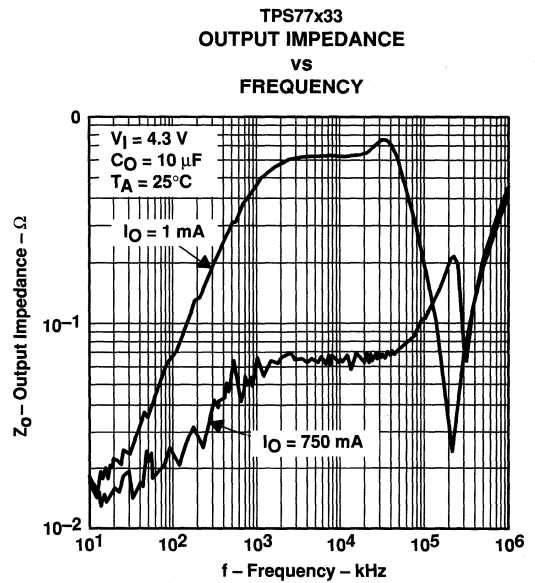


Figure 11

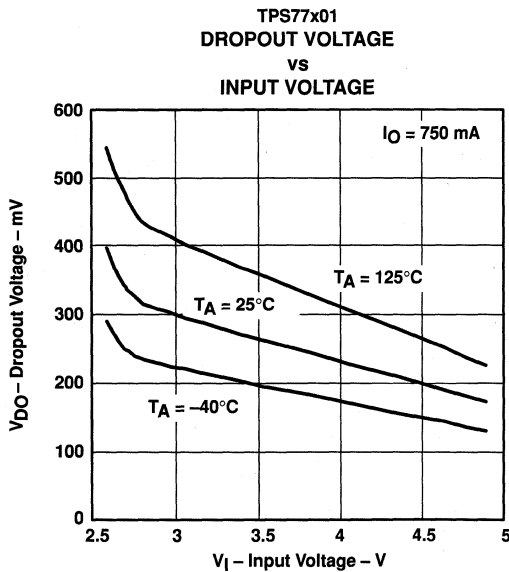


Figure 12

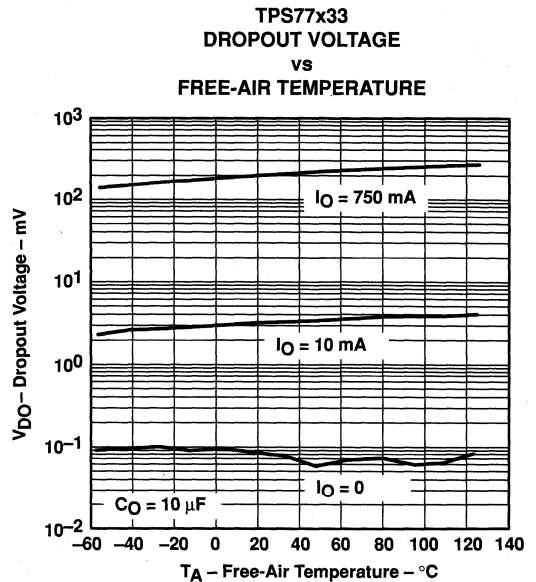


Figure 13

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

TYPICAL CHARACTERISTICS

TPS77x15
LINE TRANSIENT RESPONSE

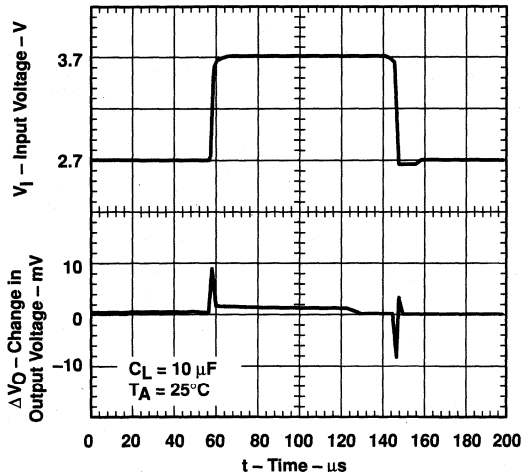


Figure 14

TPS77x15
LOAD TRANSIENT RESPONSE

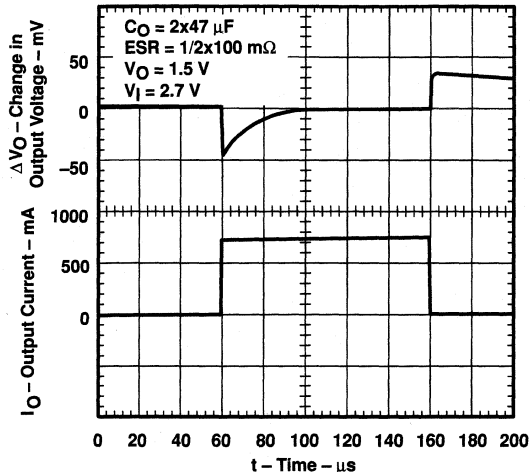


Figure 15

TPS77x33
LINE TRANSIENT RESPONSE

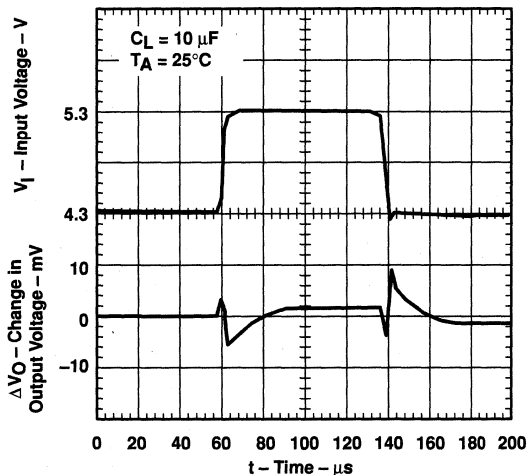


Figure 16

TPS77x33
LOAD TRANSIENT RESPONSE

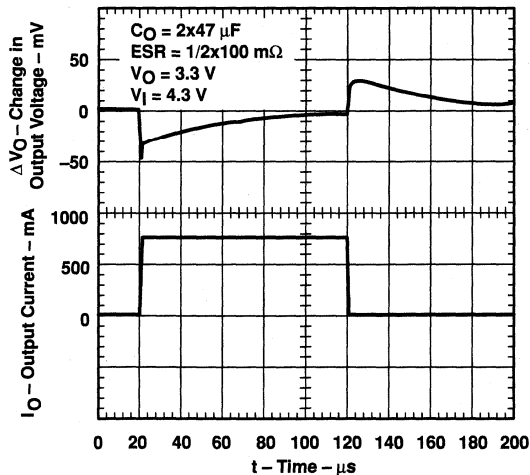


Figure 17

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
 TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
 FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

TYPICAL CHARACTERISTICS

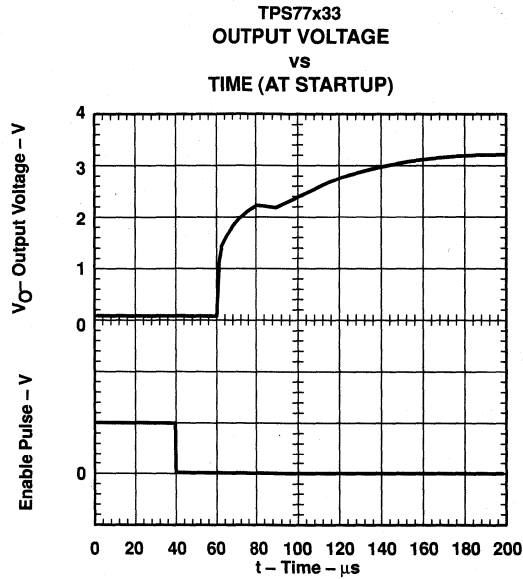


Figure 18

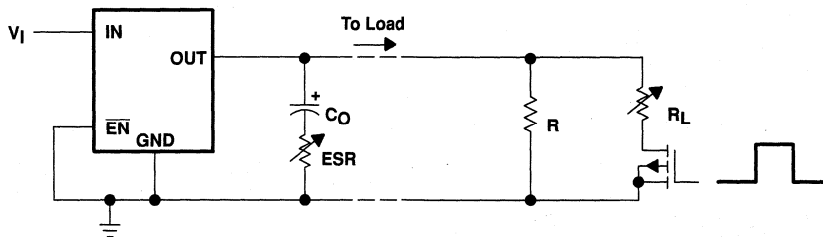


Figure 19. Test Circuit for Typical Regions of Stability (Figures 20 through 23) (Fixed Output Options)

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

TYPICAL CHARACTERISTICS

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

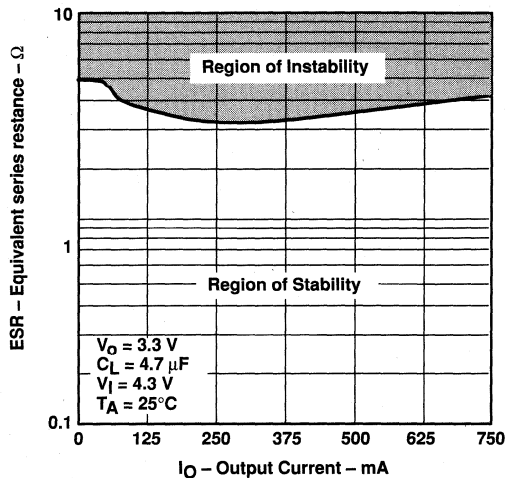


Figure 20

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

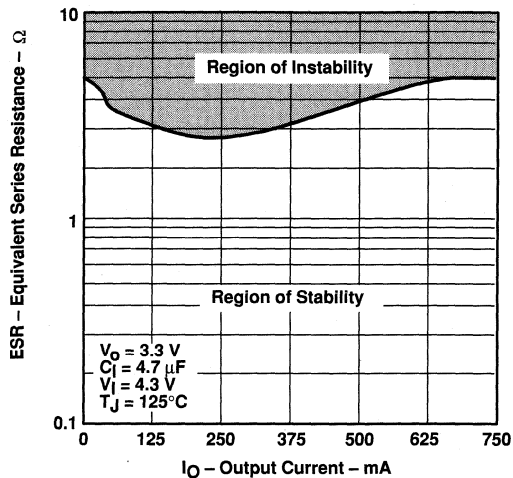


Figure 21

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

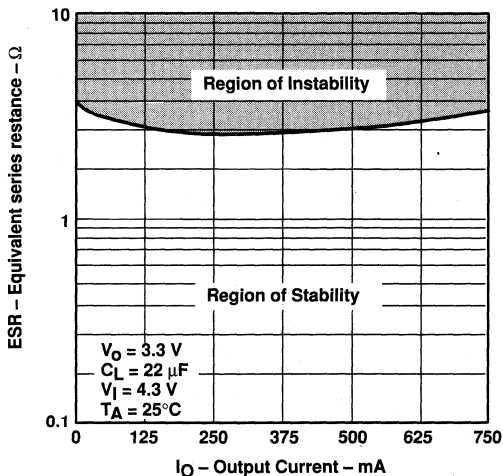


Figure 22

**TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT**

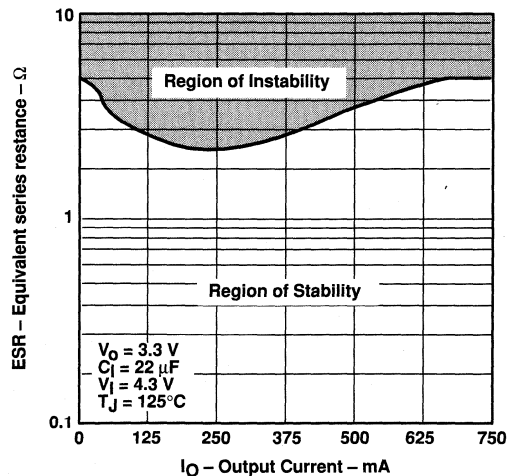


Figure 23

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

**TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS**

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

The TPS777xx and TPS778xx families include four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS77x01 (adjustable from 1.5 V to 5.5 V for TPS77701 option and 1.2 V to 5.5 V for TPS77801 option).

device operation

The TPS777xx and TPS778xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS777xx and TPS778xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS777xx and TPS778xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS777xx and TPS778xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μ A. If the shutdown feature is not used, \overline{EN} should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μ s.

minimum load requirements

The TPS777xx and TPS778xx families are stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 25. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μ F or larger) improves load transient response and noise rejection if the TPS777xx or TPS778xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS777xx and TPS778xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μ F and the ESR (equivalent series resistance) must be between 50 m Ω and 1.5 Ω . Capacitor values 10 μ F or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.



TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

external capacitor requirements (continued)

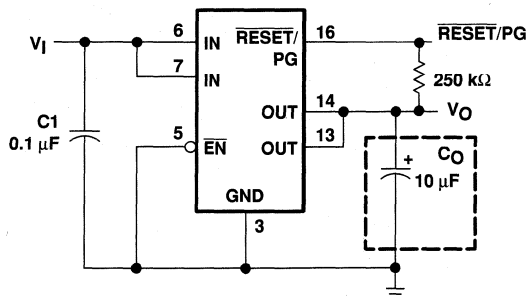


Figure 24. Typical Application Circuit (Fixed Versions)

programming the TPS77x01 adjustable LDO regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using:

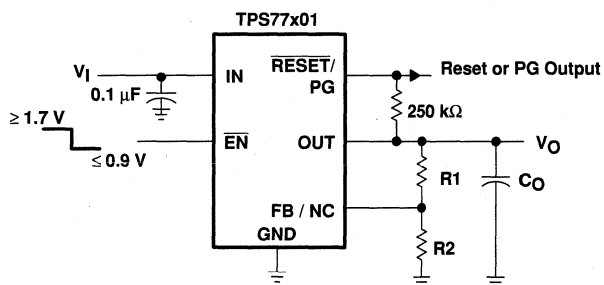
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2} \right) \tag{1}$$

Where

$$V_{ref} = 1.1834 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 110 kΩ to set the divider current at approximately 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	121	110	kΩ
3.3 V	196	110	kΩ
3.6 V	226	110	kΩ
4.75 V	332	110	kΩ

Figure 25. TPS77x01 Adjustable LDO Regulator Programming

**TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS**

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

reset indicator

The TPS777xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

power-good indicator

The TPS778xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS777xx and TPS778xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS777xx and TPS778xx also feature internal current limiting and thermal protection. During normal operation, the TPS777xx and TPS778xx limit output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

TPS77701, TPS77715, TPS77718, TPS77725, TPS77733 WITH RESET OUTPUT
TPS77801, TPS77815, TPS77818, TPS77825, TPS77833 WITH PG OUTPUT
FAST-TRANSIENT-RESPONSE 750-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS230A – SEPTEMBER 1999 – REVISED SEPTEMBER 1999

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

LM237, LM337 3-TERMINAL ADJUSTABLE REGULATORS

SLVS047C – NOVEMBER 1981 – REVISED JULY 1999

- Output Voltage Range Adjustable From -1.2 V to -37 V
- Output Current Capability of 1.5 A Max
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.3%
- Peak Output Current Constant Over Temperature Range of Regulator
- Ripple Rejection Typically 77 dB
- Direct Replacement for National Semiconductor LM237 and LM337

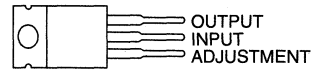
description

The LM237 and LM337 are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of -1.5 A over an output voltage range of -1.2 V to -37 V . They are exceptionally easy to use, requiring only two external resistors to set the output voltage and one output capacitor for frequency compensation. The current design has been optimized for excellent regulation and low thermal transients. In addition, the LM237 and LM337 feature internal current limiting, thermal shutdown, and safe-area compensation, making them virtually immune to failure by overloads.

The LM237 and LM337 serve a wide variety of applications, including local on-card regulation, programmable output-voltage regulation, and precision current regulation.

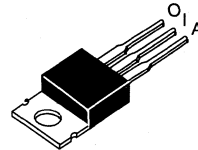
The LM237 is characterized for operation over the virtual junction temperature range of -25°C to 150°C . The LM337 is characterized for operation over the virtual junction temperature range of 0°C to 125°C .

**KC PACKAGE
(TOP VIEW)**

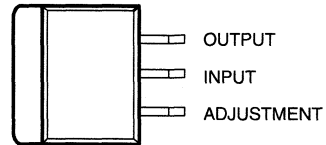


The INPUT terminal is in electrical contact with the mounting base.

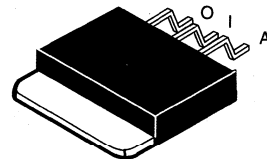
TO-220AB



**KTE PACKAGE
(TOP VIEW)**



The INPUT terminal is in electrical contact with the mounting base.



AVAILABLE OPTIONS

T _J	PACKAGED DEVICES		CHIP FORM (Y)
	HEAT-SINK MOUNTED (KC)	PLASTIC FLANGE MOUNTED (KTE)	
-25°C to 150°C	LM237KC	LM237KTE	—
0°C to 125°C	LM337KC	LM337KTE	LM337Y

The KTE package is only available taped and reeled. Add the R suffix to the device type (e.g., LM237KTER). Chip forms are tested at 25°C .

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

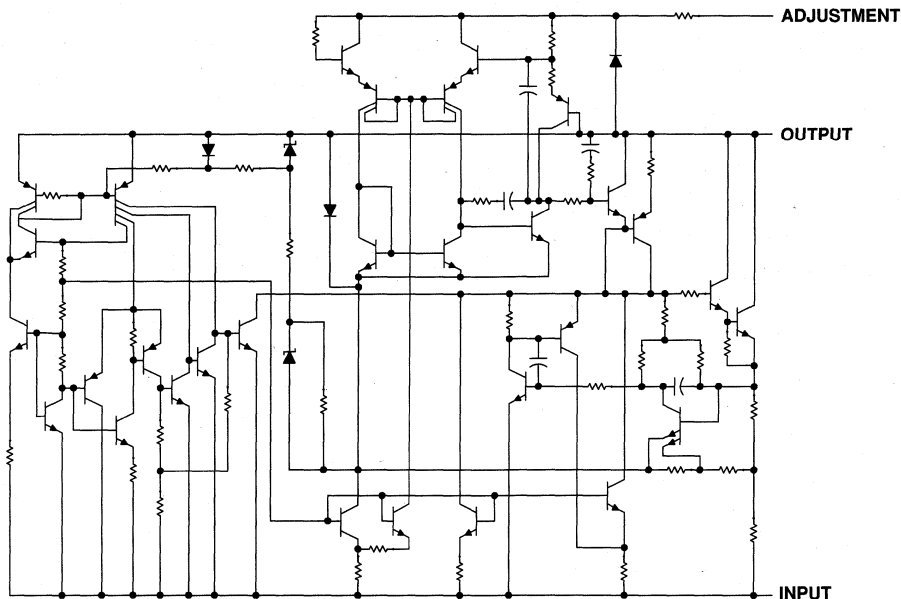
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LM237, LM337 3-TERMINAL ADJUSTABLE REGULATORS

SLVS047C – NOVEMBER 1981 – REVISED JULY 1999

schematic diagram



absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$	-40 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2): KC package	22°C/W
..... KTE package	23°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Output current, I_O	$ V_I - V_O \leq 40$ V, $P \leq 15$ W	10	1500	mA
	$ V_I - V_O \leq 10$ V, $P \leq 15$ W	6	1500	
Operating virtual junction temperature, T_J	LM237	-25	150	°C
	LM337	0	125	



LM237, LM337

3-TERMINAL ADJUSTABLE REGULATORS

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electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		LM237			LM337			UNIT		
			MIN	TYP	MAX	MIN	TYP	MAX			
Input regulation‡	$V_I - V_O = -3 \text{ V to } -40 \text{ V}$	$T_J = 25^\circ\text{C}$		0.01	0.02		0.01	0.04	% / V		
		$T_J = \text{MIN to MAX}$		0.02	0.05		0.02	0.07			
Ripple rejection	$V_O = -10 \text{ V},$	$f = 120 \text{ Hz}$		60			60	dB			
	$V_O = -10 \text{ V},$	$f = 120 \text{ Hz},$	$C_{\text{ADJ}} = 10 \mu\text{F}$	66	77		66		77		
Output regulation	$I_O = 10 \text{ mA to } 1.5 \text{ A},$	$T_J = 25^\circ\text{C}$	$ V_O \leq 5 \text{ V}$		25			50	mV		
			$ V_O \geq 5 \text{ V}$		0.3%	0.5%		0.3%	1%		
	$I_O = 10 \text{ mA to } 1.5 \text{ A}$	$ V_O \leq 5 \text{ V}$			50			70	mV		
		$ V_O \geq 5 \text{ V}$			1%			1.5%			
Output-voltage change with temperature	$T_J = \text{MIN to MAX}$			0.6%			0.6%				
Output-voltage long-term drift	After 1000 h at $T_J = \text{MAX}$ and $V_I - V_O = -40 \text{ V}$			0.3%	1%		0.3%	1%			
Output noise voltage	$f = 10 \text{ Hz to } 10 \text{ kHz},$	$T_J = 25^\circ\text{C}$		0.003%			0.003%				
Minimum output current to maintain regulation	$ V_I - V_O \leq 40 \text{ V}$			2.5	5		2.5	10	mA		
	$ V_I - V_O \leq 10 \text{ V}$			1.2	3		1.5	6			
Peak output current	$ V_I - V_O \leq 15 \text{ V}$			1.5	2.2		1.5	2.2	A		
	$ V_I - V_O \leq 40 \text{ V},$		$T_J = 25^\circ\text{C}$	0.24	0.4		0.15	0.4			
Adjustment-terminal current				65	100		65	100	μA		
Change in adjustment-terminal current	$V_I - V_O = -2.5 \text{ V to } -40 \text{ V},$		$T_J = 25^\circ\text{C},$		2	5		2	μA		
Reference voltage (output to ADJ)	$V_I - V_O = -3 \text{ V to } -40 \text{ V},$	$I_O = 10 \text{ mA to } 1.5 \text{ A},$	$P \leq \text{rated dissipation}$	$T_J = 25^\circ\text{C}$	-1.225	-1.25	-1.275	-1.213	-1.25	-1.287	V
				$T_J = \text{MIN to MAX}$	-1.2	-1.25	-1.3	-1.2	-1.25	-1.3	
Thermal regulation	Initial $T_J = 25^\circ\text{C},$		10-ms pulse		0.002	0.02	0.003	0.04	% / W		

† Unless otherwise noted, these specifications apply for the following test conditions $|V_I - V_O| = 5 \text{ V}$ and $I_O = 0.5 \text{ A}$. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $1\text{-}\mu\text{F}$ capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.



LM237, LM337

3-TERMINAL ADJUSTABLE REGULATORS

SLVS047C – NOVEMBER 1981 – REVISED JULY 1999

electrical characteristics, $T_J = 25^\circ\text{C}$

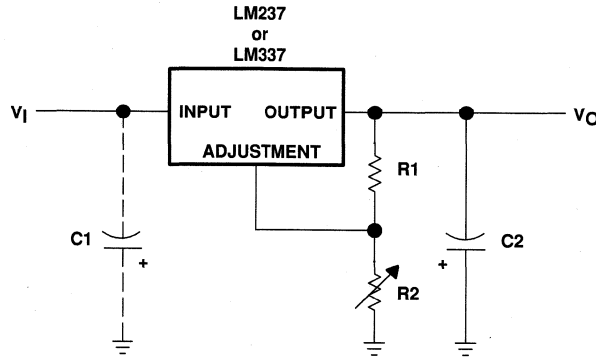
PARAMETER	TEST CONDITION†	LM237, LM337			UNIT
		MIN	TYP	MAX	
Input regulation‡	$V_I - V_O = -3\text{ V to } -40\text{ V}$		0.01	0.04	%/V
Ripple rejection	$V_O = -10\text{ V}, f = 120\text{ Hz}$		60		dB
	$V_O = -10\text{ V}, C_{\text{ADJ}} = 10\ \mu\text{F}, f = 120\text{ Hz}$		66	77	
Output regulation	$I_O = 10\text{ mA to } 1.5\text{ A}$	$ V_O \leq 5\text{ V}$		50	mV
		$ V_O \geq 5\text{ V}$		0.3% 1%	
Output noise voltage	$f = 10\text{ Hz to } 10\text{ kHz}$		0.003%		
Minimum output current to maintain regulation	$ V_I - V_O \leq 40\text{ V}$		2.5	10	mA
	$ V_I - V_O \leq 10\text{ V}$		1.5	6	
Peak output current	$ V_I - V_O \leq 15\text{ V}$		1.5	2.2	A
	$ V_I - V_O \leq 40\text{ V}$		0.15	0.4	
Adjustment-terminal current			65	100	μA
Change in adjustment-terminal current	$V_I - V_O = -2.5\text{ V to } -40\text{ V}, I_O = 10\text{ mA to MAX}$		2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = -3\text{ V to } -40\text{ V}, I_O = 10\text{ mA to } 1.5\text{ A}, P \leq \text{rated dissipation}$	-1.213	-1.25	-1.287	V

† Unless otherwise noted, these specifications apply for the following test conditions $|V_I - V_O| = 5\text{ V}$ and $I_O = 0.5\text{ A}$. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $1\text{-}\mu\text{F}$ capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.



APPLICATION INFORMATION



R1 is typically 120 Ω .

$$R2 = R1 \left(\frac{-V_O}{-1.25} - 1 \right) \text{ where } V_O \text{ is the output in volts.}$$

C1 is a 1- μ F solid tantalum capacitor required only if the regulator is more than 10 cm (4 in) from the power-supply filter capacitor. C2 is a 1- μ F solid tantalum or 10- μ F aluminum electrolytic capacitor required for stability.

Figure 1. Adjustable Negative-Voltage Regulator

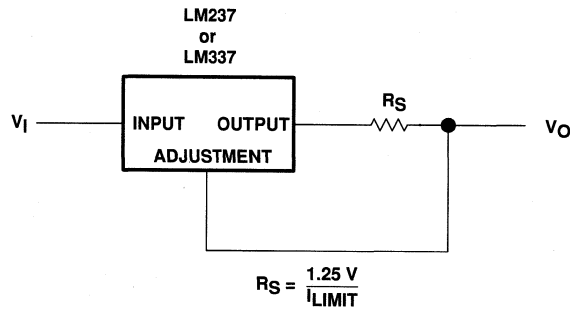


Figure 2. Current-Limiting Circuit

TL317 3-TERMINAL ADJUSTABLE REGULATORS

SLVS004C – APRIL 1979 – REVISED JULY 1999

- Output Voltage Range Adjustable From 1.2 V to 32 V When Used With an External Resistor Divider
- Output Current Capability of 100 mA
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.5%
- Ripple Rejection Typically 80 dB

description

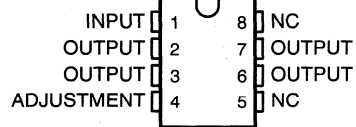
The TL317 is an adjustable three-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional, even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the TL317 regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.2 V, where most loads draw little current.

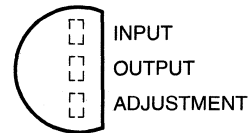
The TL317C is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

**D PACKAGE
(TOP VIEW)**



NC – No internal connection
OUTPUT terminals are all internally connected.

**LP PACKAGE
(TOP VIEW)**



AVAILABLE OPTIONS

T _J	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC (LP)	
0°C to 125°C	TL317CD	TL317CLP	TL317Y

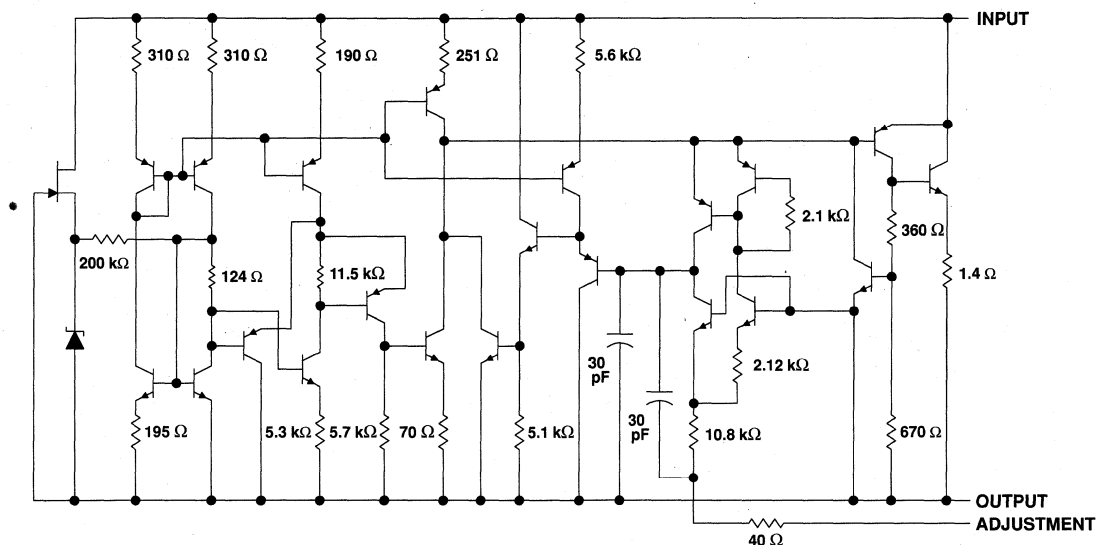
The D and LP packages are available taped and reeled. Add the suffix R to device type (e.g., TL317CDR). Chip forms are tested at 25°C.

TL317

3-TERMINAL ADJUSTABLE REGULATORS

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schematic



NOTE A. All component values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$	35 V
Operating free-air, T_A , case, or virtual-junction temperature range, T_J : TL317C	0°C to 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package	97°C/W
LP package	156°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		35	V
Output current, I_O	2.5	100	mA
Operating virtual-junction temperature, T_J	TL317C	0	125 °C



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TL317

3-TERMINAL ADJUSTABLE REGULATORS

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electrical characteristics over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317C			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 3)	$V_I - V_O = 5 \text{ V to } 35 \text{ V}$	$T_J = 25^\circ\text{C}$	0.01	0.02		%V
		$I_O = 2.5 \text{ mA to } 100 \text{ mA}$	0.02	0.05		
Ripple regulation	$V_O = 10 \text{ V},$ $f = 120 \text{ Hz}$		65			dB
	$V_O = 10 \text{ V},$ $10\text{-}\mu\text{F}$ capacitor between ADJUSTMENT and ground		66	80		
Output voltage regulation	$V_I = 5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA},$ $T_J = 25^\circ\text{C}$	$V_O \leq 5 \text{ V}$	25			mV
		$V_O \geq 5 \text{ V}$	5			mV/V
	$V_I = 5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA}$	$V_O \leq 5 \text{ V}$	50			mV
		$V_O \geq 5 \text{ V}$	10			mV/V
Output voltage change with temperature	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$		10			mV/V
Output voltage long-term drift	After 1000 hours at $T_J = 125^\circ\text{C}$ and $V_I - V_O = 35 \text{ V}$		3	10		mV/V
Output noise voltage	$f = 10 \text{ Hz to } 10 \text{ kHz},$ $T_J = 25^\circ\text{C}$		30			$\mu\text{V/V}$
Minimum output current to maintain regulation	$V_I - V_O = 35 \text{ V}$		1.5	2.5		mA
Peak output current	$V_I - V_O \leq 35 \text{ V}$		100	200		mA
ADJUSTMENT current			50	100		μA
Change in ADJUSTMENT current	$V_I - V_O = 2.5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA}$		0.2	5		μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O = 5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA},$ $P \leq \text{rated dissipation}$		1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O = 5 \text{ V}$ and $I_O = 40 \text{ mA}$. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $1\text{-}\mu\text{F}$ capacitor across the output.

NOTE 3: Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

electrical characteristics over recommended operating conditions, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL317Y			UNIT
			MIN	TYP	MAX	
Input voltage regulation (see Note 3)	$V_I - V_O = 5 \text{ V to } 35 \text{ V}$		0.01			%V
Ripple regulation	$V_O = 10 \text{ V},$ $f = 120 \text{ Hz}$		65			dB
	$V_O = 10 \text{ V},$ $10\text{-}\mu\text{F}$ capacitor between ADJUSTMENT and ground		80			
Output voltage regulation	$I_O = 2.5 \text{ mA to } 100 \text{ mA}$	$V_O \leq 5 \text{ V}$	25			mV
		$V_O \geq 5 \text{ V}$	5			mV/V
Output noise voltage	$f = 10 \text{ Hz to } 10 \text{ kHz}$		30			$\mu\text{V/V}$
Minimum output current to maintain regulation	$V_I - V_O = 35 \text{ V}$		1.5			mA
Peak output current	$V_I - V_O \leq 35 \text{ V}$		200			mA
ADJUSTMENT current			50			μA
Change in ADJUSTMENT current	$V_I - V_O = 2.5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA}$		0.2			μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O = 5 \text{ V to } 35 \text{ V},$ $I_O = 2.5 \text{ mA to } 100 \text{ mA},$ $P \leq \text{rated dissipation}$		1.25			V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O = 5 \text{ V}$ and $I_O = 40 \text{ mA}$. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $1\text{-}\mu\text{F}$ capacitor across the output.

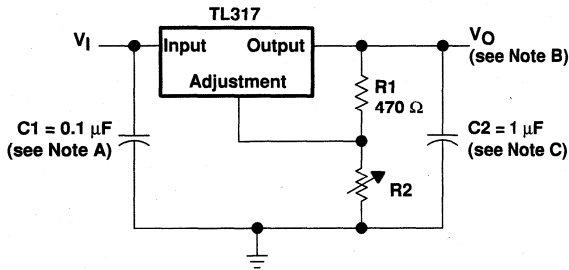
NOTE 3: Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.



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APPLICATION INFORMATION



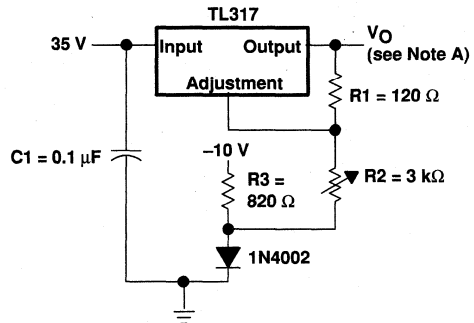
- NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors.
B. Output voltage is calculated from the equation:

$$V_O = V_{ref} \left(1 + \frac{R_2}{R_1} \right)$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈ 1.25 V).

- C. Use of an output capacitor improves transient response but is optional.

Figure 1. Adjustable Voltage Regulator

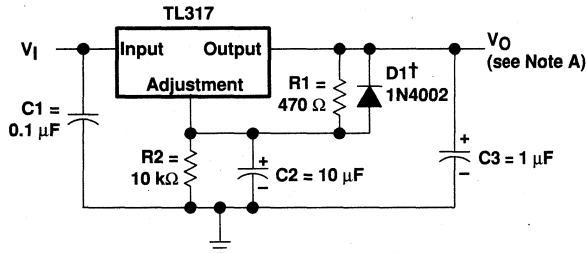


NOTE A. Output voltage is calculated from the equation:

$$V_O = V_{ref} \left(1 + \frac{R_2 + R_3}{R_1} \right) - 10 \text{ V}$$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (≈ 1.25 V).

Figure 2. 0-V to 30-V Regulator Circuit



† D1 discharges C2 if output is shorted to ground.

NOTE A. Use of an output capacitor improves transient response but is optional.

Figure 3. Regulator Circuit
With Improved Ripple Rejection

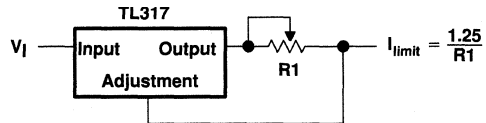


Figure 4. Precision Current-Limiter Circuit

APPLICATION INFORMATION

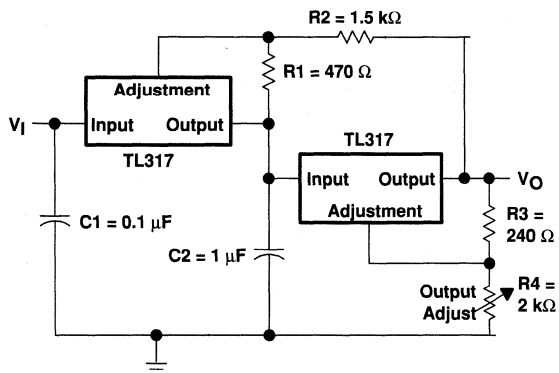


Figure 5. Tracking Preregulator Circuit

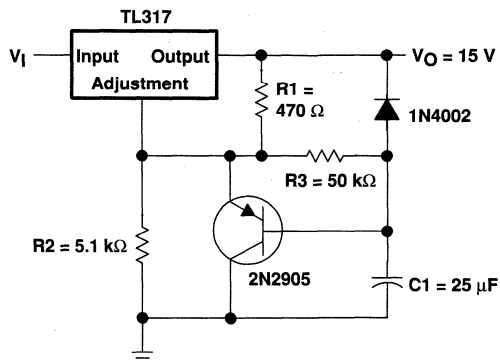


Figure 6. Slow Turnon 15-V Regulator Circuit

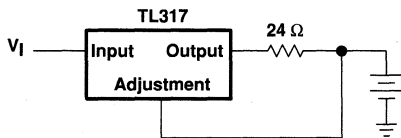


Figure 7. 50-mA Constant-Current Battery Charger Circuit

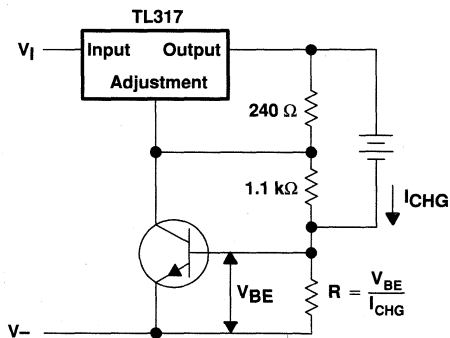
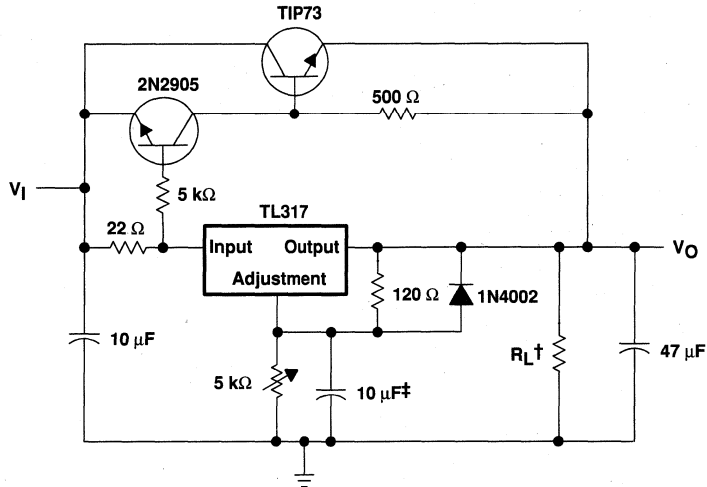


Figure 8. Current-Limited 6-V Charger

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APPLICATION INFORMATION



† Minimum load current is 30 mA.

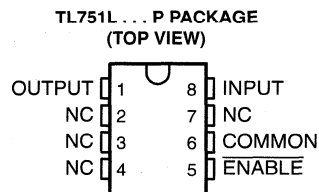
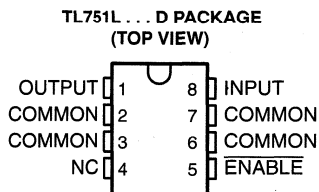
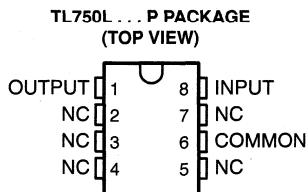
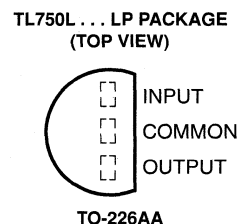
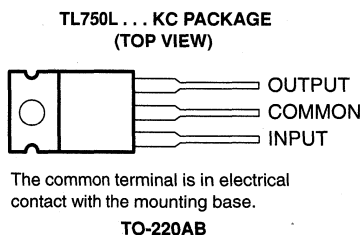
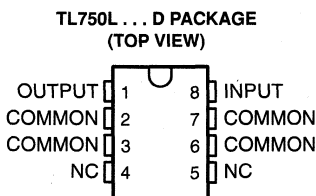
‡ Optional capacitor improves ripple rejection

Figure 9. High-Current Adjustable Regulator

TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

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- Very Low Dropout Voltage, Less Than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection Down to -50 V
- Internal Thermal-Overload Protection
- Overvoltage Protection
- Internal Overcurrent-Limiting Circuitry
- Less Than 500- μ A Disable (TL751L Series)



NC – No internal connection

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

description

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

The TL750L and TL751L series of fixed-output voltage regulators offers 5-V, 8-V, 10-V, and 12-V options. The TL751L series has the addition of an enable (ENABLE) input. When ENABLE is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

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description (continued)

The TL750LxxC and the TL751LxxC series are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The TL750L05Q and TL751L05Q are characterized for operation over the virtual junction temperature range of -40°C to 125°C.

AVAILABLE OPTIONS

T _J	V _O TYP AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE (D)	HEAT-SINK MOUNTED (KC)	PLASTIC CYLINDRICAL (LP)	PLASTIC DIP (P)	CHIP FORM (Y)
0°C to 125°C	5 V	TL750L05CD TL751L05CD	TL750L05CKC	TL750L05CLP	TL750L05CP TL751L05CP	TL750L05Y
	8 V	TL750L08CD TL751L08CD	TL750L08CKC	TL750L08CLP	TL750L08CP TL751L08CP	TL750L08Y
	10 V	TL750L10CD TL751L10CD	TL750L10CKC	TL750L10CLP	TL750L10CP TL751L10CP	TL750L10Y
	12 V	TL750L12CD TL751L12CD	TL750L12CKC	TL750L12CLP	TL750L12CP TL751L12CP	TL750L12Y
-40°C to 125°C	5 V	TL750L05QD TL751L05QD	-	-	-	-

The D, KTE, and LP packages are available taped and reeled. The KTP is only available taped and reeled. Add R suffix to device type (e.g., TL750L05CDR). Chip forms are tested at 25°C.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

	TL750Lxx TL751Lxx	UNIT
Continuous input voltage	26	V
Transient input voltage, T _A = 25°C (see Note 1)	60	V
Continuous reverse input voltage	-15	V
Transient reverse input voltage: t ≤ 100 ms	-50	V
Package thermal impedance, θ _{JA} (see Notes 2 and 3)	D package	97
	KC package	22
	LP package	156
	P package	127
Virtual junction temperature range, T _J	-40 to 150	°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds	260	°C
Storage temperature range, T _{stg}	-65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The transient input voltage rating applies to the waveform shown in Figure 1.
 2. Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can impact reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

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recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNITS	
Input voltage, V_I	TL75xL05	6	26	V	
	TL75xL08	9	26		
	TL75xL10	11	26		
	TL75xL12	13	26		
High-level ENABLE input voltage, V_{IH}	TL751Lxx	2	15	V	
Low-level ENABLE input voltage, V_{IL} †	$T_A = 25^\circ\text{C}$	TL751Lxx	-0.3	0.8	V
	$T_A = \text{full range}^\ddagger$	TL751Lxx	-0.15	0.8	
Output current range, I_O	TL75xLxx	0	150	mA	
Operating virtual junction temperature, T_J	TL75xLxxC	0	125	$^\circ\text{C}$	
	TL75xL05Q	-40	125		

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for ENABLE voltage levels and temperature only.

‡ Full range is 0°C to 125°C for the TL75xLxxC devices, and -40°C to 125°C for the TL75L05Q devices.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS§	TL750L05 TL751L05			UNIT
		MIN	TYP	MAX	
Output voltage		4.80	5	5.2	V
	$T_J = T_{J(\text{min})}$ to 125°C ¶	4.75		5.25	
Input regulation voltage	$V_I = 9\text{ V}$ to 16 V		5	10	mV
	$V_I = 6\text{ V}$ to 26 V		6	30	
Ripple rejection	$V_I = 8\text{ V}$ to 18 V , $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA}$ to 150 mA		20	50	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz}$ to 100 kHz		500		μV
Input bias current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 6\text{ V}$ to 26 V , $I_O = 10\text{ mA}$, $T_J = T_{J(\text{min})}$ to 125°C ¶		1	2	
	ENABLE > 2 V			0.5	

§ Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ capacitor, with equivalent series resistance of less than $0.4\ \Omega$, across the output.

¶ $T_{J(\text{min})}$ is 0°C for the TL75xLxxC devices, and -40°C for the TL75xLxxQ devices.

NOTE 4: For TL750L05Q/TL751L05Q, all characteristics are measured with a $0.1\text{-}\mu\text{F}$ tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL750L, TL751L SERIES LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL750L08 TL751L08			UNIT
		MIN	TYP	MAX	
Output voltage		7.68	8	8.32	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	7.6		8.4	
Input regulation voltage	$V_I = 10\text{ V to } 17\text{ V}$		10	20	mV
	$V_I = 9\text{ V to } 26\text{ V}$		25	50	
Ripple rejection	$V_I = 11\text{ V to } 21\text{ V}$, $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		40	80	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		μV
Input bias current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 9\text{ V to } 26\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	ENABLE > 2 V			0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF capacitor, with equivalent series resistance of less than 0.4 Ω , across the output.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL750L10 TL751L10			UNIT
		MIN	TYP	MAX	
Output voltage		9.6	10	10.4	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	9.5		10.5	
Input regulation voltage	$V_I = 12\text{ V to } 19\text{ V}$		10	25	mV
	$V_I = 11\text{ V to } 26\text{ V}$		30	60	
Ripple rejection	$V_I = 12\text{ V to } 22\text{ V}$, $f = 120\text{ Hz}$	60	65		dB
Output regulation voltage	$I_O = 5\text{ mA to } 150\text{ mA}$		50	100	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		700		μV
Input bias current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 11\text{ V to } 26\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 0^\circ\text{C to } 125^\circ\text{C}$		1	2	
	ENABLE > 2 V			0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF capacitor, with equivalent series resistance of less than 0.4 Ω , across the output.



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electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	TL750L12 TL751L12			UNIT
		MIN	TYP	MAX	
Output voltage		11.52	12	12.48	V
	$T_J = 0^\circ\text{C}$ to 125°C	11.4		12.6	
Input regulation voltage	$V_I = 14\text{ V}$ to 19 V		15	30	mV
	$V_I = 13\text{ V}$ to 26 V		20	40	
Ripple rejection	$V_I = 13\text{ V}$ to 23 V , $f = 120\text{ Hz}$	50	55		dB
Output regulation voltage	$I_O = 5\text{ mA}$ to 150 mA		50	120	mV
Dropout voltage	$I_O = 10\text{ mA}$			0.2	V
	$I_O = 150\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz}$ to 100 kHz		700		μV
Input bias current	$I_O = 150\text{ mA}$		10	12	mA
	$V_I = 13\text{ V}$ to 26 V , $I_O = 10\text{ mA}$, $T_J = 0^\circ\text{C}$ to 125°C		1	2	
	ENABLE > 2 V			0.5	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ capacitor, with equivalent series resistance of less than $0.4\ \Omega$, across the output.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	TL750L05Y			UNIT
		MIN	TYP	MAX	
Output voltage			5		V
Input regulation voltage	$V_I = 9\text{ V}$ to 16 V		5		mV
	$V_I = 6\text{ V}$ to 26 V		6		
Ripple rejection	$V_I = 8\text{ V}$ to 18 V , $f = 120\text{ Hz}$		65		dB
Output regulation voltage	$I_O = 5\text{ mA}$ to 150 mA		20		mV
Output noise voltage	$f = 10\text{ Hz}$ to 100 kHz		500		μV
Input bias current	$I_O = 150\text{ mA}$		10		mA
	$V_I = 6\text{ V}$ to 26 V , $I_O = 10\text{ mA}$		1		

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ capacitor, with equivalent series resistance of less than $0.4\ \Omega$, across the output.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	TL750L08Y			UNIT
		MIN	TYP	MAX	
Output voltage			8		V
Input regulation voltage	$V_I = 10\text{ V}$ to 17 V		10		mV
	$V_I = 9\text{ V}$ to 26 V		25		
Ripple rejection	$V_I = 11\text{ V}$ to 21 V , $f = 120\text{ Hz}$		65		dB
Output regulation voltage	$I_O = 5\text{ mA}$ to 150 mA		40		mV
Output noise voltage	$f = 10\text{ Hz}$ to 100 kHz		500		μV
Input bias current	$I_O = 150\text{ mA}$		10		mA
	$V_I = 9\text{ V}$ to 26 V , $I_O = 10\text{ mA}$		1		



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† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 10- μ F capacitor, with equivalent series resistance of less than 0.4 Ω , across the output.

electrical characteristics, $V_I = 14$ V, $I_O = 10$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL750L10Y			UNIT
		MIN	TYP	MAX	
Output voltage		10			V
Input regulation voltage	$V_I = 12$ V to 19 V	10			mV
	$V_I = 11$ V to 26 V	30			
Ripple rejection	$V_I = 12$ V to 22 V, $f = 120$ Hz	65			dB
Output regulation voltage	$I_O = 5$ mA to 150 mA	50			mV
Output noise voltage	$f = 10$ Hz to 100 kHz	700			μ V
Input bias current	$I_O = 150$ mA	10			mA
	$V_I = 11$ V to 26 V, $I_O = 10$ mA	1			

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 10- μ F capacitor, with equivalent series resistance of less than 0.4 Ω , across the output.

electrical characteristics, $V_I = 14$ V, $I_O = 10$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL750L12Y			UNIT
		MIN	TYP	MAX	
Output voltage		12			V
Input regulation voltage	$V_I = 14$ V to 19 V	15			mV
	$V_I = 13$ V to 26 V	20			
Ripple rejection	$V_I = 13$ V to 23 V, $f = 120$ Hz	55			dB
Output regulation voltage	$I_O = 5$ mA to 150 mA	50			mV
Output noise voltage	$f = 10$ Hz to 100 kHz	700			μ V
Input bias current	$I_O = 150$ mA	10			mA
	$V_I = 13$ V to 26 V, $I_O = 10$ mA	1			

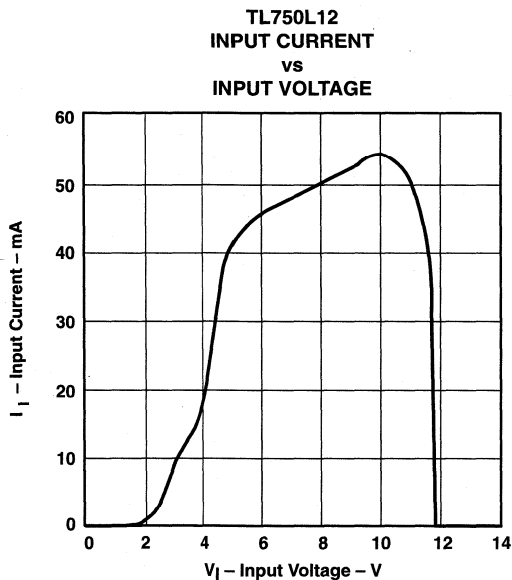
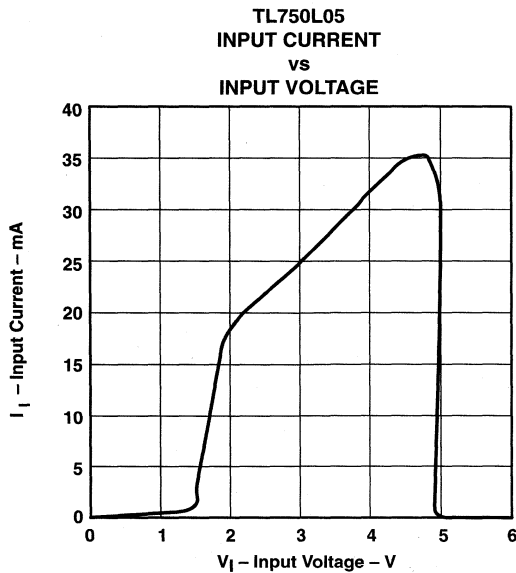
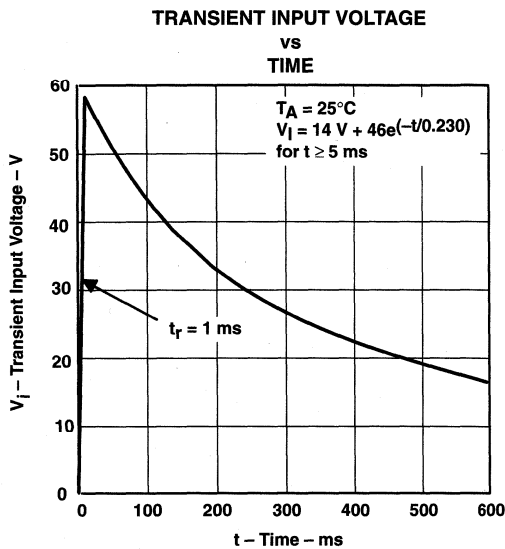
† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 10- μ F capacitor, with equivalent series resistance of less than 0.4 Ω , across the output.



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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

TL750L05
EQUIVALENT SERIES RESISTANCE
VS
LOAD CURRENT

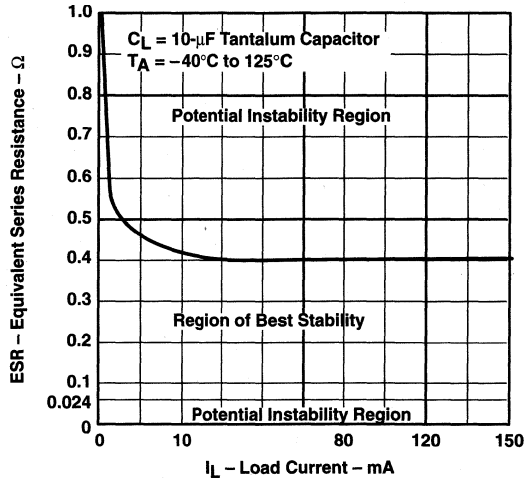


Figure 4

TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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- Very Low Dropout Voltage, Less Than 0.6 V at 750 mA
- Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751M Series
- 60-V Load-Dump Protection
- Overvoltage Protection
- Internal Thermal Overload Protection
- Internal Overcurrent Limiting Circuitry

description

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M series incorporate onboard overvoltage and current-limiting protection circuitry to protect the devices and the regulated system. Both series are fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M and TL751M series offers 5-V, 8-V, 10-V, and 12-V options. The TL751M series has the addition of an enable (ENABLE) input. The ENABLE input gives the designer complete control over power up, allowing sequential power up or emergency shutdown. When ENABLE is high, the regulator output is placed in the high-impedance state. The ENABLE input is TTL- and CMOS-compatible.

The TL750MxxC and TL751MxxC are characterized for operation over the virtual junction temperature range 0°C to 125°C.

AVAILABLE OPTIONS

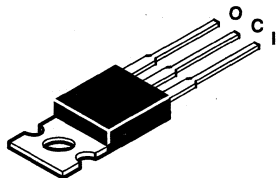
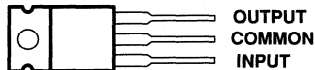
T _J	V _O TYP (V)	PACKAGED DEVICES				CHIP FORM (Y)
		HEAT-SINK MOUNTED (3-PIN) (KC)	PLASTIC FLANGE MOUNT (KTE)	PLASTIC FLANGE MOUNT (KTG)	PLASTIC FLANGE MOUNT (KTP)	
0°C to 125°C	5	TL750M05CKC	TL750M05CKTE	TL751M05CKTG	TL750M05CKTP	TL750M05Y
	8	TL750M08CKC	TL750M08CKTE	TL751M08CKTG	TL750M08CKTP	TL750M08Y
	10	TL750M10CKC	TL750M10CKTE	TL751M10CKTG	TL750M10CKTP	TL750M10Y
	12	TL750M12CKC	TL750M12CKTE	TL751M12CKTG	TL750M12CKTP	TL750M12Y

The KTE and KTG packages are available taped and reeled. The KTP is only available taped and reeled. Add the suffix R to device type (e.g., TL750M05CKTER). Chip forms are tested at 25°C.

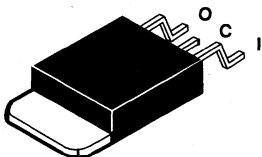
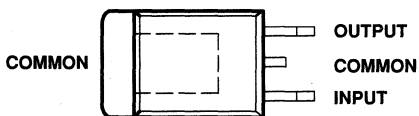
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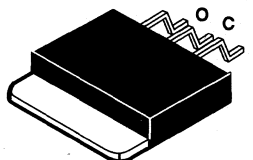
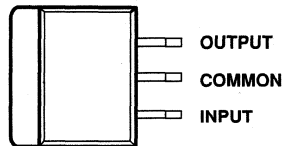
TL750M . . . 3-LEAD KC (TO-200AB) PACKAGE†
(TOP VIEW)



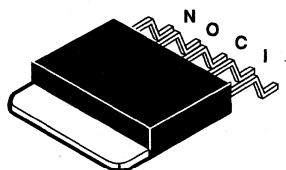
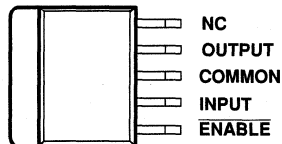
TL750M . . . KTP PACKAGE†
(TOP VIEW)



TL750M . . . 3-LEAD KTE PACKAGE†
(TOP VIEW)



TL751M . . . 5-LEAD KTG PACKAGE†
(TOP VIEW)

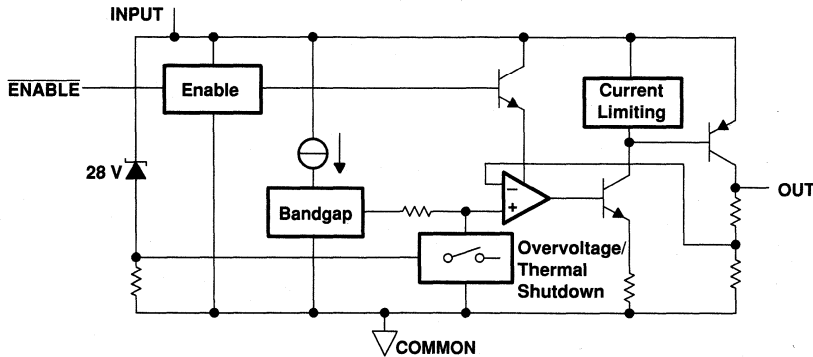


† The common terminal is in electrical contact with the mounting base.
NC – No internal connection

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TL751Mxx functional block diagram



DEVICE COMPONENT COUNT	
Transistors	46
Diodes	14
Resistors	44
Capacitors	4
JFETs	1
Tunnels (emitter R)	2

absolute maximum ratings over virtual junction temperature range (unless otherwise noted)†

Continuous input voltage	26 V
Transient input voltage (see Figure 3)	60 V
Continuous reverse input voltage	-15 V
Transient reverse input voltage: $t = 100 \text{ ms}$	-50 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2): KC package	22°C/W
KTE package	23°C/W
KTG package	23°C/W
KTP package	28°C/W
Virtual junction temperature range, T_J	0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
 - The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions over recommended virtual junction temperature range

		MIN	MAX	UNIT
Input voltage range, V_I	TL75xM05	6	26	V
	TL75xM08	9	26	
	TL75xM10	11	26	
	TL75xM12	13	26	
High-level ENABLE input voltage, V_{IH}	TL751Mxx	2	15	V
Low-level ENABLE input voltage, V_{IL}	TL751Mxx	0	0.8	
Output current range, I_O	TL75xMxxC		750	mA
Operating virtual junction temperature range, T_J	TL75xMxxC	0	125	°C



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electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $T_J = 25^\circ\text{C}$

PARAMETER	TL751MXXX			UNIT
	MIN	TYP	MAX	
Response time, $\overline{\text{ENABLE}}$ to output	50			μs

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V for TL751M05, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M05C, TL751M05C			UNIT
		MIN	TYP	MAX	
Output voltage		4.95	5	5.05	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	4.9		5.1	
Input voltage regulation	$V_I = 9\text{ V to } 16\text{ V}$, $I_O = 250\text{ mA}$		10	25	mV
	$V_I = 6\text{ V to } 26\text{ V}$, $I_O = 250\text{ mA}$		12	50	
Ripple rejection	$V_I = 8\text{ V to } 18\text{ V}$, $f = 120\text{ Hz}$	50	55		dB
Output voltage regulation	$I_O = 5\text{ mA to } 750\text{ mA}$		20	50	mV
Dropout voltage	$I_O = 500\text{ mA}$			0.5	V
	$I_O = 750\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		μV
Bias current	$I_O = 750\text{ mA}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Bias current (TL751M05C and TL751M05Q only)	$\overline{\text{ENABLE}} V_{IH} \geq 2\text{ V}$			200	μA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V for TL751M08, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M08C, TL751M08C			UNIT
		MIN	TYP	MAX	
Output voltage		7.92	8	8.08	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	7.84		8.16	
Input voltage regulation	$V_I = 10\text{ V to } 17\text{ V}$, $I_O = 250\text{ mA}$		12	40	mV
	$V_I = 9\text{ V to } 26\text{ V}$, $I_O = 250\text{ mA}$		15	68	
Ripple rejection	$V_I = 11\text{ V to } 21\text{ V}$, $f = 120\text{ Hz}$	50	55		dB
Output voltage regulation	$I_O = 5\text{ mA to } 750\text{ mA}$		24	80	mV
Dropout voltage	$I_O = 500\text{ mA}$			0.5	V
	$I_O = 750\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		μV
Bias current	$I_O = 750\text{ mA}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}} V_{IH} \geq 2\text{ V}$			200	μA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

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electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V for TL751M10, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M10C, TL751M10C			UNIT
		MIN	TYP	MAX	
Output voltage		9.9	10	10.1	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	9.8		10.2	
Input voltage regulation	$V_I = 12\text{ V to } 18\text{ V}, I_O = 250\text{ mA}$		15	43	mV
	$V_I = 11\text{ V to } 26\text{ V}, I_O = 250\text{ mA}$		20	75	
Ripple rejection	$V_I = 13\text{ V to } 23\text{ V}, f = 120\text{ Hz}$	50	55		dB
Output voltage regulation	$I_O = 5\text{ mA to } 750\text{ mA}$		30	100	mV
Dropout voltage	$I_O = 500\text{ mA}$			0.5	V
	$I_O = 750\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		1000		μV
Bias current	$I_O = 750\text{ mA}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}} V_{IH} \geq 2\text{ V}$			200	μA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V for TL751M12, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M12C, TL751M12C			UNIT
		MIN	TYP	MAX	
Output voltage		11.88	12	12.12	V
	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	11.76		12.24	
Input voltage regulation	$V_I = 14\text{ V to } 19\text{ V}, I_O = 250\text{ mA}$		15	43	mV
	$V_I = 13\text{ V to } 26\text{ V}, I_O = 250\text{ mA}$		20	78	
Ripple rejection	$V_I = 13\text{ V to } 23\text{ V}, f = 120\text{ Hz}$	50	55		dB
Output voltage regulation	$I_O = 5\text{ mA to } 750\text{ mA}$		30	120	mV
Dropout voltage	$I_O = 500\text{ mA}$			0.5	V
	$I_O = 750\text{ mA}$			0.6	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		1000		μV
Bias current	$I_O = 750\text{ mA}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}} V_{IH} \geq 2\text{ V}$			200	μA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.



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electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V , $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M05Y			UNIT
		MIN	TYP	MAX	
Output voltage		5			V
Input voltage regulation	$V_I = 9\text{ V to }16\text{ V}$, $I_O = 250\text{ mA}$	10			mV
	$V_I = 6\text{ V to }26\text{ V}$, $I_O = 250\text{ mA}$	12			
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	55			dB
Output voltage regulation	$I_O = 5\text{ mA to }750\text{ mA}$	20			mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	500			μV
Bias current	$I_O = 750\text{ mA}$	60			mA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V , $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M08Y			UNIT
		MIN	TYP	MAX	
Output voltage		8			V
Input voltage regulation	$V_I = 10\text{ V to }17\text{ V}$, $I_O = 250\text{ mA}$	12			mV
	$V_I = 9\text{ V to }26\text{ V}$, $I_O = 250\text{ mA}$	15			
Ripple rejection	$V_I = 11\text{ V to }21\text{ V}$, $f = 120\text{ Hz}$	55			dB
Output voltage regulation	$I_O = 5\text{ mA to }750\text{ mA}$	24			mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	500			μV
Bias current	$I_O = 750\text{ mA}$	60			mA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, $\overline{\text{ENABLE}}$ at 0 V , $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M10Y			UNIT
		MIN	TYP	MAX	
Output voltage		10			V
Input voltage regulation	$V_I = 12\text{ V to }18\text{ V}$, $I_O = 250\text{ mA}$	15			mV
	$V_I = 11\text{ V to }26\text{ V}$, $I_O = 250\text{ mA}$	20			
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	55			dB
Output voltage regulation	$I_O = 5\text{ mA to }750\text{ mA}$	30			mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	1000			μV
Bias current	$I_O = 750\text{ mA}$	60			mA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $10\text{-}\mu\text{F}$ tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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TL751M12Y electrical characteristics, $V_I = 14\text{ V}$, $I_O = 300\text{ mA}$, ENABLE at 0 V, $T_J = 25^\circ\text{C}$ (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	TL750M12Y			UNIT
		MIN	TYP	MAX	
Output voltage			12		V
Input voltage regulation	$V_I = 14\text{ V to }19\text{ V}$, $I_O = 250\text{ mA}$		15		mV
	$V_I = 13\text{ V to }26\text{ V}$, $I_O = 250\text{ mA}$		20		
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$		55		dB
Output voltage regulation	$I_O = 5\text{ mA to }750\text{ mA}$		30		mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		1000		μV
Bias current	$I_O = 750\text{ mA}$		60		mA

NOTE 3: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 10- μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 3.

PARAMETER MEASUREMENT INFORMATION

The TL751Mxx is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 1 and 2 can establish the capacitance value and ESR range for the best regulator performance.

Figure 1 shows the recommended range of ESR for a given load with a 10- μF capacitor on the output. This figure also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 2 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω . This figure establishes the amount that the minimum ESR limit shown in Figure 1 can be adjusted for different capacitor values. For example, where the minimum load needed is 200 mA, Figure 2 suggests an ESR range of 0.8 Ω to 2 Ω for 10 μF . Figure 2 shows that changing the capacitor from 10 μF to 400 μF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω , achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figures 1 and 2.

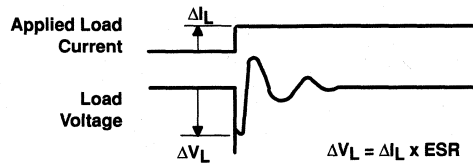
TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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PARAMETER MEASUREMENT INFORMATION

Table 1. Compensation for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 μF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 μF	0.6 Ω	T491D336M010AS	0.5 Ω



OUTPUT CAPACITOR
EQUIVALENT SERIES RESISTANCE (ESR)
vs
LOAD CURRENT RANGE

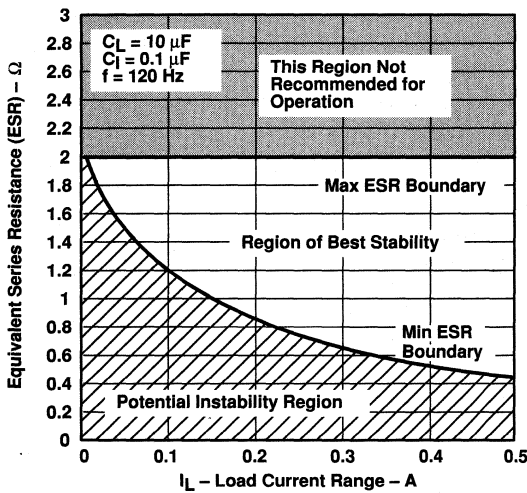


Figure 1

STABILITY
vs
EQUIVALENT SERIES RESISTANCE (ESR)

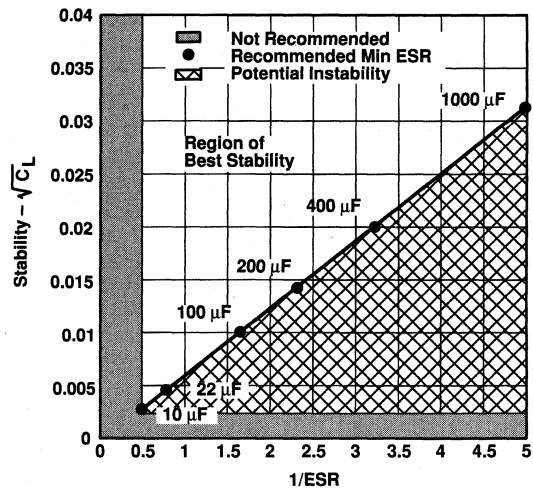


Figure 2

TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Transient input voltage vs Time		3
Output voltage vs Input voltage		4
Input current vs Input voltage	$I_O = 10 \text{ mA}$	5
	$I_O = 100 \text{ mA}$	6
Dropout voltage vs Output current		7
Quiescent current vs Output current		8
Load transient response		9
Line transient response		10

TRANSIENT INPUT VOLTAGE
vs
TIME

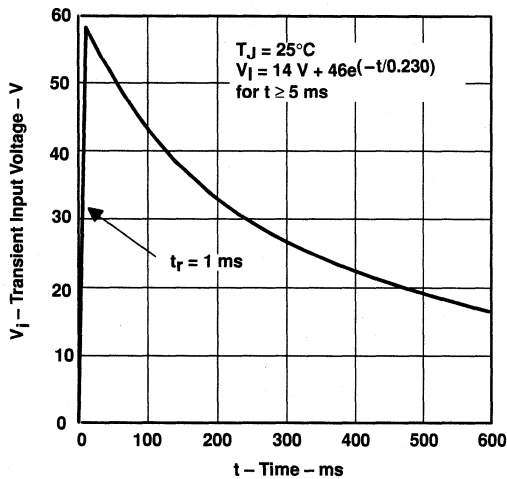


Figure 3

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

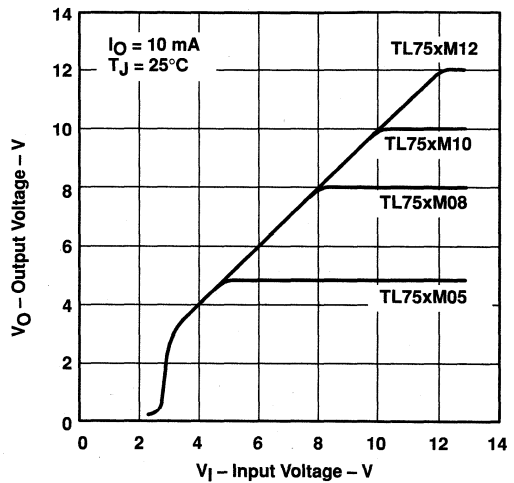
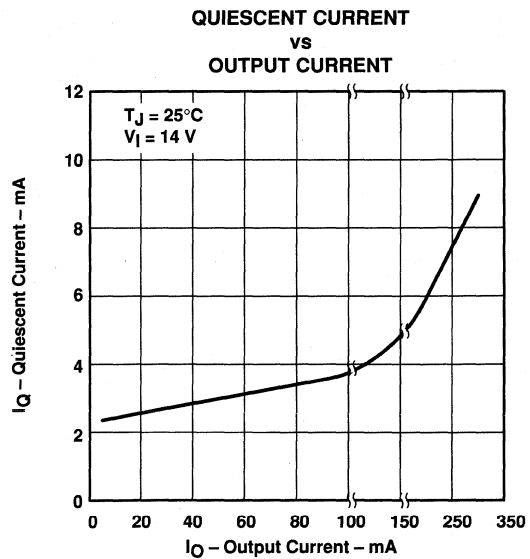
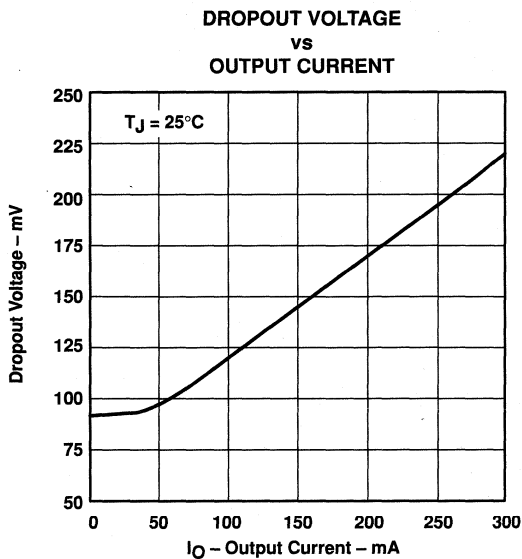
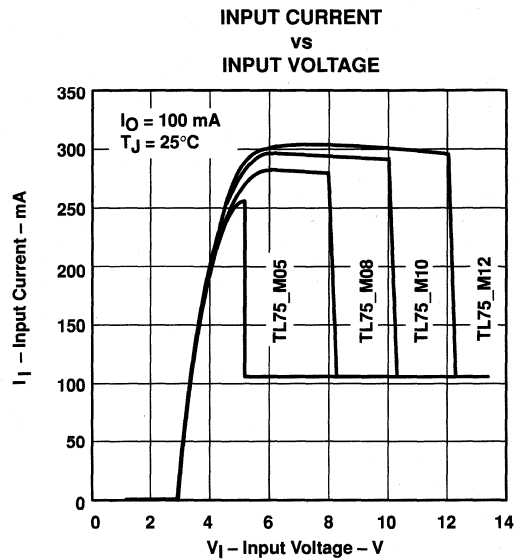
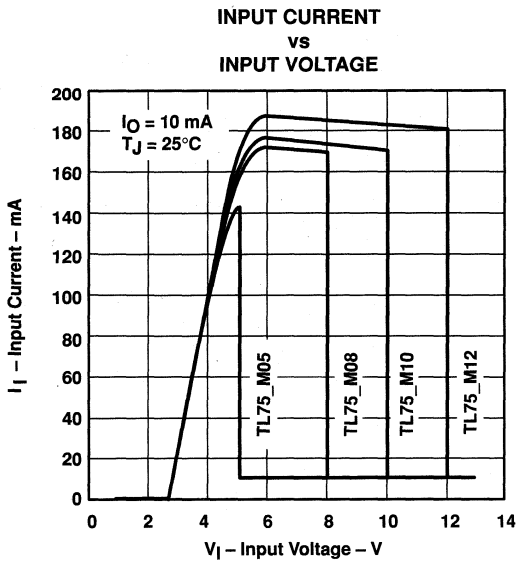


Figure 4

TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS



TL750M, TL751M SERIES LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

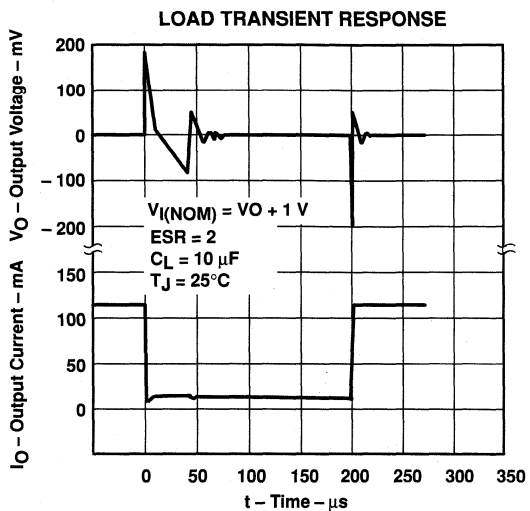


Figure 9

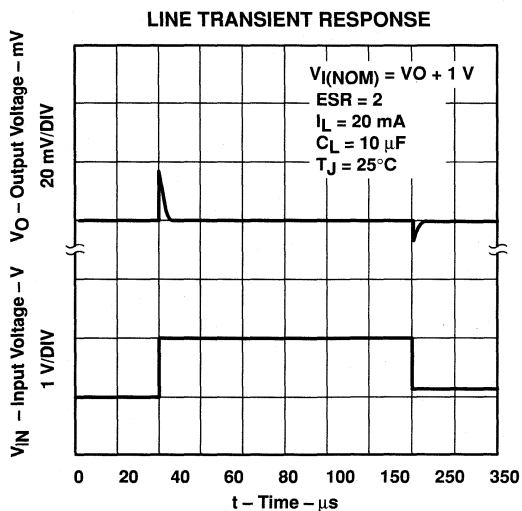


Figure 10

TL780 SERIES POSITIVE-VOLTAGE REGULATORS

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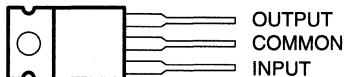
- $\pm 1\%$ Output Tolerance at 25°C
- $\pm 2\%$ Output Tolerance Over Full Operating Range
- Thermal Shutdown
- Internal Short-Circuit Current Limiting
- Pinout Identical to $\mu A7800$ Series
- Improved Version of $\mu A7800$ Series

description

Each fixed-voltage precision regulator in the TL780 series is capable of supplying 1.5 A of load current. A unique temperature-compensation technique coupled with an internally trimmed band-gap reference has resulted in improved accuracy when compared to other three-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current-limiting and thermal-shutdown features make the devices essentially immune to overload.

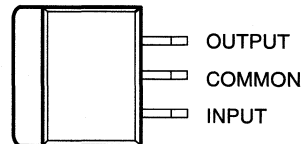
The TL780-xxC series regulators are characterized for operation over the virtual junction temperature range of 0°C to 125°C.

**KC PACKAGE
(TOP VIEW)**

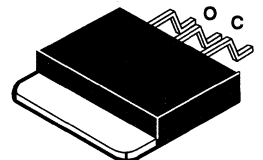
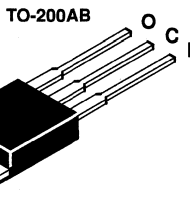


The COMMON terminal is in electrical contact with the mounting base.

**KTE PACKAGE
(TOP VIEW)**



The COMMON terminal is in electrical contact with the mounting base.



AVAILABLE OPTIONS

T _J	V _O TYP (V)	PACKAGED DEVICES		
		HEAT-SINK MOUNTED (KC)	PLASTIC FLANGE MOUNTED (KTE)	CHIP FORM (Y)
0°C to 125°C	5	TL780-05CKC	TL780-05CKTE	TL780-05Y
	12	TL780-12CKC	TL780-12CKTE	TL780-12Y
	15	TL780-15CKC	TL780-15CKTE	TL780-15Y

The KTE package is available taped and reeled. Add the suffix R to the device type (e.g., TL780-05CKTER). Chip forms are tested at 25°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

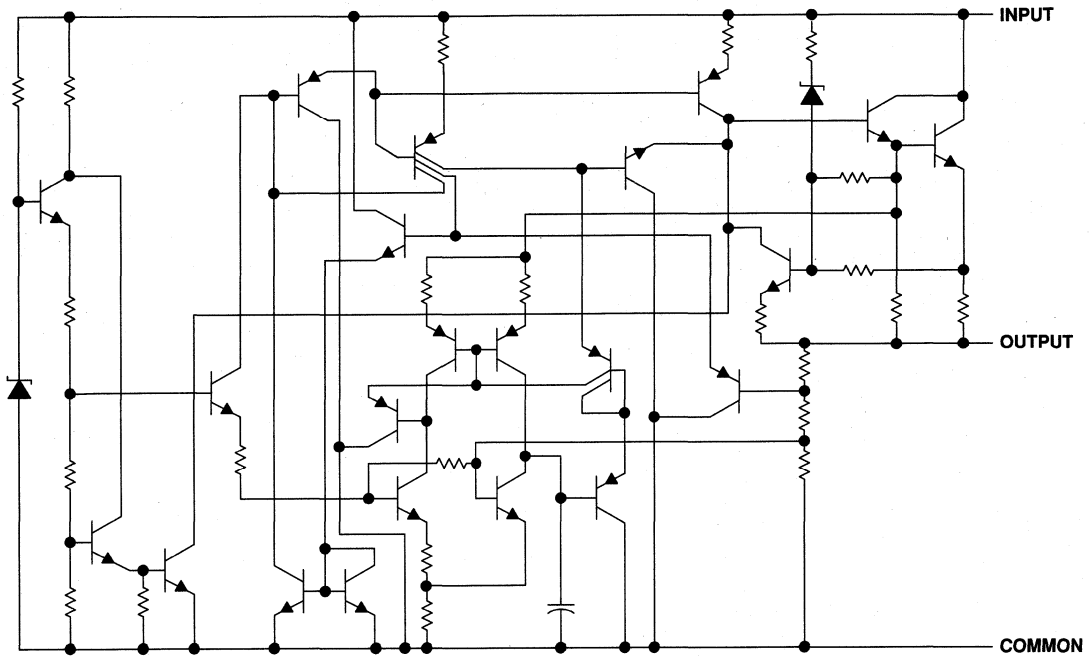
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TL780 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS055E - APRIL 1981 - REVISED JULY 1999

schematic



TL780 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS055E – APRIL 1981 – REVISED JULY 1999

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input voltage, V_I	35 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2): DBV package	23°C/W
KC package	22°C/W
Operating free-air, T_A , case, T_C , or virtual junction, T_J , temperature range	0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL780-05C	7	25	V
	TL780-12C	14.5	30	
	TL780-15C	17.5	30	
Output current, I_O		1.5		A
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, $V_I = 10$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J ‡	TL780-05C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5$ mA to 1 A, $P \leq 15$ W, $V_I = 7$ V to 20 V	25°C	4.95	5	5.05	V
		0°C to 125°C	4.9		5.1	
Input voltage regulation	$V_I = 7$ V to 25 V	25°C	0.5		5	mV
	$V_I = 8$ V to 12 V		0.5		5	
Ripple rejection	$V_I = 8$ V to 18 V, $f = 120$ Hz	0°C to 125°C	70	85		dB
Output voltage regulation	$I_O = 5$ mA to 1.5 A	25°C	4		25	mV
	$I_O = 250$ mA to 750 mA		1.5		15	
Output resistance	$f = 1$ kHz	0°C to 125°C	0.0035			Ω
Temperature coefficient of output voltage	$I_O = 5$ mA	0°C to 125°C	0.25			mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz	25°C	75			μV
Dropout voltage	$I_O = 1$ A	25°C	2			V
Input bias current		25°C	5		8	mA
Input bias-current change	$V_I = 7$ V to 25 V	0°C to 125°C	0.7		1.3	mA
	$I_O = 5$ mA to 1 A		0.003		0.5	
Short-circuit output current		25°C	750			mA
Peak output current		25°C	2.2			A

‡ Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.



TL780 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS055E – APRIL 1981 – REVISED JULY 1999

electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	TL780-12C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P \leq 15\text{ W}$, $V_I = 14.5\text{ V to }27\text{ V}$	25°C	11.88	12	12.12	V
		0°C to 125°C	11.76		12.24	
Input voltage regulation	$V_I = 14.5\text{ V to }30\text{ V}$	25°C		1.2	12	mV
	$V_I = 16\text{ V to }22\text{ V}$			1.2	12	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	65	80		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		6.5	60	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			2.5	36	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.0035			Ω
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	0.6			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	180			μV
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V
Input bias current		25°C	5.5			8 mA
Input bias-current change	$V_I = 14.5\text{ V to }30\text{ V}$	0°C to 125°C	0.4			1.3 mA
	$I_O = 5\text{ mA to }1\text{ A}$		0.03			
Short-circuit output current		25°C	350			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.22- μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	TL780-15C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P \leq 15\text{ W}$, $V_I = 17.5\text{ V to }30\text{ V}$	25°C	14.85	15	15.15	V
		0°C to 125°C	14.7		15.3	
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	25°C	1.5			15 mV
	$V_I = 20\text{ V to }26\text{ V}$		1.5			
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	60	75		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	7			75 mV
	$I_O = 250\text{ mA to }750\text{ mA}$		2.5			
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.0035			Ω
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	0.62			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	225			μV
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V
Input bias current		25°C	5.5			8 mA
Input bias-current change	$V_I = 17.5\text{ V to }30\text{ V}$	0°C to 125°C	0.4			1.3 mA
	$I_O = 5\text{ mA to }1\text{ A}$		0.02			
Short-circuit output current		25°C	230			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.22- μF capacitor across the output.



TL780 SERIES POSITIVE-VOLTAGE REGULATORS

SLVS055E – APRIL 1981 – REVISED JULY 1999

electrical characteristics, $V_I = 10\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST	TL780-05Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P \leq 15\text{ W}$		5		V
Input voltage regulation	$V_I = 7\text{ V to }25\text{ V}$		0.5		mV
	$V_I = 8\text{ V to }12\text{ V}$		0.5		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		4		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		1.5		
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		75		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Input bias current			5		mA
Short-circuit output current			750		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.33\text{-}\mu\text{F}$ capacitor across the input and a $0.22\text{-}\mu\text{F}$ capacitor across the output.

electrical characteristics, $V_I = 19\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST	TL780-12Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P \leq 15\text{ W}$		12		V
Input voltage regulation	$V_I = 14.5\text{ V to }30\text{ V}$		1.2		mV
	$V_I = 16\text{ V to }22\text{ V}$		1.2		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		6.5		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		2.5		
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		180		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Input bias current			5.5		mA
Short-circuit output current			350		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.33\text{-}\mu\text{F}$ capacitor across the input and a $0.22\text{-}\mu\text{F}$ capacitor across the output.

TL780 SERIES POSITIVE-VOLTAGE REGULATORS

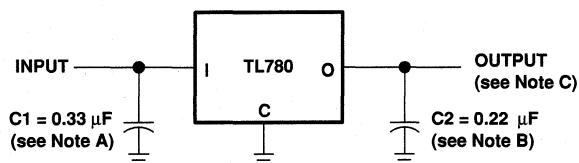
SLVS055E – APRIL 1981 – REVISED JULY 1999

electrical characteristics, $V_I = 23\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL780-15Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P \leq 15\text{ W}$		15		V
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$		1.5		mV
	$V_I = 20\text{ V to }26\text{ V}$		1.5		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		7		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		2.5		
Output resistance	$f = 1\text{ kHz}$		0.0035		Ω
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		225		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Input bias current			5.5		mA
Short-circuit output current			230		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μF capacitor across the input and a 0.22- μF capacitor across the output.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C1 is required when the regulator is far from the power supply filter.
 B. C2 is not required for stability; however, transient response is improved.
 C. Permanent damage can occur when output is pulled below ground.

Figure 1. Test Circuit

APPLICATION INFORMATION

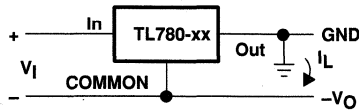


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

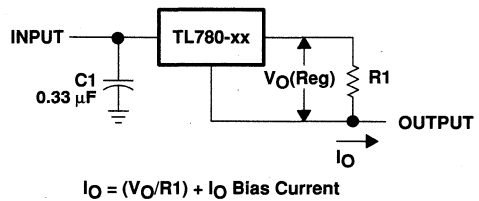


Figure 3. Current Regulator

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 4. This protects the regulator from output polarity reversals during startup and short-circuit operation.

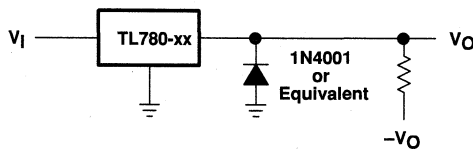


Figure 4. Output Polarity-Reversal-Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This, for example, could occur when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 5.

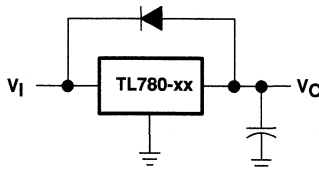


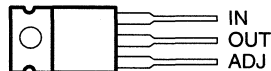
Figure 5. Reverse-Bias-Protection Circuit

TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

SLVS036D – SEPTEMBER 1981 – REVISED AUGUST 1999

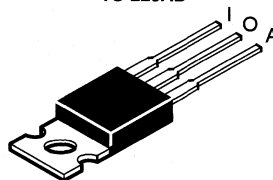
- Output Adjustable From 1.25 V to 125 V When Used With an External Resistor Divider
- 700-mA Output Current
- Full Short-Circuit, Safe-Operating-Area, and Thermal-Shutdown Protection
- 0.001%/V Typical Input Voltage Regulation
- 0.15% Typical Output Voltage Regulation
- 76-dB Typical Ripple Rejection
- Standard TO-220AB Package

KC PACKAGE
(TOP VIEW)



The OUT terminal is in electrical contact with the mounting base.

TO-220AB



description

The TL783 is an adjustable three-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary-breakdown and thermal-runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if ADJ is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

The TL783C is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

T _J	PACKAGED DEVICE	CHIP FORM (Y)
	HEAT-SINK MOUNTED (KC)	
0°C to 125°C	TL783CKC	TL783Y

Chip forms are tested at 25°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

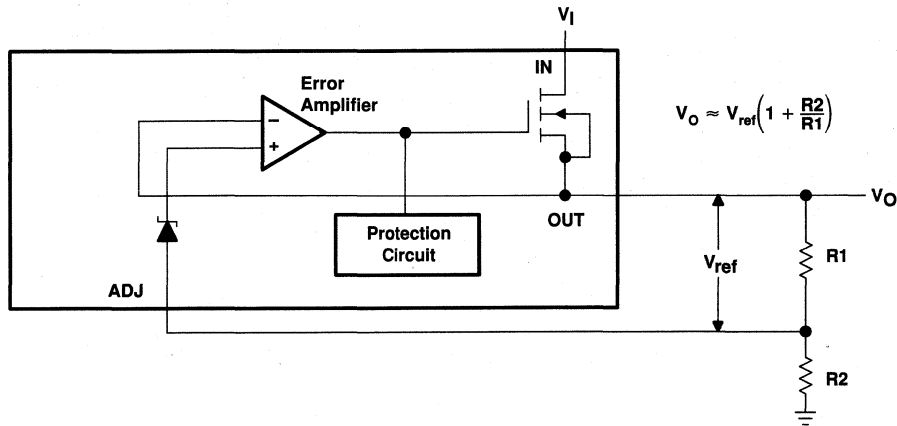
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TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

SLVS036D – SEPTEMBER 1981 – REVISED AUGUST 1999

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Input-to-output differential voltage, $V_I - V_O$	125 V
Operating free-air, T_A , case, T_C , or virtual junction, T_J , temperature range	0°C to 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2)	22°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J		0	125
	TL783C		°C

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electrical characteristics at $V_I - V_O = 25\text{ V}$, $I_O = 0.5\text{ A}$, $T_J = 0^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TL783C			UNIT
			MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O = 20\text{ V}$ to 125 V , $P \leq$ rated dissipation	$T_J = 25^\circ\text{C}$	0.001	0.01		%V
		$T_J = 0^\circ\text{C}$ to 125°C	0.004	0.02		
Ripple rejection	$\Delta V_I(\text{PP}) = 10\text{ V}$, $V_O = 10\text{ V}$, $f = 120\text{ Hz}$		66	76		dB
Output voltage regulation	$I_O = 15\text{ mA}$ to 700 mA , $T_J = 25^\circ\text{C}$	$V_O \leq 5\text{ V}$		7.5	25	mV
		$V_O \geq 5\text{ V}$		0.15%	0.5%	
	$I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation	$V_O \leq 5\text{ V}$		20	70	mV
		$V_O \geq 5\text{ V}$		0.3%	1.5%	
Output voltage change with temperature			0.4%			
Output voltage long-term drift	1000 hours at $T_J = 125^\circ\text{C}$, $V_I - V_O = 125\text{ V}$		0.2%			
Output noise voltage	$f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$		0.003%			
Minimum output current to maintain regulation	$V_I - V_O = 125\text{ V}$			15		mA
Peak output current	$V_I - V_O = 25\text{ V}$, $t = 1\text{ ms}$		1100			mA
	$V_I - V_O = 15\text{ V}$, $t = 30\text{ ms}$		715			
	$V_I - V_O = 25\text{ V}$, $t = 30\text{ ms}$		700	900		
	$V_I - V_O = 125\text{ V}$, $t = 30\text{ ms}$		100	250		
ADJ input current			83	110		μA
Change in ADJ input current	$V_I - V_O = 15\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation		0.5	5		μA
Reference voltage (OUT to ADJ)	$V_I - V_O = 10\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation, See Note 3		1.2	1.27	1.3	V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTE 3: Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

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electrical characteristics at $V_I - V_O = 25\text{ V}$, $I_O = 0.5\text{ A}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

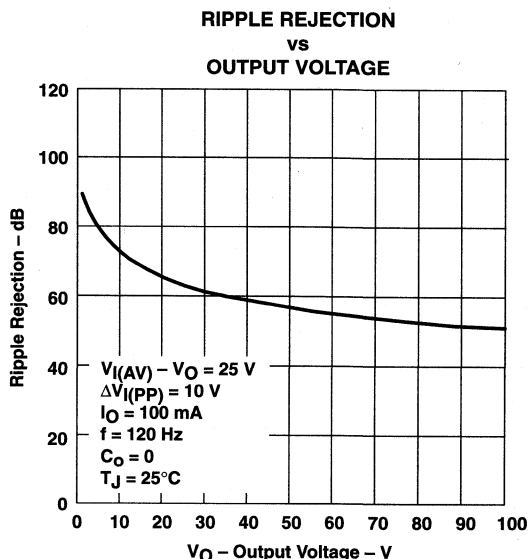
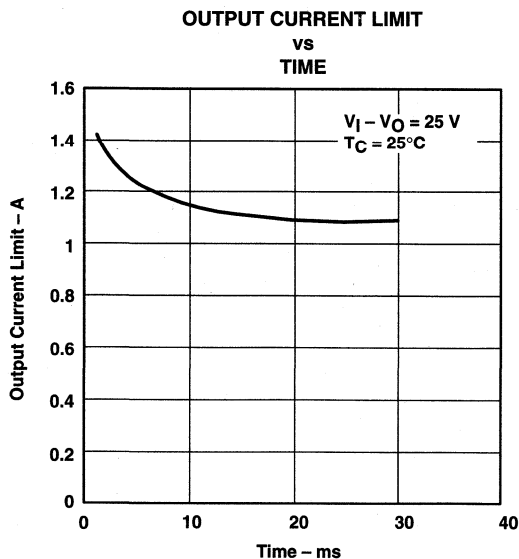
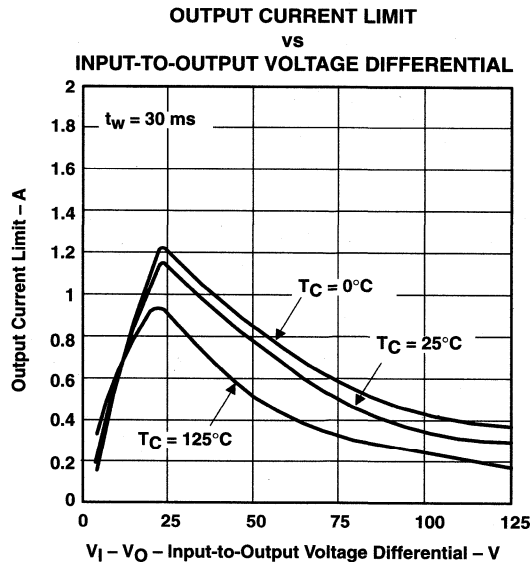
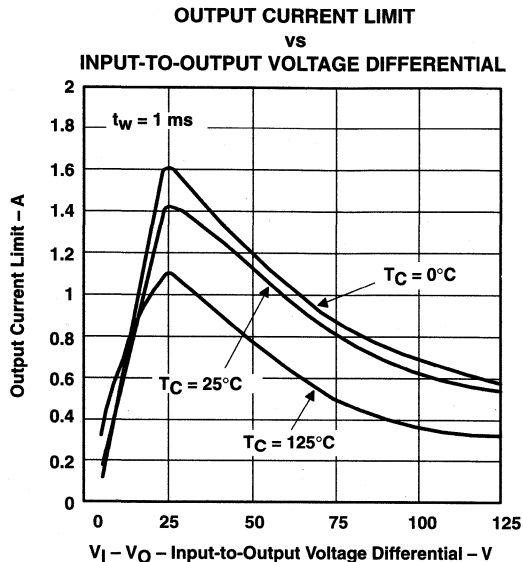
PARAMETER	TEST CONDITIONS†	TL783Y			UNIT
		MIN	TYP	MAX	
Input voltage regulation‡	$V_I - V_O = 20\text{ V to }125\text{ V}$, $P \leq \text{rated dissipation}$	0.001			%/V
Ripple rejection	$\Delta V_I(\text{PP}) = 10\text{ V}$, $V_O = 10\text{ V}$, $f = 120\text{ Hz}$	76			dB
Output voltage regulation	$I_O = 15\text{ mA to }700\text{ mA}$	$V_O \leq 5\text{ V}$	7.5		mV
		$V_O \geq 5\text{ V}$	0.15%		
	$I_O = 15\text{ mA to }700\text{ mA}$, $P \leq \text{rated dissipation}$	$V_O \leq 5\text{ V}$	20		mV
		$V_O \geq 5\text{ V}$	0.3%		
Output voltage change with temperature		0.4%			
Output noise voltage	$f = 10\text{ Hz to }10\text{ kHz}$	0.003%			
Peak output current	$V_I - V_O = 25\text{ V}$, $t = 1\text{ ms}$	1100			mA
	$V_I - V_O = 15\text{ V}$, $t = 30\text{ ms}$	715			
	$V_I - V_O = 25\text{ V}$, $t = 30\text{ ms}$	900			
	$V_I - V_O = 125\text{ V}$, $t = 30\text{ ms}$	250			
ADJ input current		83			μA
Change in ADJ input current	$V_I - V_O = 15\text{ V to }125\text{ V}$, $I_O = 15\text{ mA to }700\text{ mA}$, $P \leq \text{rated dissipation}$	0.5			μA
Reference voltage (OUT to ADJ)	$V_I - V_O = 10\text{ V to }125\text{ V}$, $I_O = 15\text{ mA to }700\text{ mA}$, $P \leq \text{rated dissipation}$, See Note 3	1.27			V

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTE 3: Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TYPICAL CHARACTERISTICS



TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

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TYPICAL CHARACTERISTICS†

**RIPPLE REJECTION
vs
OUTPUT CURRENT**

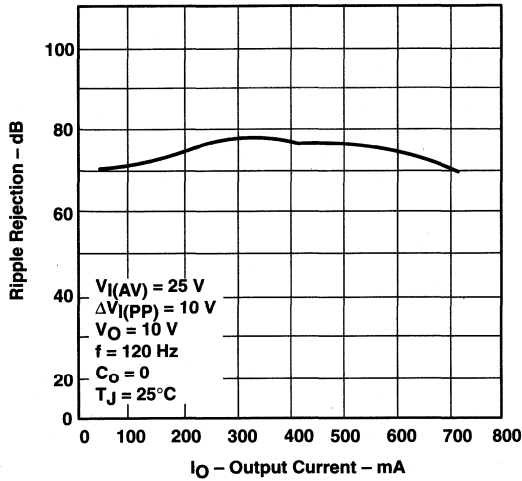


Figure 5

**RIPPLE REJECTION
vs
FREQUENCY**

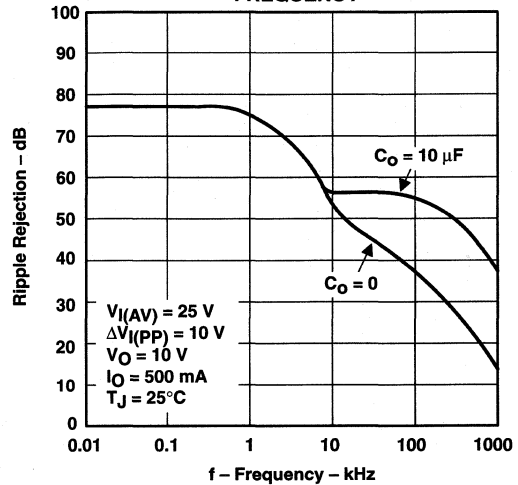


Figure 6

**OUTPUT IMPEDANCE
vs
FREQUENCY**

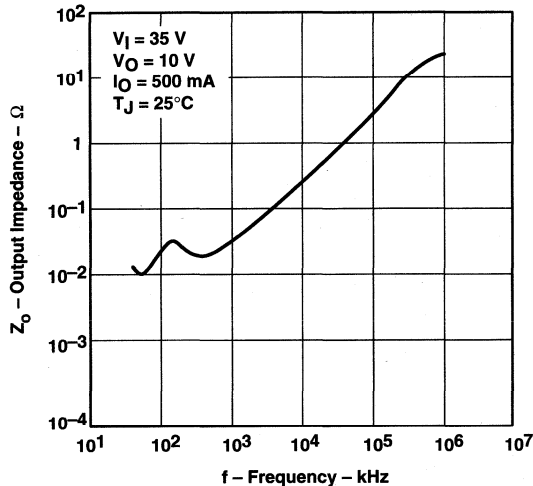


Figure 7

**REFERENCE VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE**

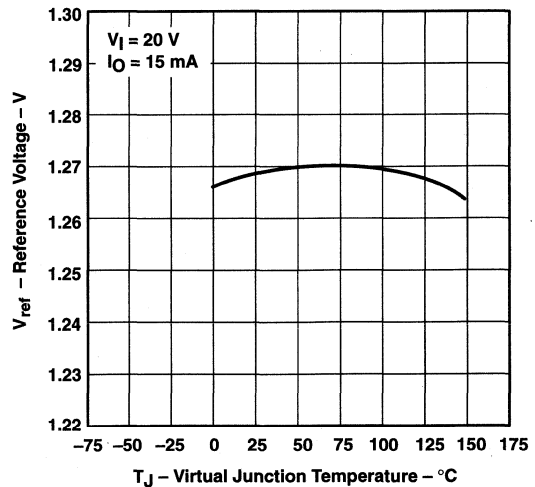


Figure 8

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

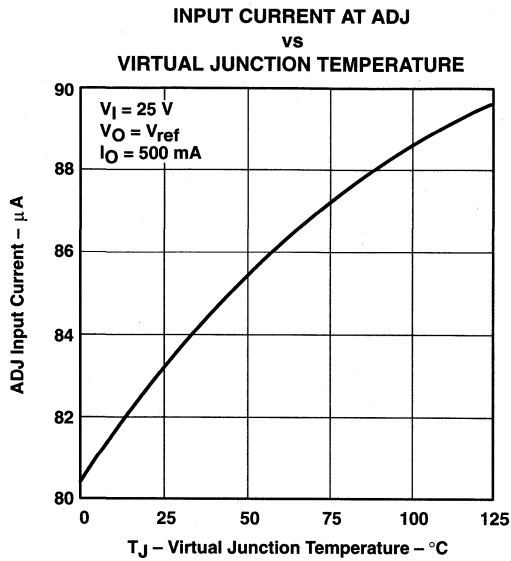


Figure 9

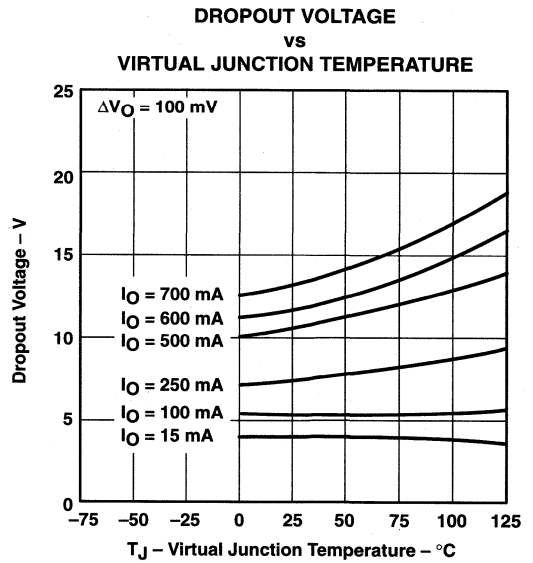


Figure 10

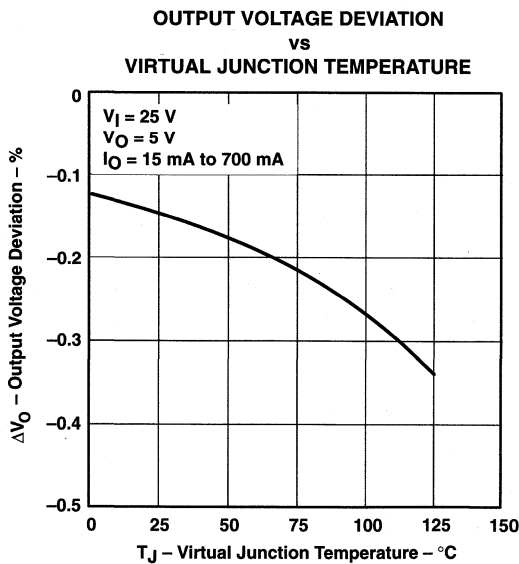
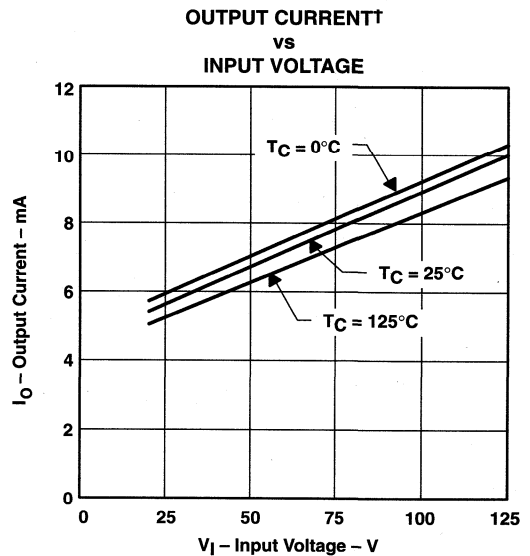


Figure 11



† This is the minimum current required to maintain voltage regulation.

Figure 12

TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

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TYPICAL CHARACTERISTICS

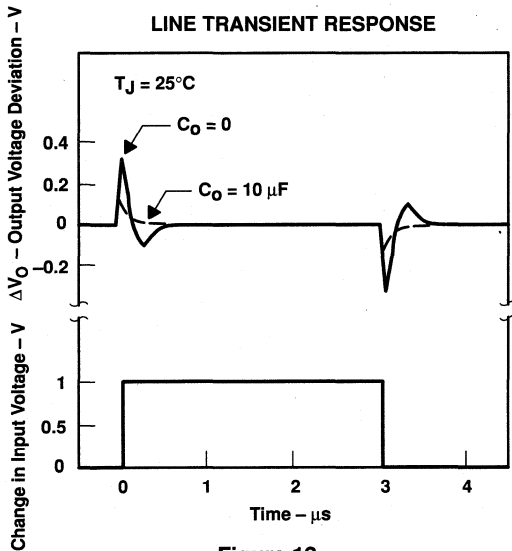


Figure 13

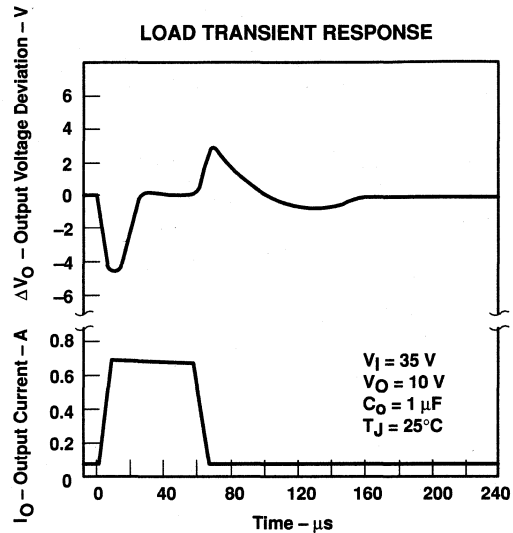


Figure 14

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) generates 1.25 V nominal (V_{ref}) between OUT and ADJ. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R_2/R_1) + I_{I(ADJ)} (R_2)$$

or

$$V_O \approx V_{ref} (1 + R_2/R_1)$$

The TL783 was designed to minimize the input current at ADJ and maintain consistency over line and load variations, thereby minimizing the associated (R_2) error term.

To maintain $I_{I(ADJ)}$ at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω provides a minimum load current of 15 mA. Larger values can be used when the input-to-output differential voltage is less than 125 V (see output-current curve, Figure 14) or when the load sinks some portion of the minimum current.

DESIGN CONSIDERATIONS

bypass capacitors

The TL783 regulator is stable without bypass capacitors; however, any regulator becomes unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1- μF tantalum or aluminum electrolytic capacitor usually is sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783 because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large load transient conditions. The addition of an output bypass capacitor greatly enhances load transient response as well as prevents dropout. For most applications, it is recommended that an output bypass capacitor be used, with a minimum value of:

$$C_O (\mu\text{F}) = 15/V_O$$

Larger values provide proportionally better transient-response characteristics.

protection circuitry

The TL783 regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783 protect the device up to maximum-rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, when rise times in excess of 10 V/ns are applied to the input, a parasitic npn transistor in parallel with the DMOS output can be turned on, causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as tantalum or aluminum electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater usually provides adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, when an instantaneous short circuit is applied to the output, both ringing and excessive fall times can result. A tantalum or aluminum electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I . A protective diode (see Figure 17) is required only for capacitance values greater than:

$$C_O (\mu\text{F}) = 3 \times 10^4 / (V_O)^2$$

Care always should be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR

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DESIGN CONSIDERATIONS

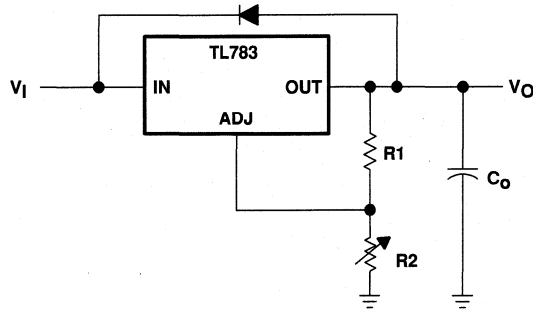


Figure 15. Regulator With Protective Diode

load regulation

The current-set resistor (R_1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R_1 and R_2 to degrade load regulation. To provide remote ground sensing, R_2 should be near the load ground.

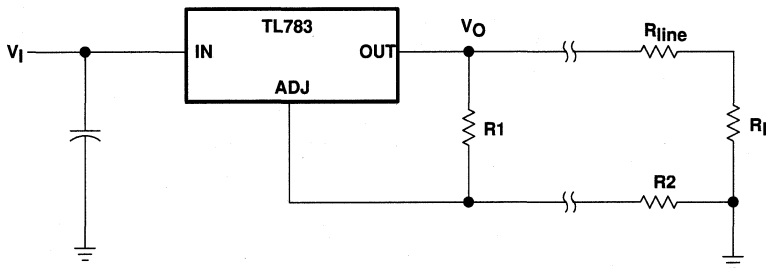
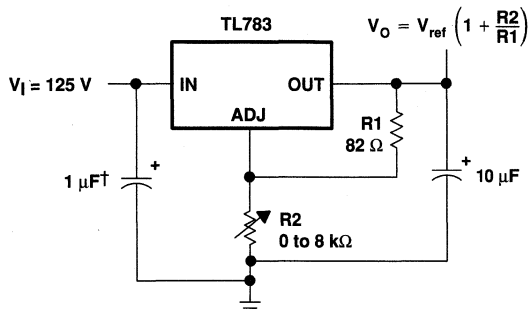


Figure 16. Regulator With Current-Set Resistor

APPLICATION INFORMATION



† Needed if device is more than 4 inches from filter capacitor

Figure 17. 1.25-V to 115-V Adjustable Regulator

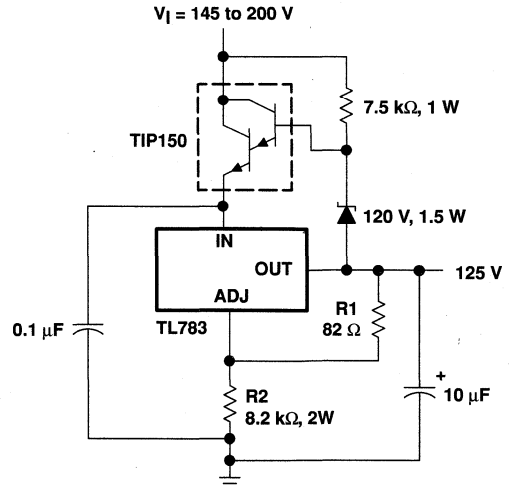


Figure 18. 125-V Short-Circuit-Protected Off-Line Regulator

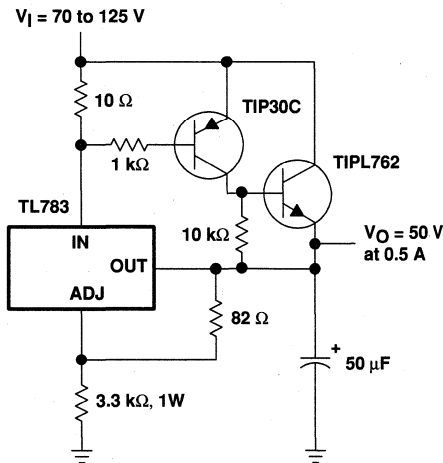


Figure 19. 50-V Regulator With Current Boost

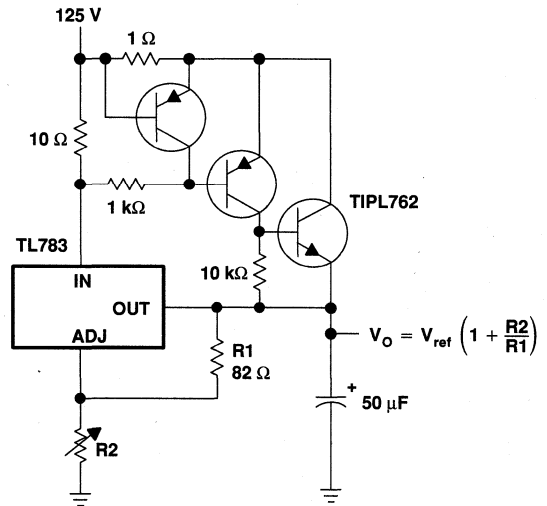


Figure 20. Adjustable Regulator With Current Boost and Current Limit

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APPLICATION INFORMATION

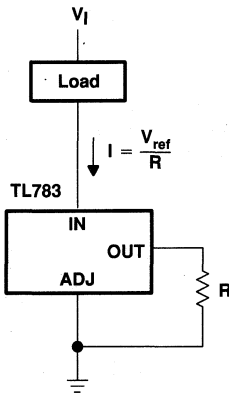


Figure 21. Current-Sinking Regulator

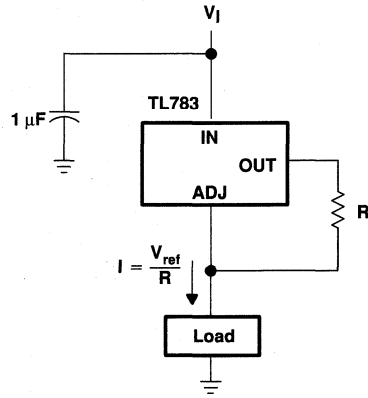


Figure 22. Current-Sourcing Regulator

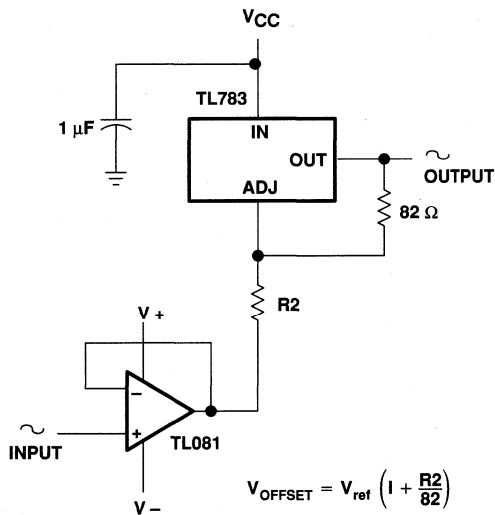


Figure 23. High-Voltage Unity-Gain Offset Amplifier

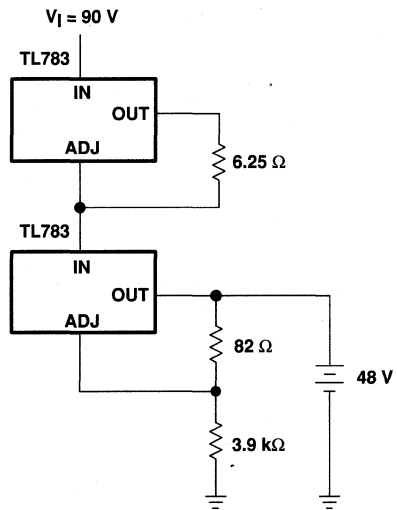


Figure 24. 48-V, 200-mA Float Charger

TLV2217-33 LOW-DROPOUT 3.3-V FIXED-VOLTAGE REGULATORS

SLVS067G – MARCH 1992 – REVISED JULY 1999

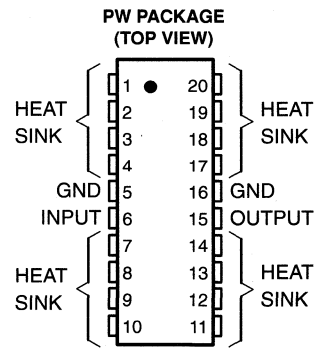
- Fixed 3.3-V Output
- $\pm 1\%$ Maximum Output Voltage Tolerance at $T_J = 25^\circ\text{C}$
- 500-mV Maximum Dropout Voltage at 500 mA
- 500-mA Dropout Current
- $\pm 2\%$ Absolute Output Voltage Variation
- Internal Overcurrent Limiting
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection
- Package Options Include Plastic Flange Mounted (KTP), Power (KC), and Thin Shrink Small-Outline (PW) Packages

description

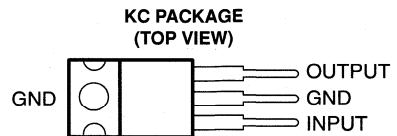
The TLV2217-33 is a low-dropout 3.3-V fixed-voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V, or less. The TLV2217-33 provides internal overcurrent limiting, thermal-overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator can drop as low as 3.8 V, and the TLV2217-33 can continue to regulate the system. For higher voltage systems, the TLV2217-33 can be operated with a continuous input voltage of 12 V.

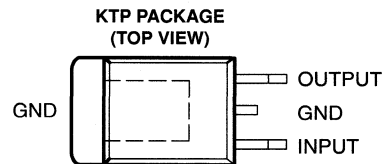
The TLV2217-33 regulators are characterized for virtual junction temperature operation from 0°C to 125°C .



HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.



The GND terminal is in electrical contact with the mounting base.



The GND terminal is in electrical contact with the mounting base.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC POWER (KC)	SURFACE MOUNT (PW)	PLASTIC FLANGE MOUNT (KTP)	
0°C to 125°C	TLV2217-33KC	TLV2217-33PW	TLV2217-33KTP	TLV2217-33Y

The KTP and PW packages are available taped and reeled only. Add R suffix to device type (e.g., TLV2212-33PWR). Chip forms are tested at 25°C .

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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TLV2217-33 LOW-DROPOUT 3.3-V FIXED-VOLTAGE REGULATORS

SLVS067G – MARCH 1992 – REVISED JULY 1999

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I	16 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2):	
KC package	22°C/W
KTP package	28°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.8	12	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at $V_I = 4.5$ V, $I_O = 500$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TLV2217-33			UNIT	
		MIN	TYP	MAX	UNIT	
Output voltage	$I_O = 20$ mA to 500 mA, $V_I = 3.8$ V to 5.5 V	$T_J = 25^\circ\text{C}$	3.267	3.30	3.333	V
		$T_J = 0^\circ\text{C}$ to 125°C	3.234		3.366	
Input voltage regulation	$V_I = 3.8$ V to 5.5 V		5	15	mV	
Ripple rejection	$f = 120$ Hz, $V_{ripple} = 1$ V _{PP}		-62		dB	
Output voltage regulation	$I_O = 20$ mA to 500 mA		5	30	mV	
Output noise voltage	$f = 10$ Hz to 100 kHz		500		µV	
Dropout voltage	$I_O = 250$ mA			400	mV	
	$I_O = 500$ mA			500		
Bias current	$I_O = 0$		2	5	mA	
	$I_O = 500$ mA		19	49		

‡ Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



TLV2217-33

LOW-DROPOUT 3.3-V FIXED-VOLTAGE REGULATORS

SLVS067G – MARCH 1992 – REVISED JULY 1999

electrical characteristics at $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TLV2217-33Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 20\text{ mA to }500\text{ mA}$, $V_I = 3.8\text{ V to }5.5\text{ V}$	3.267	3.30	3.333	V
Input voltage regulation	$V_I = 3.8\text{ V to }5.5\text{ V}$		5	15	mV
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_{\text{PP}}$		-62		dB
Output voltage regulation	$I_O = 20\text{ mA to }500\text{ mA}$		5	30	mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		500		μV
Dropout voltage	$I_O = 250\text{ mA}$			400	mV
	$I_O = 500\text{ mA}$			500	
Bias current	$I_O = 0$		2	5	mA
	$I_O = 500\text{ mA}$		19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 22- μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

TLV2217-33 LOW-DROPOUT 3.3-V FIXED-VOLTAGE REGULATORS

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COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 1 and 2 can be used to establish the capacitance value and ESR range for best regulator performance.

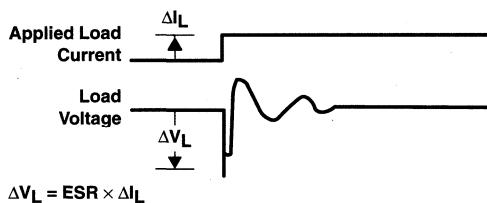
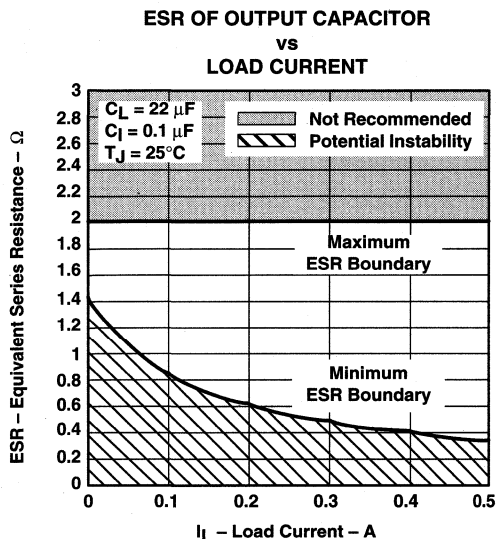


Figure 1

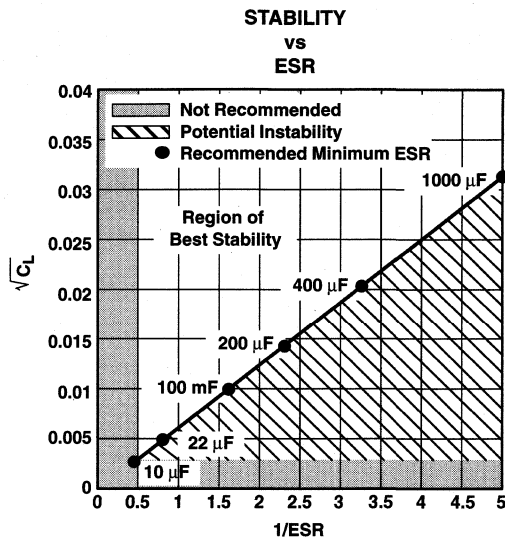


Figure 2

TLV2217-33 LOW-DROPOUT 3.3-V FIXED-VOLTAGE REGULATORS

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APPLICATION INFORMATION

application schematic

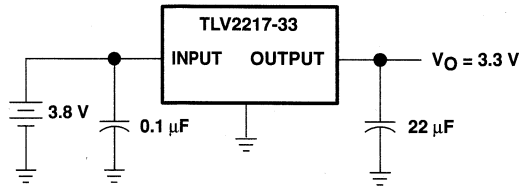


Figure 3

- 150-mA Load Current Without External Power Transistor
- Adjustable Current-Limiting Capability
- Input Voltages up to 40 V
- Output Adjustable From 2 V to 37 V
- Direct Replacement for Fairchild μA723C

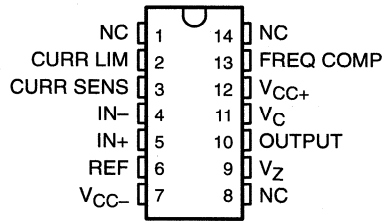
description

The μA723 is a precision integrated-circuit voltage regulator, featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference-voltage amplifier, an error amplifier, a 150-mA output transistor, and an adjustable-output current limiter.

The μA723 is designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements can be connected as shown in Figures 4 and 5.

The μA723C is characterized for operation from 0°C to 70°C.

**D OR N PACKAGE
(TOP VIEW)**

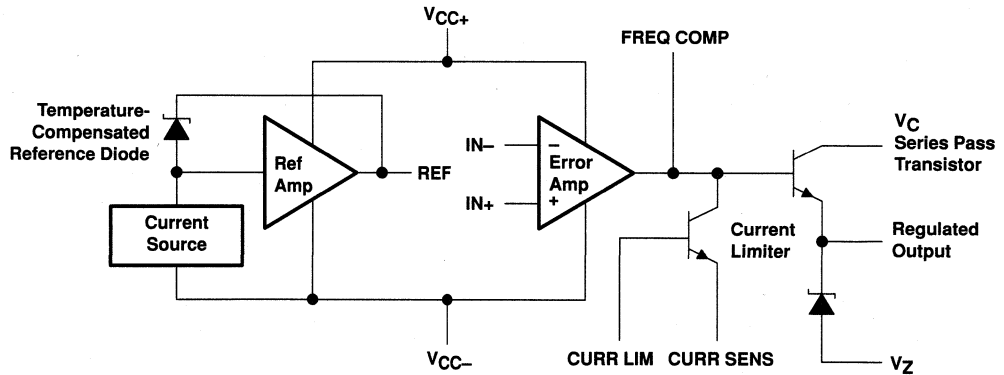


AVAILABLE OPTIONS

TA	PACKAGED DEVICES		CHIP FORM (Y)
	PLASTIC DIP (N)	SMALL OUTLINE (D)	
0°C to 70°C	μA723CN	μA723CD	μA723Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., μA723CDR). Chip forms are tested at 25°C.

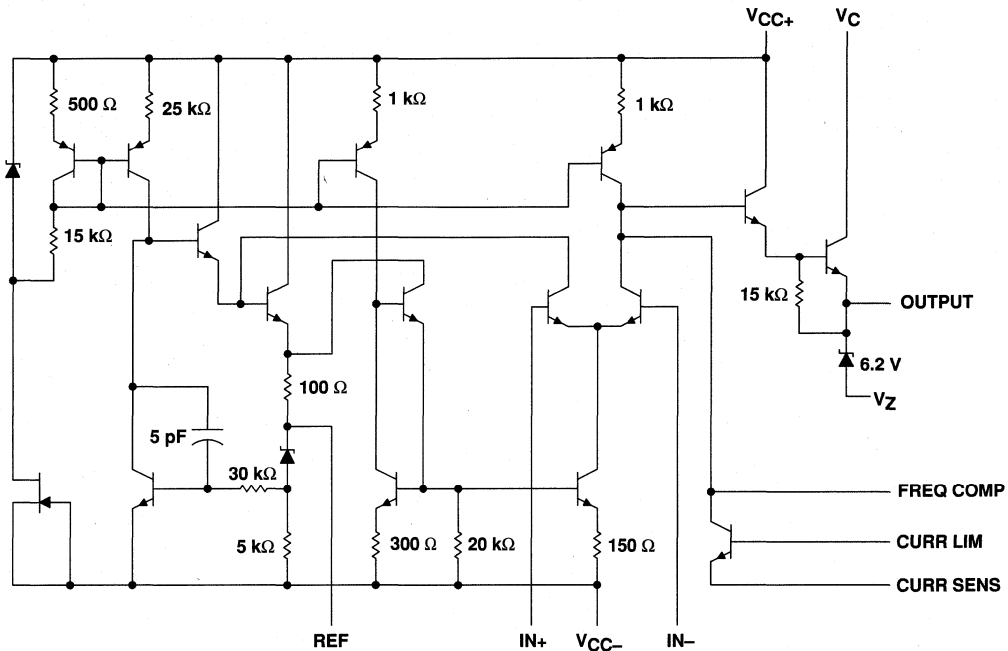
functional block diagram



μA723 PRECISION VOLTAGE REGULATORS

SLVS057D – AUGUST 1972 – REVISED JULY 1999

schematic



Resistor and capacitor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Peak voltage from V_{CC+} to V_{CC-} ($t_w \leq 50$ ms)	50 V
Continuous voltage from V_{CC+} to V_{CC-}	40 V
Input-to-output voltage differential	40 V
Differential input voltage to error amplifier	± 5 V
Voltage between noninverting input and V_{CC-}	8 V
Current from V_Z	25 mA
Current from REF	15 mA
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package	86°C/W
N package	
101°C/W	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA
Operating free-air temperature range, T_A	μA723C		0 70 °C

electrical characteristics at specified free-air temperature (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS	T_A	μA723C			UNIT
			MIN	TYP	MAX	
Input regulation	$V_I = 12\text{ V to }V_I = 15\text{ V}$	25°C	0.1 1		mV/V	
	$V_I = 12\text{ V to }V_I = 40\text{ V}$	25°C	1 5			
	$V_I = 12\text{ V to }V_I = 15\text{ V}$	0°C to 70°C	3			
Ripple rejection	$f = 50\text{ Hz to }10\text{ kHz}, C_{ref} = 0$	25°C	74		dB	
	$f = 50\text{ Hz to }10\text{ kHz}, C_{ref} = 5\text{ }\mu\text{F}$	25°C	86			
Output regulation		25°C	-0.3	-2	mV/V	
		0°C to 70°C	-6			
Reference voltage, V_{ref}		25°C	6.8	7.15	7.5	V
Standby current	$V_I = 30\text{ V}, I_O = 0$	25°C	2.3	4		mA
Temperature coefficient of output voltage		0°C to 70°C	0.003	0.015		%/°C
Short-circuit output current	$R_{SC} = 10\text{ }\Omega, V_O = 0$	25°C	65		mA	
Output noise voltage	$BW = 100\text{ Hz to }10\text{ kHz}, C_{ref} = 0$	25°C	20		μV	
	$BW = 100\text{ Hz to }10\text{ kHz}, C_{ref} = 5\text{ }\mu\text{F}$	25°C	2.5			

- NOTES: 3. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier $\leq 10\text{ k}\Omega$. Unless otherwise specified, $V_I = V_{CC+} = V_C = 12\text{ V}, V_{CC-} = 0, V_O = 5\text{ V}, I_O = 1\text{ mA}, R_{SC} = 0$, and $C_{ref} = 0$.
4. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $T_A = 25^\circ\text{C}$ (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS	μA723Y			UNIT
		MIN	TYP	MAX	
Input regulation	$V_I = 12\text{ V to }V_I = 15\text{ V}$	0.1		mV/V	
	$V_I = 12\text{ V to }V_I = 40\text{ V}$	1			
Ripple rejection	$f = 50\text{ Hz to }10\text{ kHz}, C_{ref} = 0$	74		dB	
	$f = 50\text{ Hz to }10\text{ kHz}, C_{ref} = 5\text{ }\mu\text{F}$	86			
Output regulation		-0.3	mV/V		
Reference voltage, V_{ref}		7.15	V		
Standby current	$V_I = 30\text{ V}, I_O = 0$	2.3	mA		
Short-circuit output current	$R_{SC} = 10\text{ }\Omega, V_O = 0$	65	mA		
Output noise voltage	$BW = 100\text{ Hz to }10\text{ kHz}, C_{ref} = 0$	20		μV	
	$BW = 100\text{ Hz to }10\text{ kHz}, C_{ref} = 5\text{ }\mu\text{F}$	2.5			

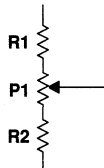
- NOTES: 3. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier $\leq 10\text{ k}\Omega$. Unless otherwise specified, $V_I = V_{CC+} = V_C = 12\text{ V}, V_{CC-} = 0, V_O = 5\text{ V}, I_O = 1\text{ mA}, R_{SC} = 0$, and $C_{ref} = 0$.
4. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

APPLICATION INFORMATION

Table 1. Resistor Values (kΩ) for Standard Output Voltages

OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 5)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 6)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	P2 (kΩ)
3.0	1, 5, 6, 9, 11, 12 (4)	4.12	3.01	1.8	0.5	1.2
3.6	1, 5, 6, 9, 11, 12 (4)	3.57	3.65	1.5	0.5	1.5
5.0	1, 5, 6, 9, 11, 12 (4)	2.15	4.99	0.75	0.5	2.2
6.0	1, 5, 6, 9, 11, 12 (4)	1.15	6.04	0.5	0.5	2.7
9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7
12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0
15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0
28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0
45	7	3.57	48.7	2.2	10	39
75	7	3.57	78.7	2.2	10	68
100	7	3.57	105	2.2	10	91
250	7	3.57	255	2.2	10	240
-6 (see Note 7)	3, 10	3.57	2.43	1.2	0.5	0.75
-9	3, 10	3.48	5.36	1.2	0.5	2.0
-12	3, 10	3.57	8.45	1.2	0.5	3.3
-15	3, 10	3.57	11.5	1.2	0.5	4.3
-28	3, 10	3.57	24.3	1.2	0.5	10
-45	8	3.57	41.2	2.2	10	33
-100	8	3.57	95.3	2.2	10	91
-250	8	3.57	249	2.2	10	240

- NOTES: 5. The R1/R2 divider can be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use the figure numbers without parentheses. If the divider is across V_O , use the figure numbers in parentheses.
6. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown below.



Adjustable Output Circuit

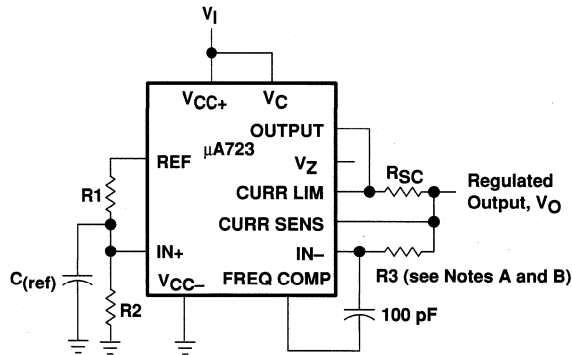
7. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than -9 V.

APPLICATION INFORMATION

Table 2. Formulas for Intermediate Output Voltages

OUTPUTS FROM 2 V TO 7 V SEE FIGURES 1, 5, 6, 9, 11, 12 (4) AND NOTE 5	OUTPUTS FROM 4 V TO 250 V SEE FIGURE 7 AND NOTE 5	CURRENT LIMITING
$V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	$V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1}$ $R3 = R4$	$I_{(limit)} \approx \frac{0.65 V}{R_{SC}}$
OUTPUTS FROM 7 V TO 37 V SEE FIGURES 2, 4, (5, 6, 9, 11, 12) AND NOTE 5	OUTPUTS FROM -6 V TO -250 V SEE FIGURES 3, 8, 10 AND NOTES 5 AND 7	FOLDBACK CURRENT LIMITING SEE FIGURE 6
$V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	$V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$ $R3 = R4$	$I_{(knee)} \approx \frac{V_O R3 + (R3 + R4) 0.65 V}{R_{SC} R4}$ $I_{OS} \approx \frac{0.65 V}{R_{SC}} \times \frac{R3 + R4}{R4}$

- NOTES: 5. The R1/R2 divider can be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use figure numbers without parentheses. If the divider is across V_O , use the figure numbers in parentheses.
7. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than -9 V.



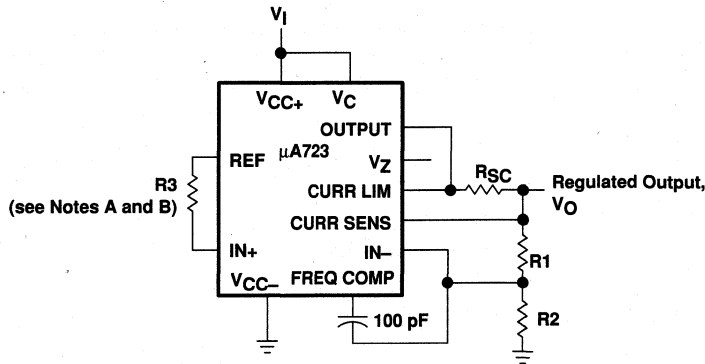
- NOTES: A. $R3 = \frac{R1 \times R2}{R1 + R2}$ for a minimum α_{V_O}
- B. R3 can be eliminated for minimum component count. Use direct connection (i.e., $R3 = 0$).

Figure 1. Basic Low-Voltage Regulator ($V_O = 2 V$ to $7 V$)

μA723
PRECISION VOLTAGE REGULATORS

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APPLICATION INFORMATION



- NOTES: A. $R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$ for a minimum α_{V_O}
 B. R_3 can be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

Figure 2. Basic High-Voltage Regulator ($V_O = 7\text{ V to }37\text{ V}$)

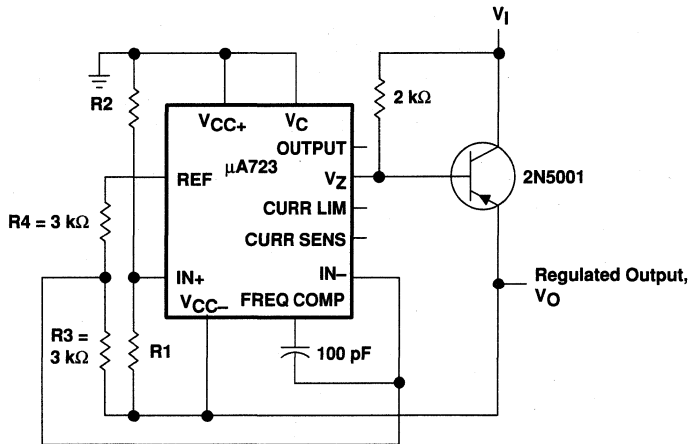


Figure 3. Negative-Voltage Regulator

APPLICATION INFORMATION

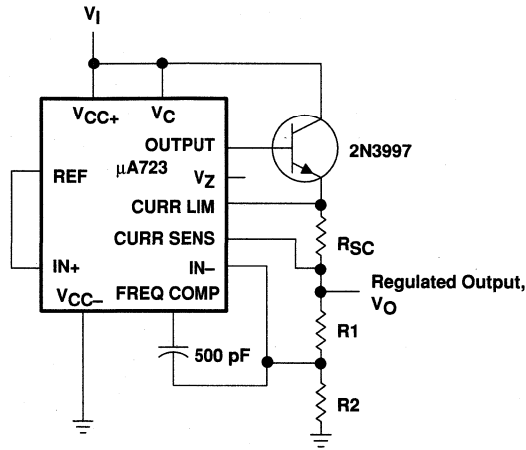


Figure 4. Positive-Voltage Regulator (External npn Pass Transistor)

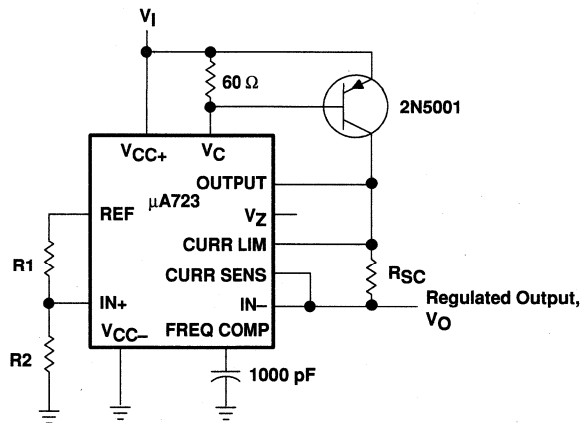


Figure 5. Positive-Voltage Regulator (External pnp Pass Transistor)

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APPLICATION INFORMATION

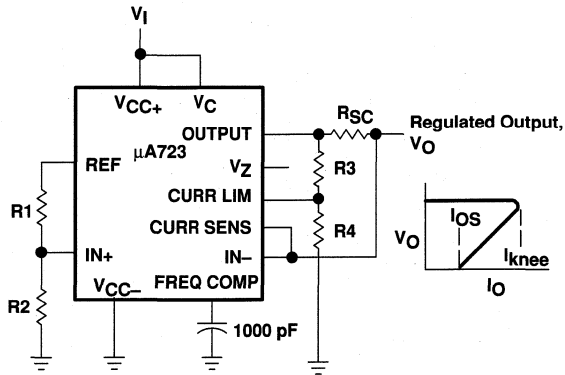


Figure 6. Foldback Current Limiting

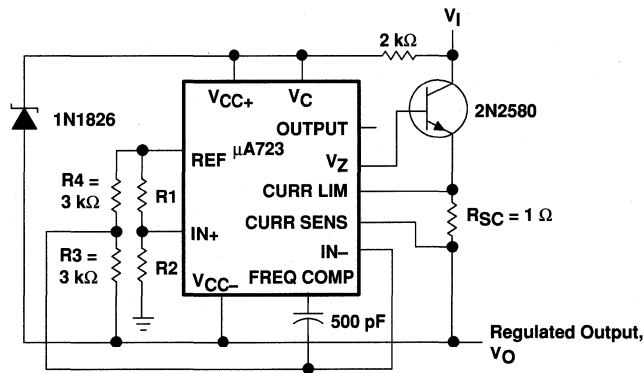


Figure 7. Positive Floating Regulator

APPLICATION INFORMATION

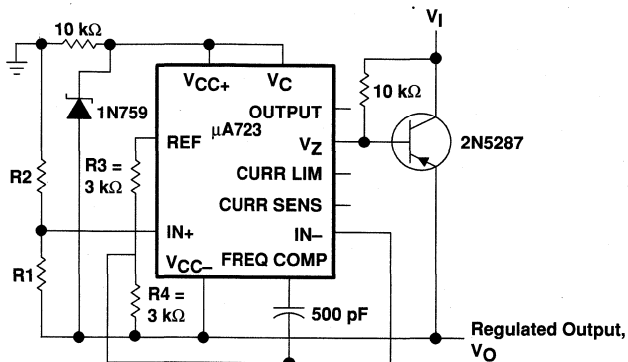
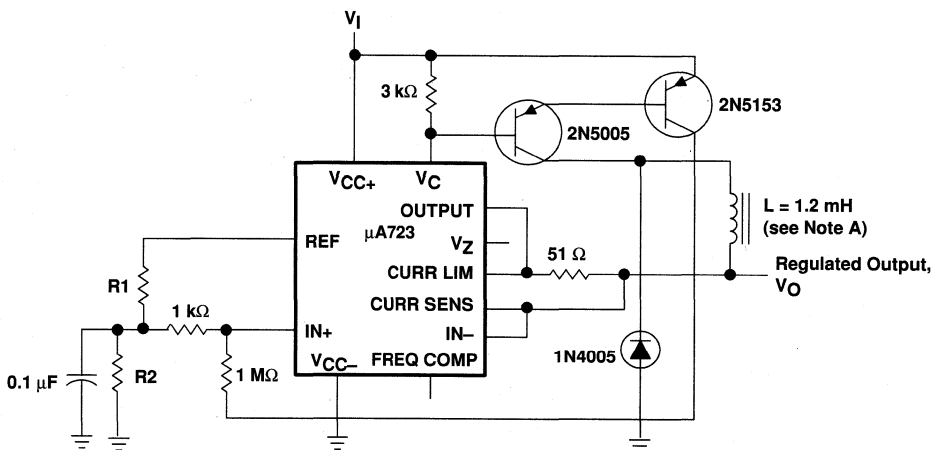


Figure 8. Negative Floating Regulator



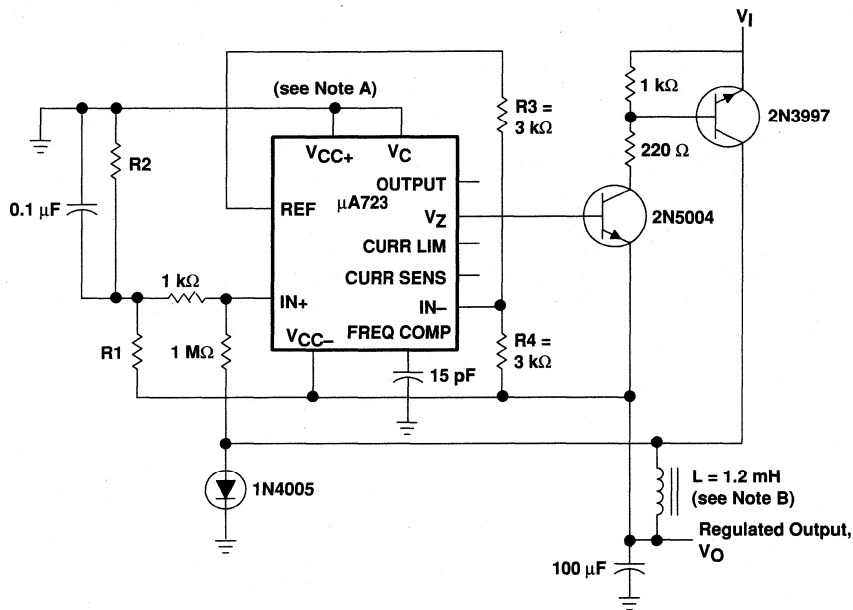
NOTE A. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with a 0.009-inch air gap.

Figure 9. Positive Switching Regulator

μ A723 PRECISION VOLTAGE REGULATORS

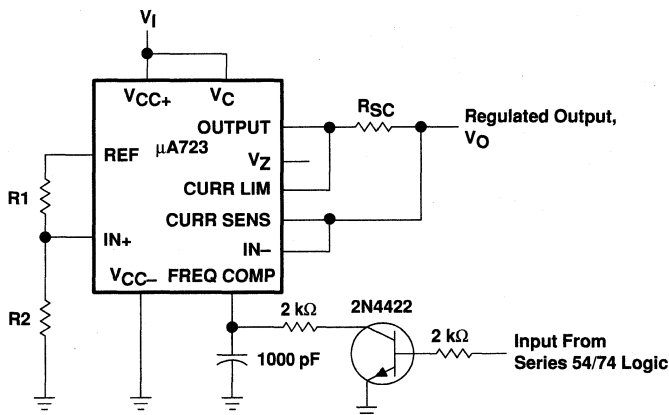
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APPLICATION INFORMATION



- NOTES: A. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than -9 V.
 B. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with a 0.009-inch air gap.

Figure 10. Negative Switching Regulator



NOTE A. A current-limiting transistor can be used for shutdown if current limiting is not required.

Figure 11. Remote Shutdown Regulator With Current Limiting

**TEXAS
INSTRUMENTS**

APPLICATION INFORMATION

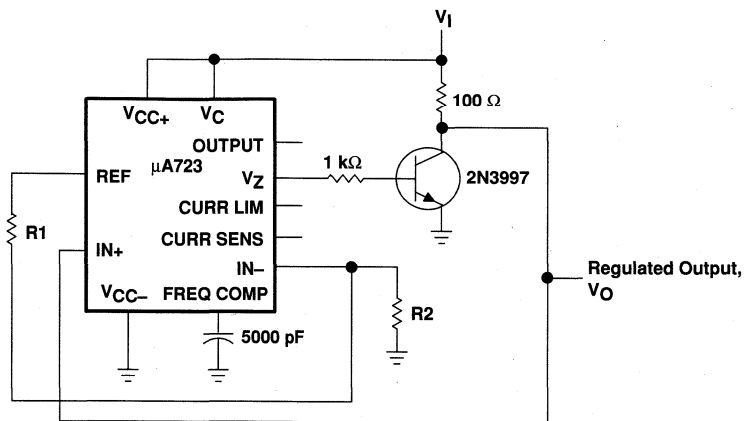


Figure 12. Shunt Regulator

μ A7800 SERIES POSITIVE-VOLTAGE REGULATORS

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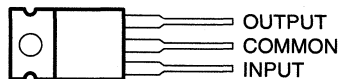
- 3-Terminal Regulators
- Output Current up to 1.5 A
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μ A7800 Series

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

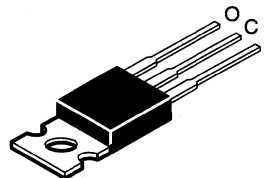
The μ A7800C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

KC PACKAGE
(TOP VIEW)

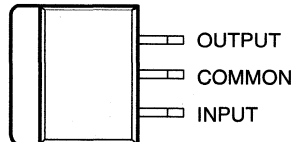


The COMMON terminal is in electrical contact with the mounting base.

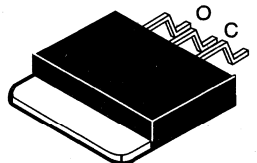
TO-220AB



KTE PACKAGE
(TOP VIEW)



The COMMON terminal is in electrical contact with the mounting base.



μA7800 SERIES POSITIVE-VOLTAGE REGULATORS

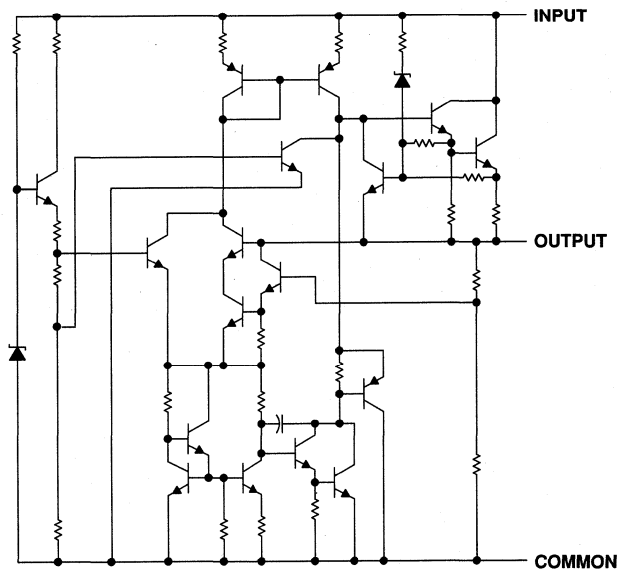
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AVAILABLE OPTIONS

T _J	V _{O(NOM)} (V)	PACKAGED DEVICES		CHIP FORM (Y)
		PLASTIC FLANGE-MOUNT (KC)	HEAT-SINK MOUNTED (KTE)	
0°C to 125°C	5	μA7805CKC	μA7805CKTE	μA7805Y
	6	μA7806CKC	μA7806CKTE	μA7806Y
	8	μA7808CKC	μA7808CKTE	μA7808Y
	8.5	μA7885CKC	μA7885CKTE	μA7885Y
	10	μA7810CKC	μA7810CKTE	μA7810Y
	12	μA7812CKC	μA7812CKTE	μA7812Y
	15	μA7815CKC	μA7815CKTE	μA7815Y
	18	μA7818CKC	μA7818CKTE	μA7818Y
	24	μA7824CKC	μA7824CKTE	μA7824Y

The KTE package is only available taped and reeled. Add the suffix R to the device type (e.g., μA7805CKTER). Chip forms are tested at 25°C.

schematic



μA7800 SERIES POSITIVE-VOLTAGE REGULATORS

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absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

		μA78xx	UNIT
Input voltage, V_I	μA7824C	40	V
	All others	35	
Virtual junction temperature range, T_J		0 to 150	°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2)	KC package	22	°C
	KTE package	23	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range, T_{stg}		-65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA7805C	7	25	V
	μA7806C	8	25	
	μA7808C	10.5	25	
	μA7885C	10.5	25	
	μA7810C	12.5	28	
	μA7812C	14.5	30	
	μA7815C	17.5	30	
	μA7818C	21	33	
	μA7824C	27	38	
Output current, I_O		1.5		A
Operating virtual junction temperature, T_J		μA7800C series		0 125 °C



μA7800 SERIES POSITIVE-VOLTAGE REGULATORS

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electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7805C			UNIT	
			MIN	TYP	MAX		
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$, $V_I = 7\text{ V to }20\text{ V}$	25°C	4.8	5	5.2	V	
		0°C to 125°C	4.75		5.25		
Input voltage regulation	$V_I = 7\text{ V to }25\text{ V}$	25°C	3			mV	
	$V_I = 8\text{ V to }12\text{ V}$		1				
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	62	78		dB	
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	15			mV	
	$I_O = 250\text{ mA to }750\text{ mA}$		5				
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.017			Ω	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1.1			mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	40			μV	
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V	
Bias current		25°C	4.2			8	mA
Bias current change	$V_I = 7\text{ V to }25\text{ V}$	0°C to 125°C				1.3	mA
	$I_O = 5\text{ mA to }1\text{ A}$					0.5	
Short-circuit output current		25°C	750			mA	
Peak output current		25°C	2.2			A	

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 11\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7806C			UNIT	
			MIN	TYP	MAX		
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$, $V_I = 8\text{ V to }21\text{ V}$	25°C	5.75	6	6.25	V	
		0°C to 125°C	5.7		6.3		
Input voltage regulation	$V_I = 8\text{ V to }25\text{ V}$	25°C	5			mV	
	$V_I = 9\text{ V to }13\text{ V}$		1.5				
Ripple rejection	$V_I = 9\text{ V to }19\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	59	75		dB	
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	14			mV	
	$I_O = 250\text{ mA to }750\text{ mA}$		4				
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.019			Ω	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-0.8			mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	45			μV	
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V	
Bias current		25°C	4.3			8	mA
Bias current change	$V_I = 8\text{ V to }25\text{ V}$	0°C to 125°C				1.3	mA
	$I_O = 5\text{ mA to }1\text{ A}$					0.5	
Short-circuit output current		25°C	550			mA	
Peak output current		25°C	2.2			A	

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electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7808C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5$ mA to 1 A, $V_I = 10.5$ V to 23 V, $P_D \leq 15$ W	25°C	7.7	8	8.3	V
		0°C to 125°C	7.6		8.4	
Input voltage regulation	$V_I = 10.5$ V to 25 V	25°C	6		160	mV
	$V_I = 11$ V to 17 V		2		80	
Ripple rejection	$V_I = 11.5$ V to 21.5 V, $f = 120$ Hz	0°C to 125°C	55	72		dB
Output voltage regulation	$I_O = 5$ mA to 1.5 A	25°C	12		160	mV
	$I_O = 250$ mA to 750 mA		4		80	
Output resistance	$f = 1$ kHz	0°C to 125°C	0.016			Ω
Temperature coefficient of output voltage	$I_O = 5$ mA	0°C to 125°C	-0.8			mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz	25°C	52			μV
Dropout voltage	$I_O = 1$ A	25°C	2			V
Bias current		25°C	4.3	8		mA
Bias current change	$V_I = 10.5$ V to 25 V	0°C to 125°C			1	mA
	$I_O = 5$ mA to 1 A				0.5	
Short-circuit output current		25°C	450			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 15$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7885C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5$ mA to 1 A, $V_I = 11$ V to 23.5 V, $P_D \leq 15$ W	25°C	8.15	8.5	8.85	V
		0°C to 125°C	8.1		8.9	
Input voltage regulation	$V_I = 10.5$ V to 25 V	25°C	6		170	mV
	$V_I = 11$ V to 17 V		2		85	
Ripple rejection	$V_I = 11.5$ V to 21.5 V, $f = 120$ Hz	0°C to 125°C	54	70		dB
Output voltage regulation	$I_O = 5$ mA to 1.5 A	25°C	12		170	mV
	$I_O = 250$ mA to 750 mA		4		85	
Output resistance	$f = 1$ kHz	0°C to 125°C	0.016			Ω
Temperature coefficient of output voltage	$I_O = 5$ mA	0°C to 125°C	-0.8			mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz	25°C	55			μV
Dropout voltage	$I_O = 1$ A	25°C	2			V
Bias current		25°C	4.3	8		mA
Bias current change	$V_I = 10.5$ V to 25 V	0°C to 125°C			1	mA
	$I_O = 5$ mA to 1 A				0.5	
Short-circuit output current		25°C	450			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 17\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_{J\uparrow}$	μA7810C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5	10	10.5	
Input voltage regulation	$V_I = 12.5\text{ V to }28\text{ V}$	25°C	7		200	mV
	$V_I = 14\text{ V to }20\text{ V}$		2		100	
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	55	71		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	12		200	mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		100	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.018			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	70			μV
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V
Bias current		25°C	4.3		8	mA
Bias current change	$V_I = 12.5\text{ V to }28\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C	400			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_{J\uparrow}$	μA7812C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$	25°C	11.5	12	12.5	V
		0°C to 125°C	11.4		12.6	
Input voltage regulation	$V_I = 14.5\text{ V to }30\text{ V}$	25°C	10		240	mV
	$V_I = 16\text{ V to }22\text{ V}$		3		120	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	55	71		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	12		240	mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		120	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.018			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	75			μV
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V
Bias current		25°C	4.3		8	mA
Bias current change	$V_I = 14.5\text{ V to }30\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C	350			mA
Peak output current		25°C	2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7815C			UNIT	
			MIN	TYP	MAX		
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$	$V_I = 17.5\text{ V to }30\text{ V}$	25°C	14.4	15	15.6	V
			0°C to 125°C	14.25		15.75	
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	25°C	11			300	mV
	$V_I = 20\text{ V to }26\text{ V}$		3			150	
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	54	70		dB	
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	12			300	mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4			150	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.019			W	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1			mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	90			μV	
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V	
Bias current		25°C	4.4			8 mA	
Bias current change	$V_I = 17.5\text{ V to }30\text{ V}$	0°C to 125°C				1	mA
	$I_O = 5\text{ mA to }1\text{ A}$					0.5	
Short-circuit output current		25°C	230			mA	
Peak output current		25°C	2.1			A	

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 27\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7818C			UNIT	
			MIN	TYP	MAX		
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$	$V_I = 21\text{ V to }33\text{ V}$	25°C	17.3	18	18.7	V
			0°C to 125°C	17.1		18.9	
Input voltage regulation	$V_I = 21\text{ V to }33\text{ V}$	25°C	15			360	mV
	$V_I = 24\text{ V to }30\text{ V}$		5			180	
Ripple rejection	$V_I = 22\text{ V to }32\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	53	69		dB	
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C	12			360	mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4			180	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.022			W	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1			mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	110			μV	
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V	
Bias current		25°C	4.5			8 mA	
Bias current change	$V_I = 21\text{ V to }33\text{ V}$	0°C to 125°C				1	mA
	$I_O = 5\text{ mA to }1\text{ A}$					0.5	
Short-circuit output current		25°C	200			mA	
Peak output current		25°C	2.1			A	

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 33\text{ V}$, $I_O = 500\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA7824C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$, $P_D \leq 15\text{ W}$	25°C	23	24	25	V
		0°C to 125°C	22.8		25.2	
Input voltage regulation	$V_I = 27\text{ V to }38\text{ V}$	25°C		18	480	mV
	$V_I = 30\text{ V to }36\text{ V}$			6	240	
Ripple rejection	$V_I = 28\text{ V to }38\text{ V}$, $f = 120\text{ Hz}$	0°C to 125°C	50	66		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	480	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	240	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C	0.028			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C	-1.5			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	170			μV
Dropout voltage	$I_O = 1\text{ A}$	25°C	2			V
Bias current		25°C	4.6	8		mA
Bias current change	$V_I = 27\text{ V to }38\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C	150			mA
Peak output current		25°C	2.1			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7805Y			UNIT
		MIN	TYP	MAX	
Output voltage		5			V
Input voltage regulation	$V_I = 7\text{ V to }25\text{ V}$	3			mV
	$V_I = 8\text{ V to }12\text{ V}$	1			
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	78			dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	15			mV
	$I_O = 250\text{ mA to }750\text{ mA}$	5			
Output resistance	$f = 1\text{ kHz}$	0.017			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	-1.1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	40			μV
Dropout voltage	$I_O = 1\text{ A}$	2			V
Bias current		4.2			mA
Short-circuit output current		750			mA
Peak output current		2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 11\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7806Y			UNIT
		MIN	TYP	MAX	
Output voltage			6		V
Input voltage regulation	$V_I = 8\text{ V to }25\text{ V}$		5		mV
	$V_I = 9\text{ V to }13\text{ V}$		1.5		
Ripple rejection	$V_I = 9\text{ V to }19\text{ V}$, $f = 120\text{ Hz}$		75		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		14		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.019		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		45		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.3		mA
Short-circuit output current			550		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7808Y			UNIT
		MIN	TYP	MAX	
Output voltage			8		V
Input voltage regulation	$V_I = 10.5\text{ V to }25\text{ V}$		6		mV
	$V_I = 11\text{ V to }17\text{ V}$		2		
Ripple rejection	$V_I = 11.5\text{ V to }21.5\text{ V}$, $f = 120\text{ Hz}$		72		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		12		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.016		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		52		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.3		mA
Short-circuit output current			450		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 15\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7885Y			UNIT
		MIN	TYP	MAX	
Output voltage			8.5		V
Input voltage regulation	$V_I = 10.5\text{ V to }25\text{ V}$		6		mV
	$V_I = 11\text{ V to }17\text{ V}$		2		
Ripple rejection	$V_I = 11.5\text{ V to }21.5\text{ V}$, $f = 120\text{ Hz}$		70		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		12		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.016		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		55		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.3		mA
Short-circuit output current			450		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 17\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7810Y			UNIT
		MIN	TYP	MAX	
Output voltage			10		V
Input voltage regulation	$V_I = 12.5\text{ V to }28\text{ V}$		7		mV
	$V_I = 14\text{ V to }20\text{ V}$		2		
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$		71		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		12		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.018		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		70		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.3		mA
Short-circuit output current			400		mA
Peak output current			2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

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electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7812Y			UNIT
		MIN	TYP	MAX	
Output voltage		12			V
Input voltage regulation	$V_I = 14.5\text{ V to }30\text{ V}$	10			mV
	$V_I = 16\text{ V to }22\text{ V}$	3			
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	71			dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	12			mV
	$I_O = 250\text{ mA to }750\text{ mA}$	4			
Output resistance	$f = 1\text{ kHz}$	0.018			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	75			μV
Dropout voltage	$I_O = 1\text{ A}$	2			V
Bias current		4.3			mA
Short-circuit output current		350			mA
Peak output current		2.2			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7815Y			UNIT
		MIN	TYP	MAX	
Output voltage		15			V
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	11			mV
	$V_I = 20\text{ V to }26\text{ V}$	3			
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	70			dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	12			mV
	$I_O = 250\text{ mA to }750\text{ mA}$	4			
Output resistance	$f = 1\text{ kHz}$	0.019			W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	90			μV
Dropout voltage	$I_O = 1\text{ A}$	2			V
Bias current		4.4			mA
Short-circuit output current		230			mA
Peak output current		2.1			A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 27\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7818Y			UNIT
		MIN	TYP	MAX	
Output voltage			18		V
Input voltage regulation	$V_I = 21\text{ V to }33\text{ V}$		15		mV
	$V_I = 24\text{ V to }30\text{ V}$		5		
Ripple rejection	$V_I = 22\text{ V to }32\text{ V}$, $f = 120\text{ Hz}$		69		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		12		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.022		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		110		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.5		mA
Short-circuit output current			200		mA
Peak output current			2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 33\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)†

PARAMETER	TEST CONDITIONS	μA7824Y			UNIT
		MIN	TYP	MAX	
Output voltage			24		V
Input voltage regulation	$V_I = 27\text{ V to }38\text{ V}$		18		mV
	$V_I = 30\text{ V to }36\text{ V}$		6		
Ripple rejection	$V_I = 28\text{ V to }38\text{ V}$, $f = 120\text{ Hz}$		66		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$		12		mV
	$I_O = 250\text{ mA to }750\text{ mA}$		4		
Output resistance	$f = 1\text{ kHz}$		0.028		W
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1.5		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		170		μV
Dropout voltage	$I_O = 1\text{ A}$		2		V
Bias current			4.6		mA
Short-circuit output current			150		mA
Peak output current			2.1		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

APPLICATION INFORMATION

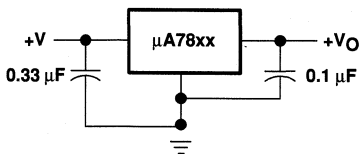


Figure 1. Fixed-Output Regulator

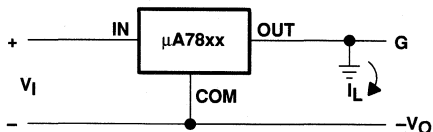
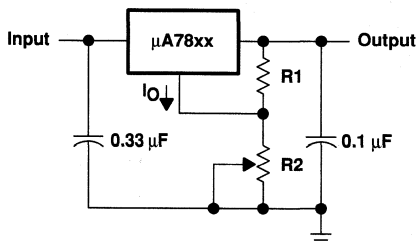


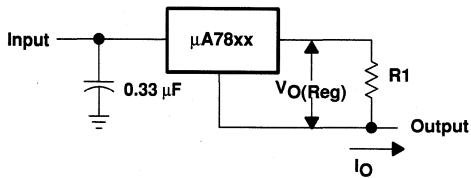
Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)



NOTE A. The following formula is used when V_{xx} is the nominal output voltage (output to common) of the fixed regulator:

$$V_O = V_{xx} + \left(\frac{V_{xx}}{R_1} + I_O \right) R_2$$

Figure 3. Adjustable-Output Regulator



$$I_O = (V_O/R_1) + I_O \text{ Bias Current}$$

Figure 4. Current Regulator

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APPLICATION INFORMATION

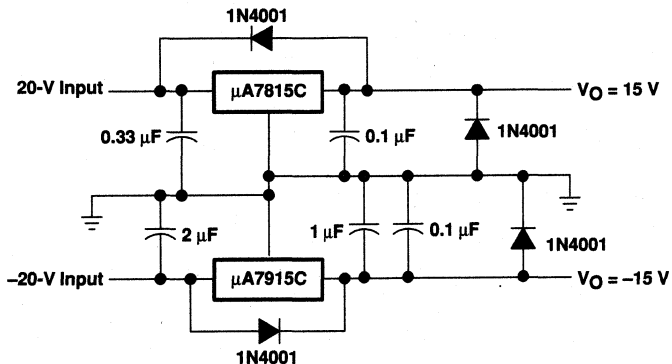


Figure 5. Regulated Dual Supply

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but, instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

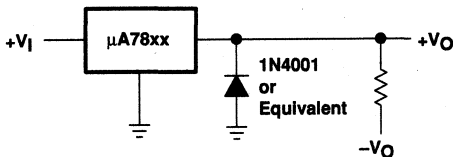


Figure 6. Output Polarity-Reversal-Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be used as shown in Figure 7.

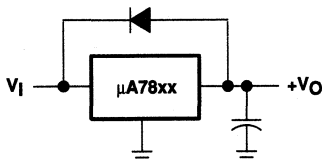


Figure 7. Reverse-Bias-Protection Circuit

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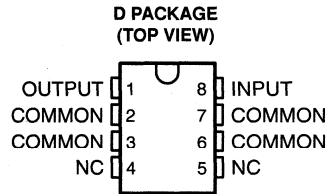
SLVS0101 – JANUARY 1976 – REVISED JULY 1999

- 3-Terminal Regulators
- Output Current up to 100 mA
- No External Components
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current Limiting
- Direct Replacements for Fairchild μA78L00 Series

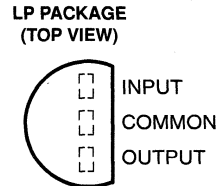
description

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower bias current.

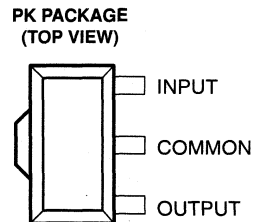
The μA78L00C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C.



NC – No internal connection



TO-226AA



AVAILABLE OPTIONS

T _J	V _{O(NOM)} (V)	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)		PLASTIC CYLINDRICAL (LP)		SOT-89 (PK)		
		OUTPUT VOLTAGE TOLERANCE						
		5%	10%	5%	10%	5%	10%	
0°C to 125°C	2.6	μA78L02ACD	–	μA78L02ACL	μA78L02CLP	μA78L02ACP	μA78L02CPK	μA78L02Y
	5	μA78L05ACD	μA78L05CD	μA78L05ACL	μA78L05CLP	μA78L05ACP	μA78L05CPK	μA78L05Y
	6.2	μA78L06ACD	μA78L06CD	μA78L06ACL	μA78L06CLP	μA78L06ACP	μA78L06CPK	μA78L06Y
	8	μA78L08ACD	μA78L08CD	μA78L08ACL	μA78L08CLP	μA78L08ACP	μA78L08CPK	μA78L08Y
	9	μA78L09ACD	μA78L09CD	μA78L09ACL	μA78L09CLP	μA78L09ACP	μA78L09CPK	μA78L09Y
	10	μA78L10ACD	–	μA78L10ACL	μA78L10CLP	μA78L10ACP	μA78L10CPK	μA78L10Y
	12	μA78L12ACD	μA78L12CD	μA78L12ACL	μA78L12CLP	μA78L12ACP	μA78L12CPK	μA78L12Y
15	μA78L15ACD	μA78L15CD	μA78L15ACL	μA78L15CLP	μA78L15ACP	μA78L15CPK	μA78L15Y	

D and LP packages are available taped and reeled. Add the suffix R to the device type (e.g., μA78L05ACDR). The PK package is only available taped and reeled (e.g., μA78L02ACPKR). Chip forms are tested at T_A = 25°C.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



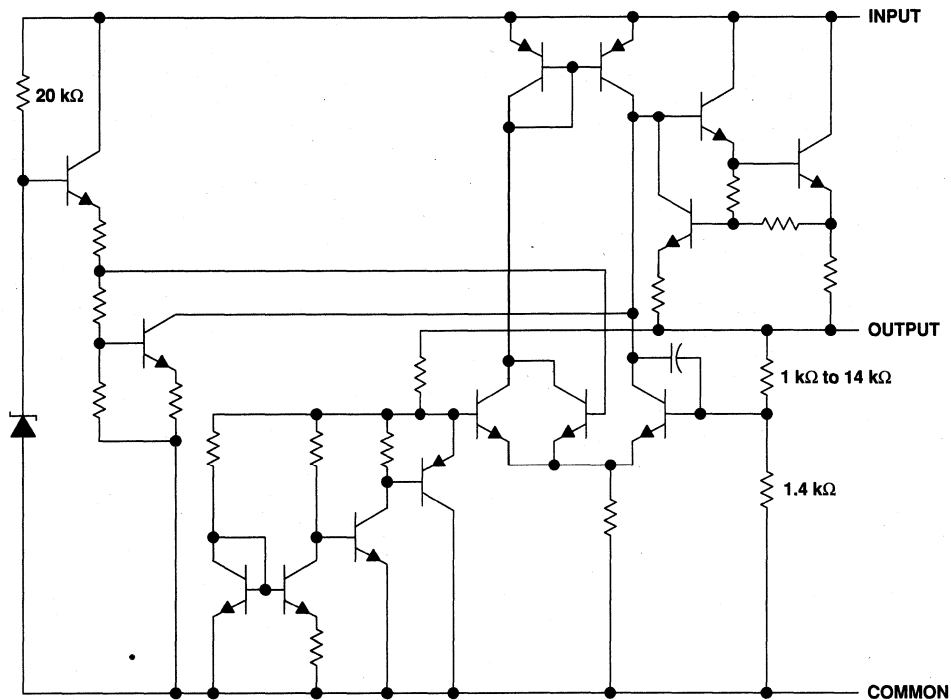
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μA78L00 SERIES POSITIVE-VOLTAGE REGULATORS

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schematic



NOTE: Resistor values shown are nominal.

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absolute maximum ratings over operating temperature range (unless otherwise noted)†

		μA78Lxx	UNIT
Input voltage, V_I	μA78L02AC, μA78L05C–μA78L09C, μA78L10AC	30	V
	μA78L12C, μA78L12AC, μA78L15C, μA78L15AC	35	
Package thermal impedance, θ_{JA} (see Notes 1 and 2)	D package	97	°C
	LP package	156	
	PK package	52	
Virtual junction temperature range, T_J		0 to 150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range, T_{stg}		–65 to 150	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA78L02AC	4.75	20	V
	μA78L05C, μA78L05AC	7	20	
	μA78L06C, μA78L06AC	8.5	20	
	μA78L08C, μA78L08AC	10.5	23	
	μA78L09C, μA78L09AC	11.5	24	
	μA78L10AC	12.5	25	
	μA78L12C, μA78L12AC	14.5	27	
	μA78L15C, μA78L15AC	17.5	30	
Output current, I_O		100		mA
Operating virtual junction temperature, T_J		0	125	°C

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electrical characteristics at specified virtual junction temperature, $V_I = 9\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L02C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 4.75\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	2.5	2.6	2.7	V
		0°C to 125°C	2.45		2.75	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	2.45		2.75	
Input voltage regulation	$V_I = 4.75\text{ V to }20\text{ V}$	25°C		20	100	mV
	$V_I = 5\text{ V to }20\text{ V}$			16	75	
Ripple rejection	$V_I = 6\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	25°C	43	51		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		12	50	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			6	25	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		30		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		3.6	6	mA
		125°C			5.5	
Bias current change	$V_I = 5\text{ V to }20\text{ V}$	0°C to 125°C			2.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L05C			μA78L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 7\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	4.6	5	5.4	4.8	5	5.2	V
		0°C to 125°C	4.5		5.5	4.75		5.25	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	4.5		5.5	4.75		5.25	
Input voltage regulation	$V_I = 7\text{ V to }20\text{ V}$	25°C		32	200		32	150	mV
	$V_I = 8\text{ V to }20\text{ V}$			26	150		26	100	
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	25°C	40	49		41	49		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		15	60		15	60	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			8	30		8	30	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 8\text{ V to }20\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 12\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L06C			μA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 8.5\text{ V to }20\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
		0°C to 125°C	5.6		6.8	5.9		6.5	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	5.6		6.8	5.9		6.5	
Input voltage regulation	$V_I = 8.5\text{ V to }20\text{ V}$	25°C		35	200		35	175	mV
	$V_I = 9\text{ V to }20\text{ V}$			29	150		29	125	
Ripple rejection	$V_I = 10\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	25°C	39	48		40	48	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		16	80		16	80	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			9	40		9	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		46			46	μV	
Dropout voltage		25°C		1.7			1.7	V	
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 9\text{ V to }20\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L08C			μA78L08AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 10.5\text{ V to }23\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	7.36	8	8.64	7.7	8	8.3	V
		0°C to 125°C	7.2		8.8	7.6		8.4	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	7.2		8.8	7.6		8.4	
Input voltage regulation	$V_I = 10.5\text{ V to }23\text{ V}$	25°C		42	200		42	175	mV
	$V_I = 11\text{ V to }23\text{ V}$			36	150		36	125	
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	25°C	36	46		37	46	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		18	80		18	80	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			10	40		10	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		54			54	μV	
Dropout voltage		25°C		1.7			1.7	V	
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 5\text{ V to }20\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 16\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L09C			μA78L09AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 12\text{ V to }24\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	8.3	9	9.7	8.6	9	9.4	V
		0°C to 125°C	8.1		9.9	8.55		9.45	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	8.1		9.9	8.55		9.45	
Input voltage regulation	$V_I = 12\text{ V to }24\text{ V}$	25°C		45	225		45	175	mV
	$V_I = 13\text{ V to }24\text{ V}$			40	175		40	125	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	36	45		38	45	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		19	90		19	90	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			11	40		11	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		58		58		μV	
Dropout voltage		25°C		1.7		1.7		V	
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	$V_I = 13\text{ V to }24\text{ V}$	0°C to 125°C			1.5			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L10AC			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 13\text{ V to }25\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	9.5		10.5	
Input voltage regulation	$V_I = 13\text{ V to }25\text{ V}$	25°C		51	175	mV
	$V_I = 14\text{ V to }25\text{ V}$			42	125	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	37	44		dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C		20	90	mV
	$I_O = 1\text{ mA to }40\text{ mA}$			11	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		62		μV
Dropout voltage		25°C		1.7		V
Bias current		25°C		4.2	6	mA
		125°C			5.5	
Bias current change	$V_I = 14\text{ V to }25\text{ V}$	0°C to 125°C			1.5	mA
	$I_O = 1\text{ mA to }40\text{ mA}$				0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L12C			μA78L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 14\text{ V to }27\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	11.1	12	12.9	11.5	12	12.5	V
		0°C to 125°C	10.8		13.2	11.4		12.6	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	10.8		13.2	11.4		12.6	
Input voltage regulation	$V_I = 14.5\text{ V to }27\text{ V}$	25°C	55		250	55		250	mV
	$V_I = 16\text{ V to }27\text{ V}$		49		200	49		200	
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	25°C	36	42		37	42	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C	22		100	22		100	mV
	$I_O = 1\text{ mA to }40\text{ mA}$		13		50	13		50	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	70			70		μV	
Dropout voltage		25°C	1.7			1.7		V	
Bias current		25°C	4.3	6.5		4.3	6.5	mA	
		125°C	6			6			
Bias current change	$V_I = 16\text{ V to }27\text{ V}$	0°C to 125°C			1.5			1.5	
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 40\text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J †	μA78L15C			μA78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 17.5\text{ V to }30\text{ V}$, $I_O = 1\text{ mA to }40\text{ mA}$	25°C	13.8	15	16.2	14.4	15	15.6	V
		0°C to 125°C	13.5		16.5	14.25		15.75	
	$I_O = 1\text{ mA to }70\text{ mA}$	0°C to 125°C	13.5		16.5	14.25		15.75	
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	25°C	65		300	65		300	mV
	$V_I = 20\text{ V to }30\text{ V}$		58		250	58		250	
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	25°C	33	39		34	39	dB	
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	25°C	25		150	25		150	mV
	$I_O = 1\text{ mA to }40\text{ mA}$		15		75	15		75	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C	82			82		μV	
Dropout voltage		25°C	1.7			1.7		V	
Bias current		25°C	4.6	6.5		4.6	6.5	mA	
		125°C	6			6			
Bias current change	$V_I = 10\text{ V to }30\text{ V}$	0°C to 125°C			1.5			1.5	
	$I_O = 1\text{ mA to }40\text{ mA}$				0.2			0.1	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 9\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L02Y			UNIT
		MIN	TYP	MAX	
Output voltage		2.6			V
Input voltage regulation	$V_I = 4.75\text{ V to }20\text{ V}$	20			mV
	$V_I = 5\text{ V to }20\text{ V}$	16			
Ripple rejection	$V_I = 6\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	51			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	12			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	6			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	30			μV
Dropout voltage		1.7			V
Bias current		3.6			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L05Y			UNIT
		MIN	TYP	MAX	
Output voltage		5			V
Input voltage regulation	$V_I = 7\text{ V to }20\text{ V}$	32			mV
	$V_I = 8\text{ V to }20\text{ V}$	26			
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	49			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	15			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	8			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	42			μV
Dropout voltage		1.7			V
Bias current		3.8			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 12\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA78L06Y			UNIT
		MIN	TYP	MAX	
Output voltage		6.2			V
Input voltage regulation	$V_I = 8.5\text{ V to }20\text{ V}$	35			mV
	$V_I = 9\text{ V to }20\text{ V}$	29			
Ripple rejection	$V_I = 10\text{ V to }20\text{ V}$, $f = 120\text{ Hz}$	48			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	16			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	9			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	46			μV
Dropout voltage		1.7			V
Bias current		3.9			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78L08Y			UNIT
		MIN	TYP	MAX	
Output voltage		8			V
Input voltage regulation	$V_I = 10.5\text{ V to }23\text{ V}$	42			mV
	$V_I = 11\text{ V to }23\text{ V}$	36			
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	46			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	18			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	10			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	54			μV
Dropout voltage		1.7			V
Bias current		4			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 16\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78L09Y			UNIT
		MIN	TYP	MAX	
Output voltage		9			V
Input voltage regulation	$V_I = 12\text{ V to }24\text{ V}$	45			mV
	$V_I = 13\text{ V to }24\text{ V}$	40			
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	45			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	19			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	11			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	58			μV
Dropout voltage		1.7			V
Bias current		4.1			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 40\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78L10Y			UNIT
		MIN	TYP	MAX	
Output voltage		10			V
Input voltage regulation	$V_I = 13\text{ V to }25\text{ V}$	51			mV
	$V_I = 14\text{ V to }25\text{ V}$	42			
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	44			dB
Output voltage regulation	$I_O = 1\text{ mA to }100\text{ mA}$	20			mV
	$I_O = 1\text{ mA to }40\text{ mA}$	11			
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	62			μV
Dropout voltage		1.7			V
Bias current		4.2			mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = 19$ V, $I_O = 40$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μ A78L12Y			UNIT
		MIN	TYP	MAX	
Output voltage			12		V
Input voltage regulation	$V_I = 14.5$ V to 27 V		55		mV
	$V_I = 16$ V to 27 V		49		
Ripple rejection	$V_I = 15$ V to 25 V, $f = 120$ Hz		42		dB
Output voltage regulation	$I_O = 1$ mA to 100 mA		22		mV
	$I_O = 1$ mA to 40 mA		13		
Output noise voltage	$f = 10$ Hz to 100 kHz		70		μ V
Dropout voltage			1.7		V
Bias current			4.3		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μ F capacitor across the input and a 0.1- μ F capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 40$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μ A78L15Y			UNIT
		MIN	TYP	MAX	
Output voltage			15		V
Input voltage regulation	$V_I = 17.5$ V to 30 V		65		mV
	$V_I = 20$ V to 30 V		58		
Ripple rejection	$V_I = 18.5$ V to 28.5 V, $f = 120$ Hz		39		dB
Output voltage regulation	$I_O = 1$ mA to 100 mA		25		mV
	$I_O = 1$ mA to 40 mA		15		
Output noise voltage	$f = 10$ Hz to 100 kHz		82		μ V
Dropout voltage			1.7		V
Bias current			4.6		mA

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- μ F capacitor across the input and a 0.1- μ F capacitor across the output.

APPLICATION INFORMATION

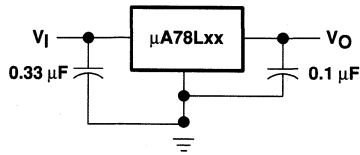


Figure 1. Fixed-Output Regulator

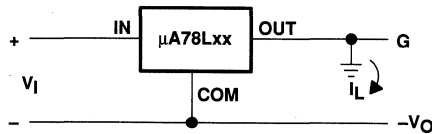


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

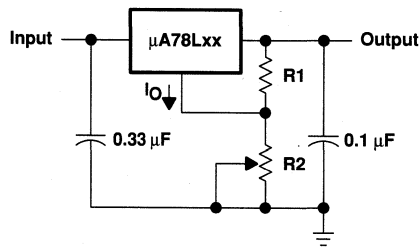
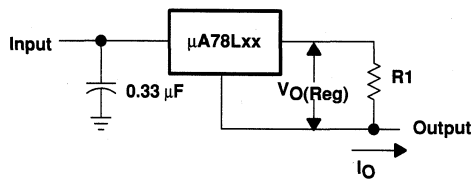


Figure 3. Adjustable-Output Regulator



$$I_O = (V_O/R1) + I_O \text{ Bias Current}$$

Figure 4. Current Regulator

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APPLICATION INFORMATION

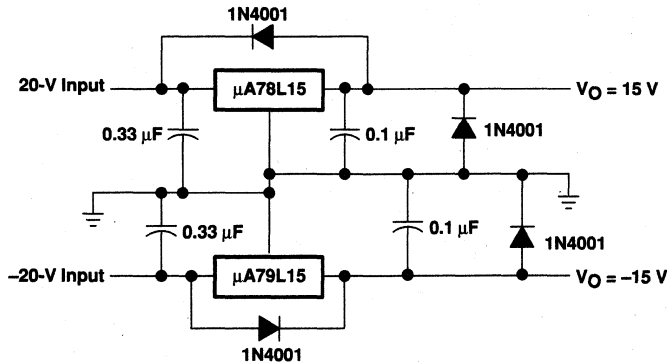


Figure 5. Regulated Dual Supply

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but, instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

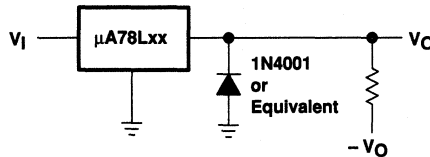


Figure 6. Output Polarity-Reversal-Protection Circuit

reverse-bias protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 7.

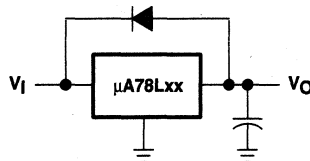


Figure 7. Reverse-Bias-Protection Circuit

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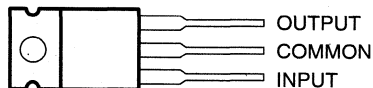
- 3-Terminal Regulators
- Output Current up to 500 mA
- No External Components
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μ A78M00 Series

description

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

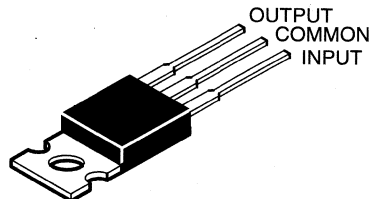
The μ A78M00C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

KC PACKAGE
(TOP VIEW)

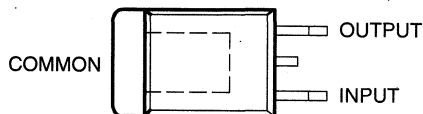


The COMMON terminal is in electrical contact with the mounting base.

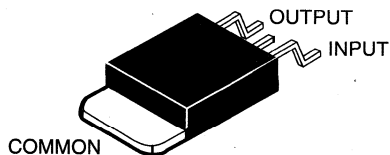
TO-220AB



KTP PACKAGE
(TOP-VIEW)



The COMMON terminal is in electrical contact with the mounting base.



μA78M00 SERIES POSITIVE-VOLTAGE REGULATORS

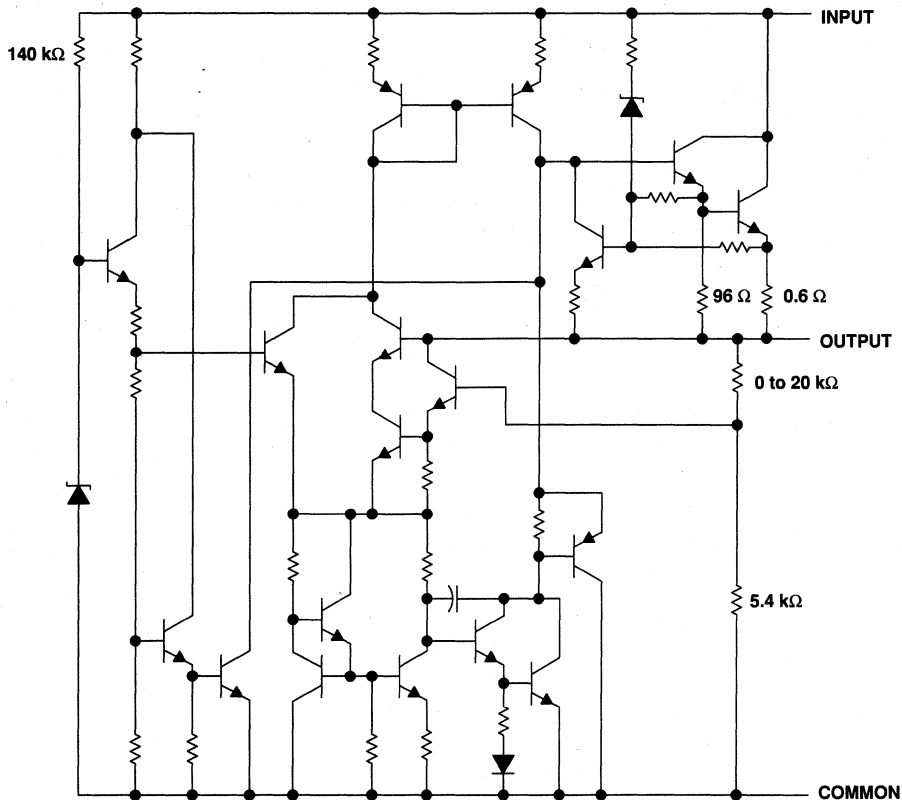
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AVAILABLE OPTIONS

T _J	V _{O(NOM)} (V)	PACKAGED DEVICES		CHIP FORM (Y)
		HEAT-SINK MOUNTED (KC)	PLASTIC FLANGE MOUNTED (KTP)	
0°C to 125°C	5	μA78M05CKC	μA78M05CKTP	μA78M05Y
	6	μA78M06CKC	μA78M06CKTP	μA78M06Y
	8	μA78M08CKC	μA78M08CKTP	μA78M08Y
	9	μA78M09CKC	μA78M09CKTP	μA78M09Y
	10	μA78M10CKC	μA78M10CKTP	μA78M10Y
	12	μA78M12CKC	μA78M12CKTP	μA78M12Y
	15	μA78M15CKC	μA78M15CKTP	μA78M15Y
	20	μA78M20CKC	μA78M20CKTP	μA78M20Y
	24	μA78M24CKC	μA78M24CKTP	μA78M24Y

The KTP package is only available taped and reeled. Add the suffix R to the device type (e.g., μA78M05CKTPR). Chip forms are tested at 25°C.

schematic



Resistor values shown are nominal.

 **TEXAS
INSTRUMENTS**

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μA78M00 SERIES POSITIVE-VOLTAGE REGULATORS

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absolute maximum ratings over operating temperature range (unless otherwise noted)†

	μA78Mxx	UNIT
Input voltage, V_I	μA78M20, μA78M24	40
	All others	35
Package thermal impedance, θ_{JA} (see Notes 1 and 2)	KC package	22
	KTP package	28
Virtual junction temperature range, T_J		0 to 150
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260
Storage temperature range, T_{stg}		-65 to 150

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA78M05	7	25	V
	μA78M06	8	25	
	μA78M08	10.5	25	
	μA78M09	11.5	26	
	μA78M10	12.5	28	
	μA78M12	14.5	30	
	μA78M15	17.5	30	
	μA78M24	27	38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J		0	125	°C



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electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78M05C			UNIT	
		MIN	TYP	MAX		
Output voltage	$V_I = 7\text{ V to }20\text{ V}$ $T_J = 0^\circ\text{C to }125^\circ\text{C}$		4.8	5	5.2	V
			4.75		5.25	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 7\text{ V to }25\text{ V}$		3	100	mV
		$V_I = 8\text{ V to }20\text{ V}$				
		$V_I = 8\text{ V to }25\text{ V}$		1	50	
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	62			dB
		$I_O = 300\text{ mA}$	62	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		20	100	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	50		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		40	200	μV	
Dropout voltage			2		V	
Bias current			4.5	6	mA	
Bias current change	$I_O = 200\text{ mA}$, $V_I = 8\text{ V to }25\text{ V}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		300		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 11\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78M06C			UNIT	
		MIN	TYP	MAX		
Output voltage	$I_O = 5\text{ mA to }350\text{ mA}$, $V_I = 8\text{ V to }21\text{ V}$ $T_J = 0^\circ\text{C to }125^\circ\text{C}$		5.75	6	6.25	V
			5.7		6.3	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 8\text{ V to }25\text{ V}$		5	100	mV
		$V_I = 9\text{ V to }25\text{ V}$		1.5	50	
Ripple rejection	$V_I = 9\text{ V to }19\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	59			dB
		$I_O = 300\text{ mA}$	59	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		20	120	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	60		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		45		μV	
Dropout voltage			2		V	
Bias current			4.5	6	mA	
Bias current change	$V_I = 9\text{ V to }25\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		270		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 14\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M08C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 10.5\text{ V to }23\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$		7.7	8	8.3	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$		7.6	8.4	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 10.5\text{ V to }25\text{ V}$		6	100	mV
		$V_I = 11\text{ V to }25\text{ V}$		2	50	
Ripple rejection	$V_I = 11.5\text{ V to }21.5\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	56			dB
		$I_O = 300\text{ mA}$	56	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25	160	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	80		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		52		μV	
Dropout voltage			2		V	
Bias current			4.6	6	mA	
Bias current change	$V_I = 10.5\text{ V to }25\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		250		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 16\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M09C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 11.5\text{ V to }24\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$		8.6	9	9.4	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$		8.5	9.5	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 11.5\text{ V to }26\text{ V}$		6	100	mV
		$V_I = 12\text{ V to }26\text{ V}$		2	50	
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	56			dB
		$I_O = 300\text{ mA}$	56	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25	180	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	90		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		58		μV	
Dropout voltage			2		V	
Bias current			4.6	6	mA	
Bias current change	$V_I = 11.5\text{ V to }26\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		250		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 17\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M10C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 12.5\text{ V to }25\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	9.6	10	10.4	V
			9.5		10.5	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 12.5\text{ V to }28\text{ V}$	7	100	mV	
		$V_I = 14\text{ V to }28\text{ V}$	2	50		
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $I_O = 300\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	59		dB	
			55	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25	200	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	100		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		64		μV	
Dropout voltage			2		V	
Bias current			4.7	6	mA	
Bias current change	$V_I = 12.5\text{ V to }28\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		245		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M12C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 14.5\text{ V to }27\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	11.5	12	12.5	V
			11.4		12.6	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 14.5\text{ V to }30\text{ V}$	8	100	mV	
		$V_I = 16\text{ V to }30\text{ V}$	2	50		
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $I_O = 300\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	55		dB	
			55	80		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25	240	mV	
	$I_O = 5\text{ mA to }200\text{ mA}$		10	120		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1		mV/°C	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		75		μV	
Dropout voltage			2		V	
Bias current			4.8	6	mA	
Bias current change	$V_I = 14.5\text{ V to }30\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.8	mA	
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$			0.5		
Short-circuit output current	$V_I = 35\text{ V}$		240		mA	
Peak output current			0.7		A	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST		μA78M15C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 17.5\text{ V to }30\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$		14.4	15	15.6	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	14.25		15.75	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 17.5\text{ V to }30\text{ V}$		10	100	mV
		$V_I = 20\text{ V to }30\text{ V}$		3	50	
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	54			dB
		$I_O = 300\text{ mA}$	54	70		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$			25	300	mV
	$I_O = 5\text{ mA to }200\text{ mA}$			10	150	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		90			μV
Dropout voltage			2			V
Bias current			4.8	6		mA
Bias current change	$V_I = 17.5\text{ V to }30\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.8	mA
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.5	
Short-circuit output current	$V_I = 35\text{ V}$		240			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 29\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST		μA78M20C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 23\text{ V to }35\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$		19.2	20	20.8	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	19		21	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 23\text{ V to }35\text{ V}$		10	100	mV
		$V_I = 24\text{ V to }35\text{ V}$		5	50	
Ripple rejection	$V_I = 24\text{ V to }34\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	53			dB
		$I_O = 300\text{ mA}$	53	70		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$			30	400	mV
	$I_O = 5\text{ mA to }200\text{ mA}$			10	200	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1.1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		110			μV
Dropout voltage			2			V
Bias current			4.9	6		mA
Bias current change	$V_I = 23\text{ V to }35\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.8	mA
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.5	
Short-circuit output current	$V_I = 35\text{ V}$		240			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 33\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M24C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = 27\text{ V to }38\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$		23	24	25	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	22.8		25.2	
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 27\text{ V to }38\text{ V}$		10	100	mV
		$V_I = 28\text{ V to }38\text{ V}$		5	50	
Ripple rejection	$V_I = 28\text{ V to }38\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$	50			dB
		$I_O = 300\text{ mA}$	50	70		
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$			30	480	mV
	$I_O = 5\text{ mA to }200\text{ mA}$			10	240	
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		-1.2			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$			170		μV
Dropout voltage				2		V
Bias current				5	6	mA
Bias current change	$V_I = 27\text{ V to }38\text{ V}$, $I_O = 200\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.8	mA
	$I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$				0.5	
Short-circuit output current	$V_I = 35\text{ V}$			240		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 10\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M05Y			UNIT
			MIN	TYP	MAX	
Output voltage				5		V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 7\text{ V to }25\text{ V}$		3		mV
		$V_I = 8\text{ V to }25\text{ V}$		1		
Ripple rejection	$V_I = 8\text{ V to }18\text{ V}$, $I_O = 300\text{ mA}$, $f = 120\text{ Hz}$		80			dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$			20		mV
	$I_O = 5\text{ mA to }200\text{ mA}$			10		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$			-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$			40		μV
Dropout voltage				2		V
Bias current				4.5		mA
Short-circuit output current	$V_I = 35\text{ V}$			300		mA
Peak output current				0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 11$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M06Y			UNIT
			MIN	TYP	MAX	
Output voltage			6			V
Input voltage regulation	$I_O = 200$ mA	$V_I = 8$ V to 25 V	5			mV
		$V_I = 9$ V to 25 V	1.5			
Ripple rejection	$V_I = 9$ V to 19 V,	$I_O = 300$ mA, $f = 120$ Hz	80			dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		20			mV
	$I_O = 5$ mA to 200 mA		10			
Temperature coefficient of output voltage	$I_O = 5$ mA		-1			mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		45			μV
Dropout voltage			2			V
Bias current			4.5			mA
Short-circuit output current	$V_I = 35$ V		270			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M08Y			UNIT
			MIN	TYP	MAX	
Output voltage			8			V
Input voltage regulation	$I_O = 200$ mA	$V_I = 10.5$ V to 25 V	6			mV
		$V_I = 11$ V to 25 V	2			
Ripple rejection	$V_I = 11.5$ V to 21.5 V,	$I_O = 300$ mA, $f = 120$ Hz	80			dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		25			mV
	$I_O = 5$ mA to 200 mA		10			
Temperature coefficient of output voltage	$I_O = 5$ mA		-1			mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		52			μV
Dropout voltage			2			V
Bias current			4.6			mA
Short-circuit output current	$V_I = 35$ V		250			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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**electrical characteristics at specified virtual junction temperature, $V_I = 16\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$
(unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		μA78M09Y			UNIT
			MIN	TYP	MAX	
Output voltage			9			V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 11.5\text{ V to }26\text{ V}$	6			mV
		$V_I = 12\text{ V to }26\text{ V}$	2			
Ripple rejection	$V_I = 13\text{ V to }23\text{ V}$,	$I_O = 300\text{ mA}$, $f = 120\text{ Hz}$	80			dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25			mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$,	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		58			μV
Dropout voltage			2			V
Bias current			4.6			mA
Short-circuit output current	$V_I = 35\text{ V}$		250			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

**electrical characteristics at specified virtual junction temperature, $V_I = 17\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$
(unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		μA78M10Y			UNIT
			MIN	TYP	MAX	
Output voltage			10			V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 12.5\text{ V to }28\text{ V}$	7			mV
		$V_I = 14\text{ V to }28\text{ V}$	2			
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$,	$I_O = 300\text{ mA}$, $f = 120\text{ Hz}$	80			dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25			mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		64			μV
Dropout voltage			2			V
Bias current			4.7			mA
Short-circuit output current	$V_I = 35\text{ V}$		245			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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electrical characteristics at specified virtual junction temperature, $V_I = 19\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M12Y			UNIT
			MIN	TYP	MAX	
Output voltage			12			V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 14.5\text{ V to }30\text{ V}$	8			mV
		$V_I = 16\text{ V to }30\text{ V}$	2			
Ripple rejection	$V_I = 15\text{ V to }25\text{ V}$,	$I_O = 300\text{ mA}$, $f = 120\text{ Hz}$	80			dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25			mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		75			μV
Dropout voltage			2			V
Bias current			4.8			mA
Short-circuit output current	$V_I = 35\text{ V}$		240			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 23\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA78M15C			UNIT
			MIN	TYP	MAX	
Output voltage			15			V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 17.5\text{ V to }30\text{ V}$	10			mV
		$V_I = 20\text{ V to }30\text{ V}$	3			
Ripple rejection	$V_I = 18.5\text{ V to }28.5\text{ V}$,	$I_O = 300\text{ mA}$, $f = 120\text{ Hz}$	70			dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		25			mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		90			μV
Dropout voltage			2			V
Bias current			4.8			mA
Short-circuit output current	$V_I = 35\text{ V}$		240			mA
Peak output current			0.7			A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

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electrical characteristics at specified virtual junction temperature, $V_I = 29\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78M20C			UNIT
		MIN	TYP	MAX	
Output voltage			20		V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 23\text{ V to }35\text{ V}$	10		mV
		$V_I = 24\text{ V to }35\text{ V}$	5		
Ripple rejection	$V_I = 24\text{ V to }34\text{ V}$, $f = 120\text{ Hz}$, $I_O = 300\text{ mA}$		70		dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		30		mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1.1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		110		μV
Dropout voltage			2		V
Bias current			4.9		mA
Short-circuit output current	$V_I = 35\text{ V}$		240		mA
Peak output current			0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified virtual junction temperature, $V_I = 33\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA78M24Y			UNIT
		MIN	TYP	MAX	
Output voltage			24		V
Input voltage regulation	$I_O = 200\text{ mA}$	$V_I = 27\text{ V to }38\text{ V}$	10		mV
		$V_I = 28\text{ V to }38\text{ V}$	5		
Ripple rejection	$V_I = 28\text{ V to }38\text{ V}$, $I_O = 300\text{ mA}$, $f = 120\text{ Hz}$		70		dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		30		mV
	$I_O = 5\text{ mA to }200\text{ mA}$		10		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1.2		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		170		μV
Dropout voltage			2		V
Bias current			5		mA
Short-circuit output current	$V_I = 35\text{ V}$		240		mA
Peak output current			0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.



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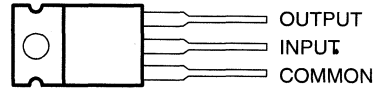
- 3-Terminal Regulators
- Output Current up to 500 mA
- No External Components
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μA79M00 Series

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement the μA78M00 series in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators delivers up to 500 mA of output current. The internal current-limiting and thermal-shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also as the power-pass element in precision regulators.

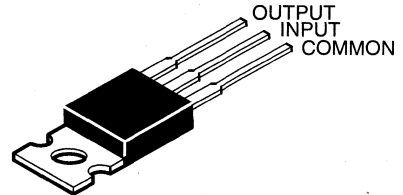
The μA79M00C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

**KC PACKAGE
(TOP VIEW)**

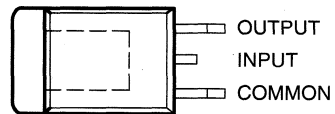


The INPUT terminal is in electrical contact with the mounting base.

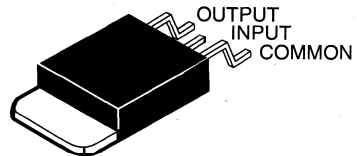
TO-220AB



**KTP PACKAGE
(TOP VIEW)**



The INPUT terminal is in electrical contact with the mounting base.



AVAILABLE OPTIONS

T _J	V _{O(NOM)} (V)	PACKAGED DEVICES		CHIP FORM (Y)
		HEAT-SINK MOUNTED (KC)	PLASTIC FLANGE MOUNTED (KTP)	
0°C to 125°C	-5	μA79M05CKC	μA79M05CKTP	μA79M05Y
	-6	μA79M06CKC	μA79M06CKTP	μA79M06Y
	-8	μA79M08CKC	μA79M08CKTP	μA79M08Y
	-12	μA79M12CKC	μA79M12CKTP	μA79M12Y
	-15	μA79M15CKC	μA79M15CKTP	μA79M15Y
	-20	μA79M20CKC	μA79M20CKTP	μA79M20Y
	-24	μA79M24CKC	μA79M24CKTP	μA79M24Y

The KTP package also is available in tape and reel. Add the suffix R to device type (e.g., μA79M05CKTPR). Chip forms are tested at 25°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


**TEXAS
INSTRUMENTS**

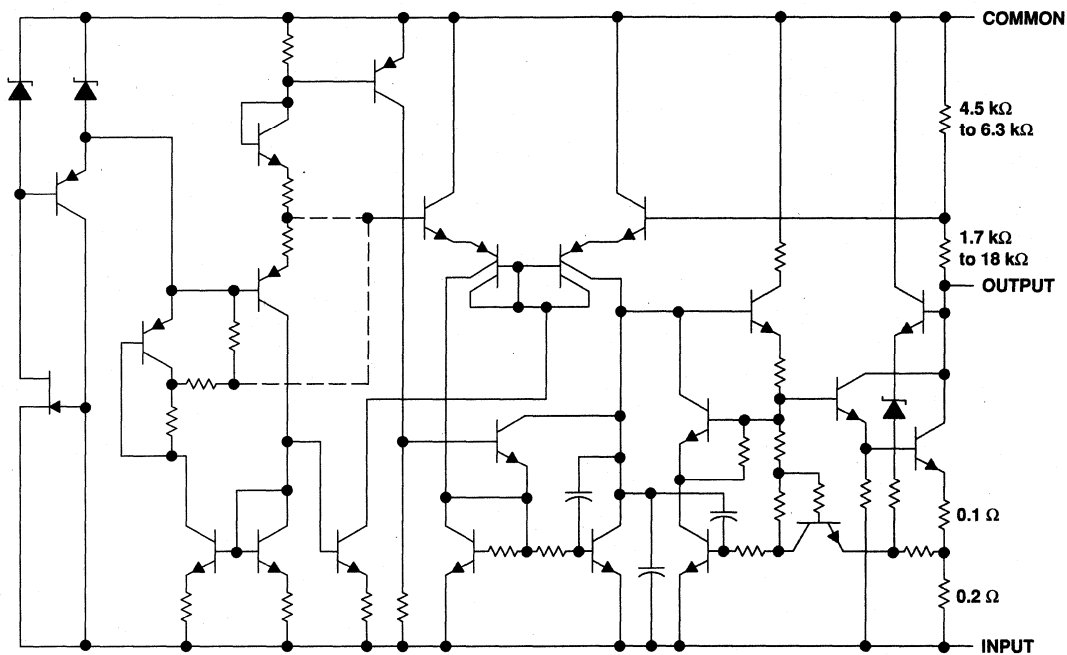
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μ A79M00 SERIES NEGATIVE-VOLTAGE REGULATORS

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schematic



Resistor values shown are nominal.

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absolute maximum ratings over operating temperature range (unless otherwise noted)†

		μA79MxxC	UNIT
Input voltage	μA79M20C, μA79M24C	-40	V
	All others	-35	
Package thermal impedance, θ_{JA} (see Notes 1 and 2)	KC package	22	°C
	KTP package	28	
Operating free-air, T_A ; case, T_C ; or virtual junction, T_J , temperature range		0 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range, T_{stg}		-65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	μA79M05C	-7	-25	V
	μA79M06C	-8	-25	
	μA79M08C	-10.5	-25	
	μA79M12C	-14.5	30	
	μA79M15C	-17.5	-30	
	μA79M20C	-23	-35	
	μA79M24C	-27	-38	
Output current, I_O		500		mA
Operating virtual junction temperature, T_J		0	125	°C



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electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M05C			UNIT	
		MIN	TYP	MAX		
Output voltage	$V_I = -7$ V to -25 V, $I_O = 5$ mA to 350 mA		-4.8	-5	-5.2	V
		$T_J = 0^\circ\text{C}$ to 125°C	-4.75		-5.25	
Input voltage regulation	$V_I = -7$ V to -25 V		7	50	mV	
	$V_I = -8$ V to -18 V		3	30		
Ripple rejection	$V_I = -8$ V to -18 V, $f = 120$ Hz	$I_O = 100$ mA, $T_J = 0^\circ\text{C}$ to 125°C	50		dB	
		$I_O = 300$ mA	54	60		
Output voltage regulation	$I_O = 5$ mA to 500 mA		75	100	mV	
	$I_O = 5$ mA to 350 mA		50			
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ\text{C}$ to 125°C		-0.4		mV/°C	
Output noise voltage	$f = 10$ Hz to 100 kHz		125		μV	
Dropout voltage			1.1		V	
Bias current			1	2	mA	
Bias current change	$V_I = -8$ V to -18 V, $T_J = 0^\circ\text{C}$ to 125°C			0.4	mA	
	$I_O = 5$ mA to 350 mA, $T_J = 0^\circ\text{C}$ to 125°C			0.4		
Short-circuit output current	$V_I = -30$ V		140		mA	
Peak output current			0.65		A	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M06C			UNIT	
		MIN	TYP	MAX		
Output voltage	$V_I = -8$ V to -25 V, $I_O = 5$ mA to 350 mA		-5.75	-6	-6.25	V
		$T_J = 0^\circ\text{C}$ to 125°C	-5.7		-6.3	
Input voltage regulation	$V_I = -8$ V to -25 V		7	60	mV	
	$V_I = -9$ V to -19 V		3	40		
Ripple rejection	$V_I = -9$ V to -19 V, $f = 120$ Hz	$I_O = 100$ mA, $T_J = 0^\circ\text{C}$ to 125°C	50		dB	
		$I_O = 300$ mA	54	60		
Output voltage regulation	$I_O = 5$ mA to 500 mA		80	120	mV	
	$I_O = 5$ mA to 350 mA		55			
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ\text{C}$ to 125°C		-0.4		mV/°C	
Output noise voltage	$f = 10$ Hz to 100 kHz		150		μV	
Dropout voltage			1.1		V	
Bias current			1	2	mA	
Bias current change	$V_I = -9$ V to -25 V, $T_J = 0^\circ\text{C}$ to 125°C			0.4	mA	
	$I_O = 5$ mA to 350 mA, $T_J = 0^\circ\text{C}$ to 125°C			0.4		
Short-circuit output current	$V_I = -30$ V		140		mA	
Peak output current			0.65		A	

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = -19\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA79M08C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = -10.5\text{ V to }-25\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	-7.7	-8	-8.3	V
			-7.6		-8.4	
Input voltage regulation	$V_I = -10.5\text{ V to }-25\text{ V}$		8			mV
	$V_I = -11\text{ V to }-21\text{ V}$		4			
Ripple rejection	$V_I = -11.5\text{ V to }-21.5\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $I_O = 300\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$			dB
			50	54	59	
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		90			mV
	$I_O = 5\text{ mA to }350\text{ mA}$		160			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		60			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		-0.6			mV/°C
Dropout voltage	$I_O = 5\text{ mA}$		200			μV
Bias current			1.1			V
Bias current change	$V_I = -10.5\text{ V to }-25\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		1			mA
			2			
Short-circuit output current	$V_I = -30\text{ V}$		140			mA
Peak output current			0.65			A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -19\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		μA79M12C			UNIT
			MIN	TYP	MAX	
Output voltage	$V_I = -14.5\text{ V to }-30\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	-11.5	-12	-12.5	V
			-11.4		-12.6	
Input voltage regulation	$V_I = -14.5\text{ V to }-30\text{ V}$		9			mV
	$V_I = -15\text{ V to }-25\text{ V}$		80			
Ripple rejection	$V_I = -15\text{ V to }-25\text{ V}$, $f = 120\text{ Hz}$	$I_O = 100\text{ mA}$, $I_O = 300\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$			dB
			50	54	60	
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		65			mV
	$I_O = 5\text{ mA to }350\text{ mA}$		240			
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		45			mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		-0.8			mV/°C
Dropout voltage			300			μV
Bias current			1.1			V
Bias current change	$V_I = -14.5\text{ V to }-30\text{ V}$, $I_O = 5\text{ mA to }350\text{ mA}$, $T_J = 0^\circ\text{C to }125^\circ\text{C}$		1.5			mA
			3			
Short-circuit output current	$V_I = -30\text{ V}$		140			mA
Peak output current			0.65			A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M15C			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = -17.5$ V to -30 V, $I_O = 5$ mA to 350 mA $T_J = 0^\circ\text{C}$ to 125°C	-14.4	-15	-15.6	V
Input voltage regulation	$V_I = -17.5$ V to -30 V		9	80	mV
	$V_I = -18$ V to -28 V		7	50	
Ripple rejection	$V_I = -18.5$ V to -28.5 V, $f = 120$ Hz, $I_O = 100$ mA, $T_J = 0^\circ\text{C}$ to 125°C		50		dB
	$I_O = 300$ mA		54	59	
Output voltage regulation	$I_O = 5$ mA to 500 mA		65	240	mV
	$I_O = 5$ mA to 350 mA		45		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ\text{C}$ to 125°C		-1		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		375		μV
Dropout voltage	$I_O = 5$ mA		1.1		V
Bias current			1.5	3	mA
Bias current change	$V_I = -17.5$ V to -30 V, $T_J = 0^\circ\text{C}$ to 125°C			0.4	mA
	$I_O = 5$ mA to 350 mA, $T_J = 0^\circ\text{C}$ to 125°C			0.4	
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -29$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M20C			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = -23$ V to -35 V, $I_O = 5$ mA to 350 mA $T_J = 0^\circ\text{C}$ to 125°C	-19.2	-20	-20.8	V
Input voltage regulation	$V_I = -23$ V to -35 V		12	80	mV
	$V_I = -24$ V to -34 V		10	70	
Ripple rejection	$V_I = -24$ V to -34 V, $f = 120$ Hz, $I_O = 100$ mA, $T_J = 0^\circ\text{C}$ to 125°C		50		dB
	$I_O = 300$ mA		54	58	
Output voltage regulation	$I_O = 5$ mA to 500 mA		75	300	mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ\text{C}$ to 125°C		-1		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		500		μV
Dropout voltage			1.1		V
Bias current			1.5	3.5	mA
Bias current change	$V_I = -23$ V to -35 V, $T_J = 0^\circ\text{C}$ to 125°C			0.4	mA
	$I_O = 5$ mA to 350 mA, $T_J = 0^\circ\text{C}$ to 125°C			0.4	
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA, $T_J = 25^\circ$ C (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M24C			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = -27$ V to -38 V, $I_O = 5$ mA to 350 mA $T_J = 0^\circ$ C to 125° C	-23	-24	-25	V
		-22.8		-25.2	
Input voltage regulation	$V_I = -27$ V to -38 V		12	80	mV
	$V_I = -28$ V to -38 V		12	70	
Ripple rejection	$V_I = -28$ V to -38 V, $f = 120$ Hz $I_O = 100$ mA, $T_J = 0^\circ$ C to 125° C $I_O = 300$ mA	50			dB
		54	58		
Output voltage regulation	$I_O = 5$ mA to 500 mA		75	300	mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ$ C to 125° C		-1		mV/ $^\circ$ C
Output noise voltage	$f = 10$ Hz to 100 kHz		600		μV
Dropout voltage			1.1		V
Bias current			1.5	3.5	mA
Bias current change	$V_I = -27$ V to -38 V, $T_J = 0^\circ$ C to 125° C			0.4	mA
	$I_O = 5$ mA to 350 mA; $T_J = 0^\circ$ C to 125° C			0.4	
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA, $T_J = 25^\circ$ C (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M05Y			UNIT
		MIN	TYP	MAX	
Output voltage			-5		V
Input voltage regulation	$V_I = -7$ V to -25 V		7		mV
	$V_I = -8$ V to -18 V		3		
Ripple rejection	$V_I = -8$ V to -18 V, $I_O = 300$ mA, $f = 120$ Hz		60		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA		-0.4		mV/ $^\circ$ C
Output noise voltage	$f = 10$ Hz to 100 kHz		125		μV
Dropout voltage			1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

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electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 350$ mA, $T_J = 25^\circ$ C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M06Y			UNIT
		MIN	TYP	MAX	
Output voltage			-6		V
Input voltage regulation	$V_I = -8$ V to -25 V		7		mV
	$V_I = -9$ V to -19 V		3		
Ripple rejection	$V_I = -9$ V to -19 V, $I_O = 300$ mA, $f = 120$ Hz		60		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		80		mV
	$I_O = 5$ mA to 350 mA		55		
Temperature coefficient of output voltage	$I_O = 5$ mA		-0.4		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		150		μV
Dropout voltage			1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA, $T_J = 25^\circ$ C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	μA79M08Y			UNIT
		MIN	TYP	MAX	
Output voltage			-8		V
Input voltage regulation	$V_I = -10.5$ V to -25 V		8		mV
	$V_I = -11$ V to -21 V		4		
Ripple rejection	$V_I = -11.5$ V to -21.5 V, $I_O = 300$ mA, $f = 120$ Hz		59		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		90		mV
	$I_O = 5$ mA to 350 mA		60		
Temperature coefficient of output voltage	$I_O = 5$ mA		-0.6		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		200		μV
Dropout voltage	$I_O = 5$ mA		1.1		V
Bias current			1		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.



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electrical characteristics at specified virtual junction temperature, $V_I = -19\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M12Y			UNIT
		MIN	TYP	MAX	
Output voltage			-12		V
Input voltage regulation	$V_I = -14.5\text{ V to }-30\text{ V}$		9		mV
	$V_I = -15\text{ V to }-25\text{ V}$		5		
Ripple rejection	$V_I = -15\text{ V to }-25\text{ V}$, $I_O = 300\text{ mA}$, $f = 120\text{ Hz}$		60		dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		65		mV
	$I_O = 5\text{ mA to }350\text{ mA}$		45		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		300		μV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30\text{ V}$		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -23\text{ V}$, $I_O = 350\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M15Y			UNIT
		MIN	TYP	MAX	
Output voltage			-15		V
Input voltage regulation	$V_I = -17.5\text{ V to }-30\text{ V}$		9		mV
	$V_I = -18\text{ V to }-28\text{ V}$		7		
Ripple rejection	$V_I = -18.5\text{ V to }-28.5\text{ V}$, $I_O = 300\text{ mA}$, $f = 120\text{ Hz}$		59		dB
Output voltage regulation	$I_O = 5\text{ mA to }500\text{ mA}$		65		mV
	$I_O = 5\text{ mA to }350\text{ mA}$		45		
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		375		μV
Dropout voltage	$I_O = 5\text{ mA}$		1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30\text{ V}$		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

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electrical characteristics at specified virtual junction temperature, $V_I = -29$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M20Y			UNIT
		MIN	TYP	MAX	
Output voltage			-20		V
Input voltage regulation	$V_I = -23$ V to -35 V		12		mV
	$V_I = -24$ V to -34 V		10		
Ripple rejection	$V_I = -24$ V to -34 V, $I_O = 300$ mA, $f = 120$ Hz		58		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA		-1		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		500		μV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	μA79M24Y			UNIT
		MIN	TYP	MAX	
Output voltage			-24		V
Input voltage regulation	$V_I = -27$ V to -38 V		12		mV
	$V_I = -28$ V to -38 V		12		
Ripple rejection	$V_I = -28$ V to -38 V, $I_O = 300$ mA, $f = 120$ Hz		58		dB
Output voltage regulation	$I_O = 5$ mA to 500 mA		75		mV
	$I_O = 5$ mA to 350 mA		50		
Temperature coefficient of output voltage	$I_O = 5$ mA, $T_J = 0^\circ\text{C}$ to 125°C		-1		mV/°C
Output noise voltage	$f = 10$ Hz to 100 kHz		600		μV
Dropout voltage			1.1		V
Bias current			1.5		mA
Short-circuit output current	$V_I = -30$ V		140		mA
Peak output current			0.65		A

† Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.



TL-SCSI285
FIXED-VOLTAGE REGULATORS
FOR SCSI ACTIVE TERMINATION
 SLVS065F – NOVEMBER 1991 – REVISED JULY 1999

- Fully Matches Parameters for SCSI Alternative 2 Active Termination
- Fixed 2.85-V Output
- ±1% Maximum Output Tolerance at $T_J = 25^\circ\text{C}$
- 0.7-V Maximum Dropout Voltage
- 620-mA Output Current
- ±2% Absolute Output Variation
- Internal Overcurrent-Limiting Circuitry
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

description

The TL-SCSI285 is a low-dropout (0.7-V) fixed-voltage regulator specifically designed for small computer systems interface (SCSI) alternative 2 active signal termination. The TL-SCSI285 0.7-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the ±1% initial tolerance on its 2.85-V output voltage ensures a tighter line-driver current tolerance, thereby increasing the system noise margin.

The fixed 2.85-V output voltage of the TL-SCSI285 supports the SCSI alternative 2 termination standard, while reducing system power consumption. The 0.7-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL-SCSI285, with internal current limiting, overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

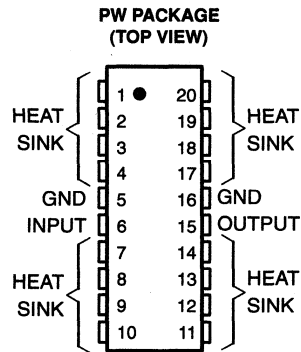
When configured as a SCSI active terminator, the TL-SCSI285 low-dropout regulator eliminates the 220-Ω and the 330-Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with 110-Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

The TL-SCSI285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

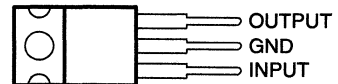
T_J	PACKAGED DEVICES		CHIP FORM (Y)
	PLASTIC POWER (KC)	SURFACE MOUNT (PW)	
0°C to 125°C	TL-SCSI285KC	TL-SCSI285PWR	TL-SCSI285Y

The PW package is only available taped and reeled. Chip forms are tested at 25°C.



HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE (TOP VIEW)



The GND terminal is in electrical contact with the mounting base.

TL-SCSI285 FIXED-VOLTAGE REGULATORS FOR SCSI ACTIVE TERMINATION

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absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I	7.5 V
Operating virtual junction temperature range, T_J	-55°C to 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): KC package	22°C/W
PW package	83°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: KC or PW package	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		TL-SCSI285		UNIT
		MIN	MAX	
Input voltage, V_I	$T_J = 25^\circ\text{C}$			V
Input voltage, V_I	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	3.55	5.5	V
Output current, I_O	KC package	0	620	mA
	PW package	0	500	
Operating virtual junction temperature range, T_J		0	125	°C

electrical characteristics, $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TL-SCSI285KC			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 20\text{ mA to } 500\text{ mA}$, $V_I = 3.55\text{ V to } 5.5\text{ V}$, $T_J = 25^\circ\text{C}$	2.82	2.85	2.88	V
	$I_O = 500\text{ mA to } 620\text{ mA}$, $V_I = 3.65\text{ V to } 5.5\text{ V}$, $T_J = 0\text{ to } 125^\circ\text{C}$	2.79		2.91	
Input regulation	$V_I = 3.55\text{ V to } 5.5\text{ V}$		5	15	mV
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_O(\text{PP})$		-62		dB
Output regulation	$I_O = 20\text{ mA to } 620\text{ mA}$		5	30	mV
	$I_O = 20\text{ mA to } 500\text{ mA}$		5	30	
Output noise voltage	$f = 10\text{ Hz to } 100\text{ kHz}$		500		µV
Dropout voltage	$I_O = 500\text{ mA}$			0.7	V
	$I_O = 620\text{ mA}$			0.8	
Bias current	$I_O = 0$		2	5	mA
	$I_O = 27\text{ mA}$, equivalent 1 line asserted		3	6	
	$I_O = 500\text{ mA}$, equivalent 18 lines asserted (8-bit)		26	49	
	$I_O = 620\text{ mA}$		37	62	

‡ Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22.0-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



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electrical characteristics, $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST	TL-SCSI285PW			UNIT	
		MIN	TYP	MAX		
Output voltage	$I_O = 20\text{ mA to }500\text{ mA}$, $V_I = 3.55\text{ V to }5.5\text{ V}$	$T_J = 25^\circ\text{C}$	2.82	2.85	2.88	V
		$T_J = 0\text{ to }125^\circ\text{C}$	2.79		2.91	
Input regulation	$V_I = 3.55\text{ V to }5.5\text{ V}$		5	15	mV	
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_O(\text{PP})$		-62		dB	
Output regulation	$I_O = 20\text{ mA to }500\text{ mA}$		5	30	mV	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		500		μV	
Dropout voltage	$I_O = 500\text{ mA}$			0.7	V	
Bias current	$I_O = 0$		2	5	mA	
	$I_O = 27\text{ mA}$, equivalent 1 line asserted		3	6		
	$I_O = 500\text{ mA}$, equivalent 18 lines asserted (8-bit)		26	49		

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $22.0\text{-}\mu\text{F}$ tantalum capacitor with equivalent series resistance of $1.5\ \Omega$ on the output.

electrical characteristics, $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONST	TL-SCSI285Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 20\text{ mA to }500\text{ mA}$, $V_I = 3.55\text{ V to }5.5\text{ V}$		2.85		V
Input regulation	$V_I = 3.55\text{ V to }5.5\text{ V}$		5		mV
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_O(\text{PP})$		-62		dB
Output regulation	$I_O = 20\text{ mA to }620\text{ mA}$		5		mV
	$I_O = 20\text{ mA to }500\text{ mA}$		5		
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		500		μV
Bias current	$I_O = 0$		2		mA
	$I_O = 27\text{ mA}$, equivalent 1 line asserted		3		
	$I_O = 500\text{ mA}$, equivalent 18 lines asserted (8-bit)		26		
	$I_O = 620\text{ mA}$		37		

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a $0.1\text{-}\mu\text{F}$ capacitor across the input and a $22.0\text{-}\mu\text{F}$ tantalum capacitor with equivalent series resistance of $1.5\ \Omega$ on the output.

TL-SCSI285
FIXED-VOLTAGE REGULATORS
FOR SCSI ACTIVE TERMINATION
 SLVS065F – NOVEMBER 1991 – REVISED JULY 1999

APPLICATION INFORMATION

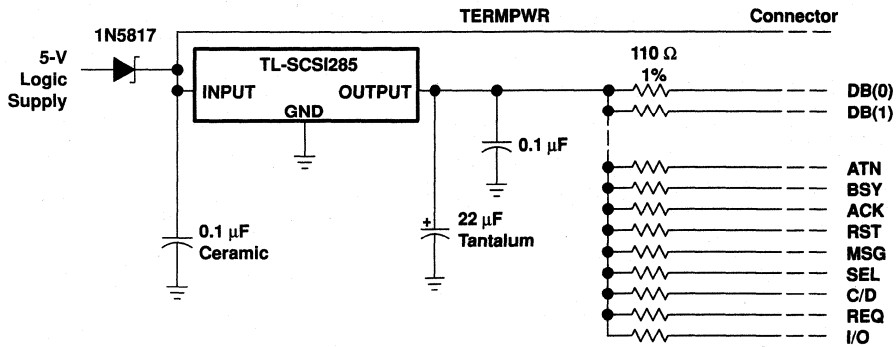


Figure 1. Typical Application Schematic

COMPENSATION CAPACITOR SELECTION INFORMATION

The TL-SCSI285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 2 and 3 can be used to establish the capacitance value and ESR range for best regulator performance.

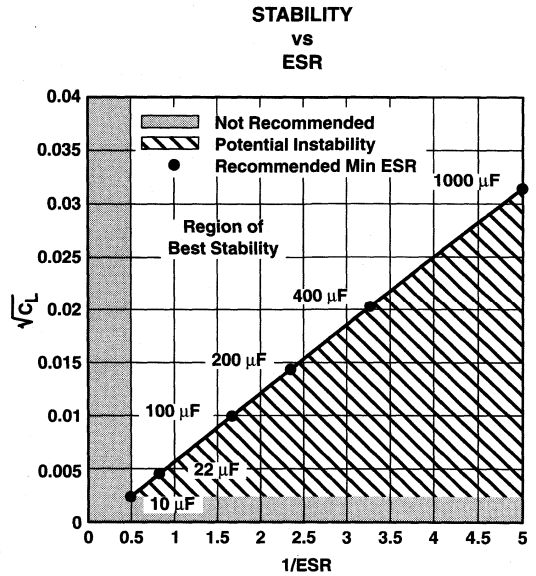
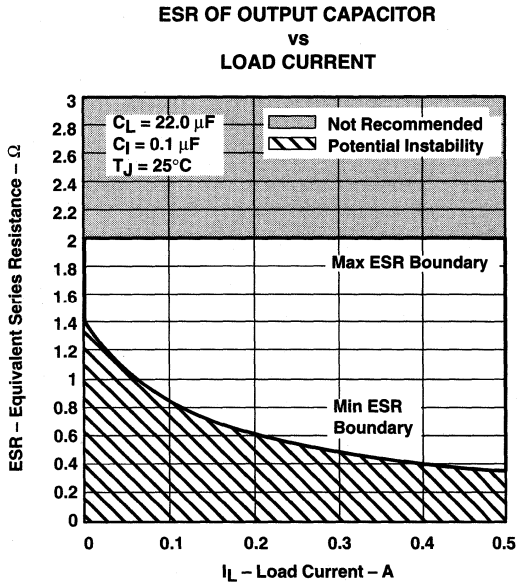


Figure 3

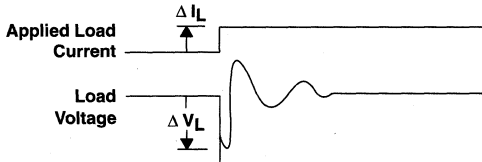


Figure 2

TL2217-285 FIXED-VOLTAGE REGULATORS FOR SCSI ACTIVE TERMINATION

SLVS066F – NOVEMBER 1991 – REVISED JULY 1999

- Fully Matches Parameters for SCSI Alternative 2 Active Termination
- Fixed 2.85-V Output
- $\pm 1.5\%$ Maximum Output Tolerance at $T_J = 25^\circ\text{C}$
- 1-V Maximum Dropout Voltage
- 500-mA Output Current
- $\pm 3\%$ Absolute Output Variation
- Internal Overcurrent-Limiting Circuitry
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

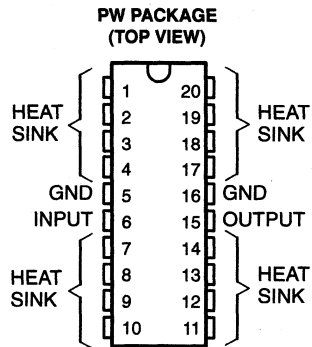
description

The TL2217-285 is a low-dropout (1 V) fixed-voltage regulator specifically designed for small computer systems interface (SCSI) alternative 2 active signal termination. The TL2217-285 1-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the $\pm 1.5\%$ initial tolerance on its 2.85-V output voltage ensures a tighter line-driver current tolerance, thereby increasing system noise margin.

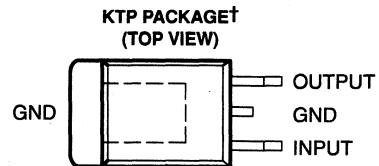
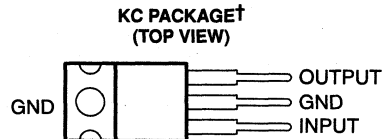
The fixed 2.85-V output voltage of TL2217-285 supports the SCSI alternative 2 termination standard, while reducing system power consumption. The 1-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL2217-285, with internal current limiting, overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

When configured as a SCSI active terminator, the TL2217-285 low-dropout regulator eliminates the 220- Ω and 330- Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system-power drain. When placed in series with 110- Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

The TL2217-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C .



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded or electrically isolated.



† The GND terminal is in electrical contact with the mounting base.

TL2217-285
FIXED-VOLTAGE REGULATORS
FOR SCSI ACTIVE TERMINATION

SLVS066F – NOVEMBER 1991 – REVISED JULY 1999

AVAILABLE OPTIONS

T _J	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC POWER (KC)	PLASTIC FLANGE MOUNT (KTP)	SURFACE MOUNT (PW)	
0°C to 125°C	TL2217-285KC	TL2217-285KTP	TL2217-285PWR	TL2217-285Y

The KTP and PW packages are only available taped and reeled. Add the suffix R to the device type (e.g., TL2217-285KTPR). Chip forms are tested at 25°C.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V _I	7.5 V
Operating virtual junction temperature range, T _J	-55°C to 150°C
Package thermal impedance, θ _{JA} (see Notes 1 and 2): KC package	22°C/W
..... KTP package	28°C/W
..... PW package	83°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	260°C
Storage temperature range, T _{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V _I	3.85	5.5	V
Output current, I _O	0	500	mA
Operating virtual junction temperature range, T _J	TL2217-285		°C



TL2217-285
FIXED-VOLTAGE REGULATORS
FOR SCSI ACTIVE TERMINATION
 SLVS066F – NOVEMBER 1991 – REVISED JULY 1999

electrical characteristics over recommended operating conditions, $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST	TL2217-285			UNIT	
		MIN	TYP	MAX		
Output voltage	$I_O = 20\text{ mA to }500\text{ mA}$, $V_I = 3.85\text{ V to }5.5\text{ V}$	$T_J = 25^\circ\text{C}$	2.81	2.85	2.89	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	2.765		2.935	
Input voltage regulation	$V_I = 3.85\text{ V to }5.5\text{ V}$		5	15	mV	
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_{\text{PP}}$		-62		dB	
Output voltage regulation	$I_O = 20\text{ mA to }500\text{ mA}$		5	30	mV	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		500		μV	
Dropout voltage				1*	V	
Bias current	$I_O = 0$		2	5	mA	
	$I_O = 27\text{ mA}$, equivalent 1 line asserted		3	6		
	$I_O = 500\text{ mA}$, equivalent 18 lines asserted (8 bit)		26	49		

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 22- μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

electrical characteristics over recommended operating conditions, $V_I = 4.5\text{ V}$, $I_O = 500\text{ mA}$, $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONST	TL2217-285Y			UNIT
		MIN	TYP	MAX	
Output voltage	$I_O = 20\text{ mA to }500\text{ mA}$, $V_I = 3.85\text{ V to }5.5\text{ V}$	2.81	2.85	2.89	V
Input voltage regulation	$V_I = 3.85\text{ V to }5.5\text{ V}$		5	15	mV
Ripple rejection	$f = 120\text{ Hz}$, $V_{\text{ripple}} = 1\text{ V}_{\text{PP}}$		-62		dB
Output voltage regulation	$I_O = 20\text{ mA to }500\text{ mA}$		5	30	mV
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$		500		μV
Dropout voltage	$I_O = 500\text{ mA}$			1	V
Bias current	$I_O = 0$		2	5	mA
	$I_O = 27\text{ mA}$, equivalent 1 line asserted		3	6	
	$I_O = 500\text{ mA}$, equivalent 18 lines asserted (8 bit)		26	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μF capacitor across the input and a 22- μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



TL2217-285
FIXED-VOLTAGE REGULATORS
FOR SCSI ACTIVE TERMINATION

SLVS066F – NOVEMBER 1991 – REVISED JULY 1999

COMPENSATION-CAPACITOR SELECTION INFORMATION

The TL2217-285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figure 3 and Figure 4 can be used to establish the capacitance value and ESR range for best regulator performance.

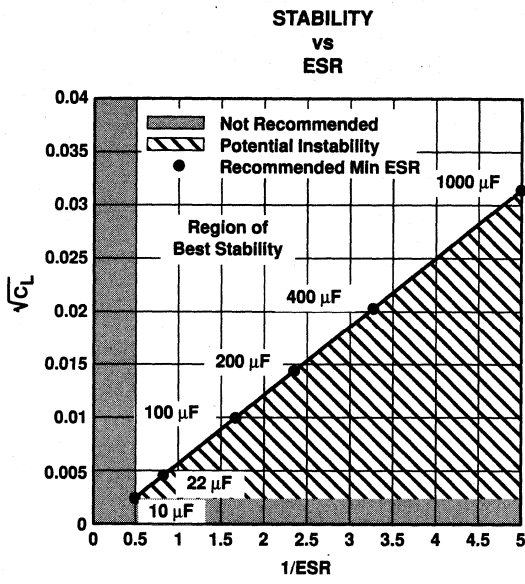
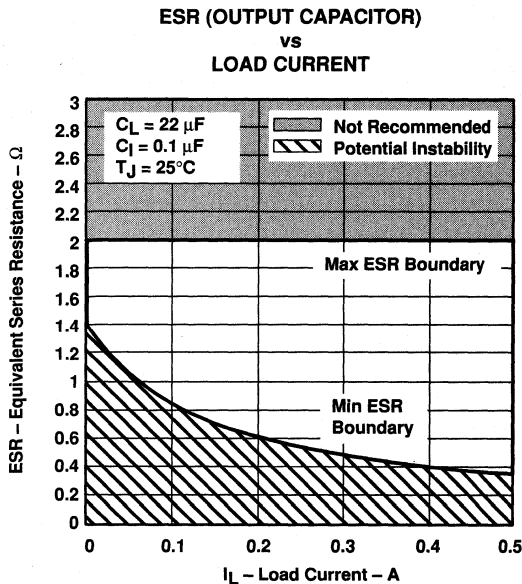


Figure 2

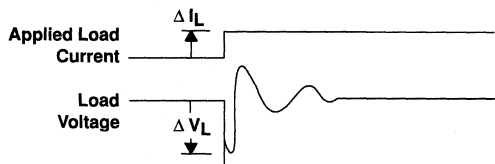


Figure 1

APPLICATION INFORMATION

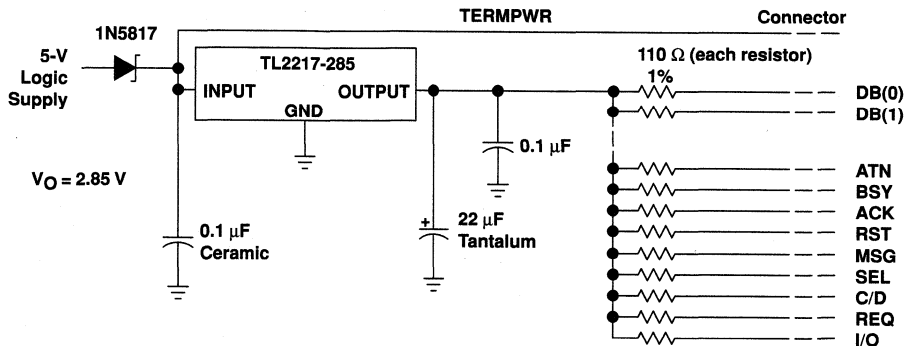


Figure 3. Typical Application Schematic

General Information (Vol. 1)	1
Linear Voltage Regulators	2
Shunt Regulators	3
Precision Virtual Grounds	4
Mechanical Data	5
General Information (Vol. 2)	6
Processor PS Controllers	7
Switching PS and DC/DC Converters	8
MOSFET Drivers	9
Supervisors	10
Mechanical Data	11
General Information (Vol. 3)	12
Power Distribution Switches	13
LED Drivers	14
Voltage Rail Splitters	15
Special Functions	16
Mechanical Data	17



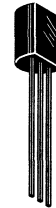
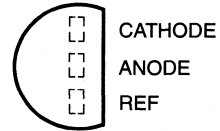
Shunt Regulators

TL430 ADJUSTABLE SHUNT REGULATORS

SLVS050B – JUNE 1976 – REVISED JULY 1999

- Temperature Compensated
- Programmable Output Voltage
- Low Output Resistance
- Low Output Noise
- Sink Capability up to 100 mA

LP PACKAGE
(TOP VIEW)

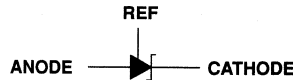


description

The TL430 is a 3-terminal adjustable shunt regulator, featuring excellent temperature stability, wide operating current range, and low output noise. The output voltage can be set by two external resistors to any desired value between 3 V and 30 V. The TL430 can replace zener diodes in many applications, providing improved performance.

The TL430C is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T _A	PACKAGED DEVICES	
	PLASTIC (LP)	CHIP FORM (Y)
0°C to 70°C	TL430CLP	TL430Y

The LP package is available taped and reeled. Add R suffix to device type (e.g., TL430CLPR). Chip forms are tested at 25°C.

TL430 ADJUSTABLE SHUNT REGULATORS

SLVS050B – JUNE 1976 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Regulator voltage (see Note 1)	30 V
Continuous regulator current	150 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	156°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the anode terminal.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Regulator voltage, V_Z	V_{ref}	30	V
Regulator current, I_Z	2	100	mA
Operating free-air temperature range, T_A	TL430C		0 70 °C

electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	TL430C			UNIT
			MIN	TYP	MAX	
$V_{I(ref)}$ Reference input voltage	1	$V_Z = V_{I(ref)}$, $I_Z = 10\text{ mA}$	2.5	2.75	3	V
$\alpha V_{I(ref)}$ Temperature coefficient of reference input voltage	1	$V_Z = V_{I(ref)}$, $I_Z = 10\text{ mA}$, $T_A = 0^\circ\text{C}$ to 70°C	120			ppm/°C
$I_{I(ref)}$ Reference input current	2	$I_Z = 10\text{ mA}$, $R_1 = 10\text{ k}\Omega$, $R_2 = \infty$	3	10		μA
I_{ZK} Regulator current near lower knee of regulation range	1	$V_Z = V_{I(ref)}$	0.5		2	mA
I_{ZK} Regulator current at maximum limit of regulation range	1	$V_Z = V_{I(ref)}$	50			mA
	2	$V_Z = 5\text{ V}$ to 30 V , See Note 4	100			
r_z Differential regulator resistance (see Note 5)	1	$V_Z = V_{I(ref)}$, $\Delta I_Z = (52 - 2)\text{ mA}$	1.5		3	W
V_n Noise voltage	2	$f = 0.1\text{ Hz}$ to 10 Hz	$V_Z = 3\text{ V}$	50		μV
			$V_Z = 12\text{ V}$	200		
			$V_Z = 30\text{ V}$	650		

- NOTES: 4. The average power dissipation, $V_Z \cdot I_Z \cdot \text{duty cycle}$, must not exceed the maximum continuous rating in any 10-ms interval.
 5. The regulator resistance for $V_Z > V_{I(ref)}$, r_z , is given by:

$$r_z' = r_z \left(1 + \frac{R_1}{R_2} \right)$$

TL430 ADJUSTABLE SHUNT REGULATORS

SLVS050B – JUNE 1976 – REVISED JULY 1999

electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	TL430Y			UNIT
			MIN	TYP	MAX	
$V_{I(\text{ref})}$ Reference input voltage	1	$V_Z = V_{I(\text{ref})}$, $I_Z = 10 \text{ mA}$	2.5	2.75	3	V
$I_{I(\text{ref})}$ Reference input current	2	$I_Z = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, $R_2 = \infty$		3	10	μA
I_{ZK} Regulator current near lower knee of regulation range	1	$V_Z = V_{I(\text{ref})}$		0.5	2	mA
I_{ZK} Regulator current at maximum limit of regulation range	1	$V_Z = V_{I(\text{ref})}$		50		mA
	2	$V_Z = 5 \text{ V to } 30 \text{ V}$, See Note 4		100		
r_z Differential regulator resistance (see Note 5)	1	$V_Z = V_{I(\text{ref})}$, ... $\Delta I_Z = (52 - 2) \text{ mA}$		1.5	3	W
V_n Noise voltage	2	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$	$V_Z = 3 \text{ V}$		50	μV
			$V_Z = 12 \text{ V}$		200	
			$V_Z = 30 \text{ V}$		650	

NOTES: 4. The average power dissipation, $V_Z \cdot I_Z \cdot \text{duty cycle}$, must not exceed the maximum continuous rating in any 10-ms interval.
5. The regulator resistance for $V_Z > V_{I(\text{ref})}$, r_z , is given by:

$$r_z' = r_z \left(1 + \frac{R_1}{R_2} \right)$$

PARAMETER MEASUREMENT INFORMATION

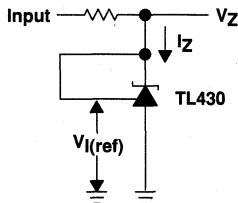
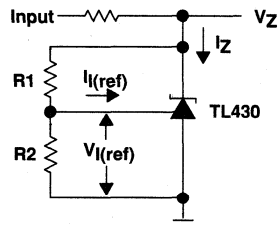


Figure 1. Test Circuit for $V_Z = V_{I(\text{ref})}$



$$V_Z = V_{I(\text{ref})} \left(1 + \frac{R_1}{R_2} \right) + I_{I(\text{ref})} \times R_1$$

Figure 2. Test Circuit for $V_Z > V_{I(\text{ref})}$

TL430 ADJUSTABLE SHUNT REGULATORS

SLVS050B – JUNE 1976 – REVISED JULY 1999

TYPICAL CHARACTERISTICS

SMALL-SIGNAL REGULATOR IMPEDANCE
vs
FREQUENCY

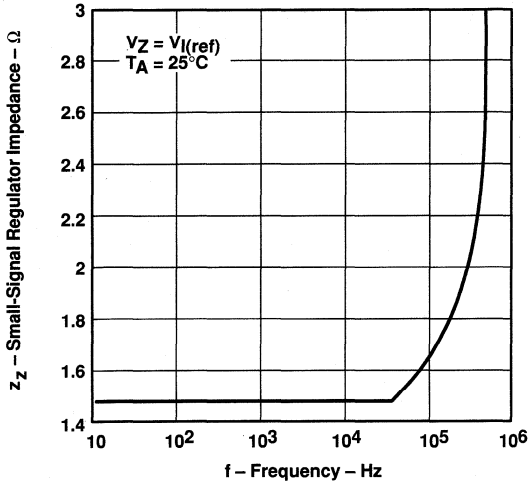


Figure 3

CATHODE CURRENT
vs
CATHODE VOLTAGE

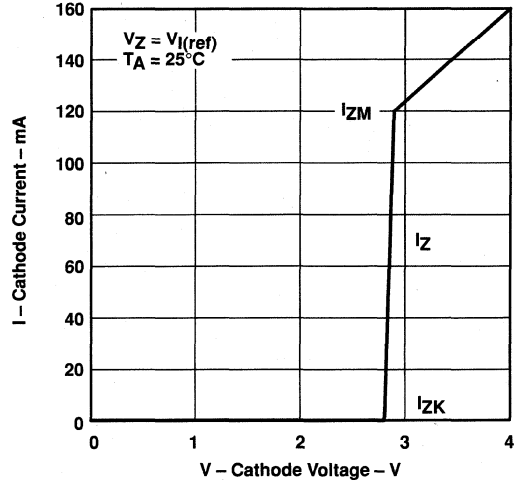
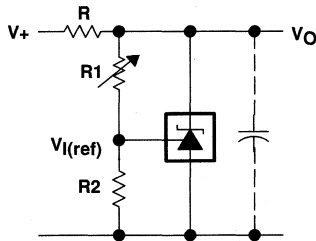


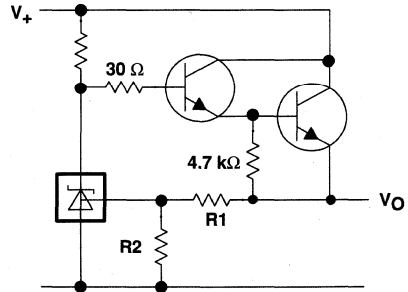
Figure 4

APPLICATION INFORMATION



$$V_O \approx \left(1 + \frac{R_1}{R_2}\right) V_{I(ref)}$$

Figure 5. Shunt Regulator



$$V_O \approx \left(1 + \frac{R_1}{R_2}\right) V_{I(ref)}$$

Figure 6. Series Regulator

APPLICATION INFORMATION

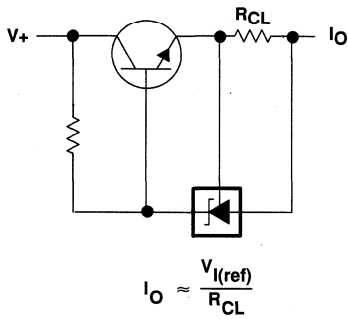


Figure 7. Current Limiter

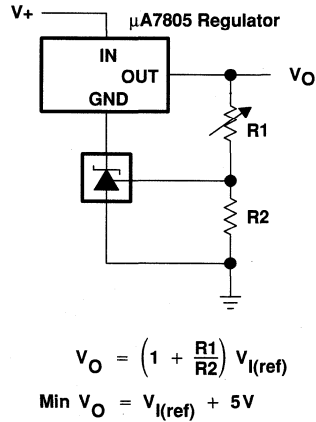


Figure 8. Output Control of a 3-Terminal Fixed Regulator

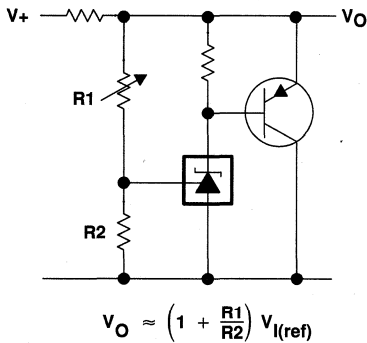


Figure 9. Higher-Current Applications

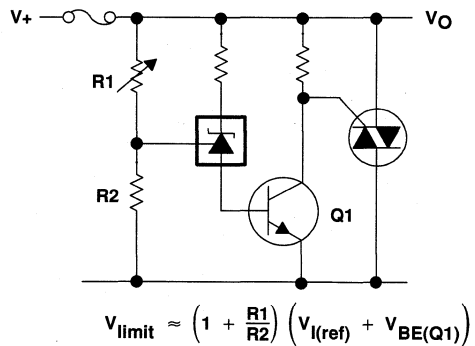


Figure 10. Crowbar

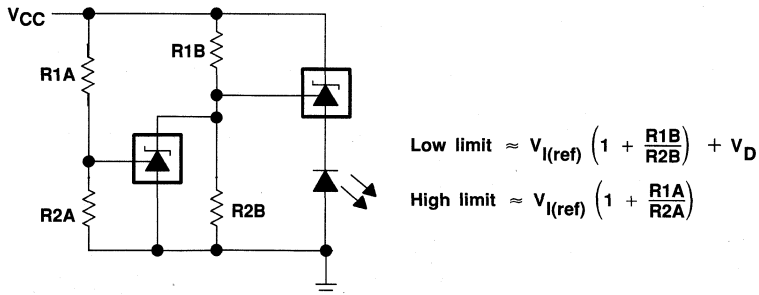


Figure 11. V_{CC} Monitor

TL431, TL431A ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS005J – JULY 1978 – REVISED JULY 1999

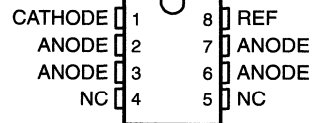
- Equivalent Full-Range Temperature Coefficient . . . 30 ppm/°C
- 0.2-Ω Typical Output Impedance
- Sink-Current Capability . . . 1 mA to 100 mA
- Low Output Noise
- Adjustable Output Voltage . . . V_{ref} to 36 V
- Available in a Wide Range of High-Density Packages

description

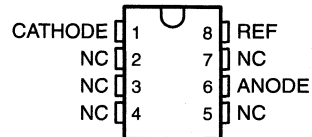
The TL431 and TL431A are three-terminal adjustable shunt regulators with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{ref} (approximately 2.5 V) and 36 V with two external resistors (see Figure 17). These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

The TL431C and TL431AC are characterized for operation from 0°C to 70°C, and the TL431I and TL431AI are characterized for operation from -40°C to 85°C.

**D PACKAGE
(TOP VIEW)**

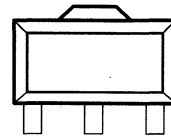


**P OR PW PACKAGE
(TOP VIEW)**



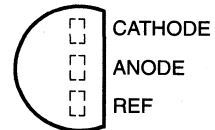
NC – No internal connection

**PK PACKAGE
(TOP VIEW)**

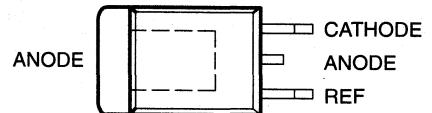


REF ANODE CATHODE

**LP PACKAGE
(TOP VIEW)**



**KTP PACKAGE
(TOP VIEW)**



TL431, TL431A ADJUSTABLE PRECISION SHUNT REGULATORS

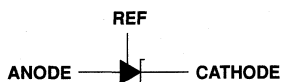
SLVS005J – JULY 1978 – REVISED JULY 1999

AVAILABLE OPTIONS

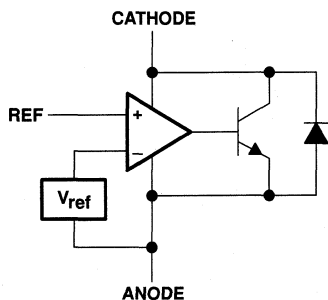
T _A	PACKAGED DEVICES						CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC FLANGE MOUNT (KTP)	TO-226AA (LP)	PLASTIC DIP (P)	SOT-89 (PK)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL431CD TL431ACD	TL431CKTPR	TL431CLP TL431ACL P	TL431CP TL431ACP	TL431CPK	TL431CPW	TL431Y
-40°C to 85°C	TL431ID TL431AID		TL431ILP TL431AILP	TL431IP TL431AIP	TL431IPK		

The D and LP packages are available taped and reeled. The KTP and PK packages are only available taped and reeled. Add the suffix R to device type (e.g., TL431CDR). Chip forms are tested at T_A = 25°C.

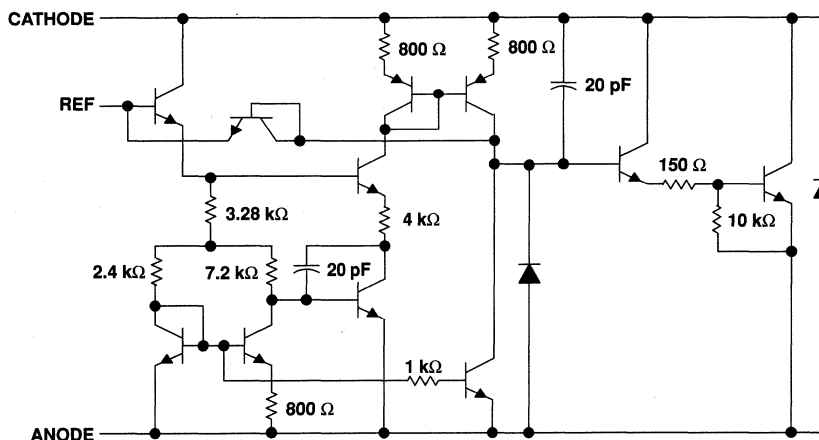
symbol



functional block diagram



equivalent schematic†



† All component values are nominal.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TL431, TL431A

ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS005J – JULY 1978 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cathode voltage, V_{KA} (see Note 1)	37 V
Continuous cathode current range, I_{KA}	–100 mA to 150 mA
Reference input current range	–50 μ A to 10 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	
D package	97°C/W
LP package	156°C/W
KTP package	28°C/W
P package	127°C/W
PK package	52°C/W
PW package	149°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: LP or PK package	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to the anode terminal unless otherwise noted.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	36	V
Cathode current, I_{KA}	1	100	mA
Operating free-air temperature range, T_A	TL431C, TL431AC	0	70
	TL431I, TL431AI	–40	85



TL431, TL431A ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS005J – JULY 1978 – REVISED JULY 1999

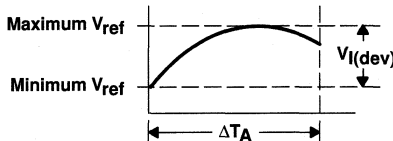
electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	TL431C			UNIT
			MIN	TYP	MAX	
V_{ref} Reference voltage	2	$V_{\text{KA}} = V_{\text{ref}}, I_{\text{KA}} = 10 \text{ mA}$	2440	2495	2550	mV
$V_{\text{I(dev)}}$ Deviation of reference voltage over full temperature range (see Figure 1)	2	$V_{\text{KA}} = V_{\text{ref}}, I_{\text{KA}} = 10 \text{ mA}, T_A = \text{full range}^\dagger$		4	25	mV
$\frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}}$ Ratio of change in reference voltage to the change in cathode voltage	3	$I_{\text{KA}} = 10 \text{ mA}$	$\Delta V_{\text{KA}} = 10 \text{ V} - V_{\text{ref}}$	-1.4	-2.7	$\frac{\text{mV}}{\text{V}}$
			$\Delta V_{\text{KA}} = 36 \text{ V} - 10 \text{ V}$	-1	-2	
I_{ref} Reference current	3	$I_{\text{KA}} = 10 \text{ mA}, R1 = 10 \text{ k}\Omega, R2 = \infty$		2	4	μA
$I_{\text{I(dev)}}$ Deviation of reference current over full temperature range (see Figure 1)	3	$I_{\text{KA}} = 10 \text{ mA}, R1 = 10 \text{ k}\Omega, R2 = \infty, T_A = \text{full range}^\dagger$		0.4	1.2	μA
I_{min} Minimum cathode current for regulation	2	$V_{\text{KA}} = V_{\text{ref}}$		0.4	1	mA
I_{off} Off-state cathode current	4	$V_{\text{KA}} = 36 \text{ V}, V_{\text{ref}} = 0$		0.1	1	μA
$ z_{\text{KA}} $ Dynamic impedance (see Figure 1)	1	$I_{\text{KA}} = 1 \text{ mA to } 100 \text{ mA}, V_{\text{KA}} = V_{\text{ref}}, f \leq 1 \text{ kHz}$		0.2	0.5	Ω

† Full range is 0°C to 70°C for the TL431C.

The deviation parameters $V_{\text{ref(dev)}}$ and $I_{\text{ref(dev)}}$ are defined as the differences between the maximum and minimum values obtained over the recommended temperature range. The average full-range temperature coefficient of the reference voltage, $\alpha_{V_{\text{ref}}}$, is defined as:

$$|\alpha_{V_{\text{ref}}}| \left(\frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left(\frac{V_{\text{I(dev)}}}{V_{\text{ref at } 25^\circ\text{C}}} \right) \times 10^6}{\Delta T_A}$$



where:

ΔT_A is the recommended operating free-air temperature range of the device.

$\alpha_{V_{\text{ref}}}$ can be positive or negative, depending on whether minimum V_{ref} or maximum V_{ref} , respectively, occurs at the lower temperature.

Example: maximum $V_{\text{ref}} = 2496 \text{ mV}$ at 30°C , minimum $V_{\text{ref}} = 2492 \text{ mV}$ at 0°C , $V_{\text{ref}} = 2495 \text{ mV}$ at 25°C , $\Delta T_A = 70^\circ\text{C}$ for TL431C

$$|\alpha_{V_{\text{ref}}}| = \frac{\left(\frac{4 \text{ mV}}{2495 \text{ mV}} \right) \times 10^6}{70^\circ\text{C}} \approx 23 \text{ ppm}/^\circ\text{C}$$

Because minimum V_{ref} occurs at the lower temperature, the coefficient is positive.

Calculating Dynamic Impedance

The dynamic impedance is defined as: $|z_{\text{KA}}| = \frac{\Delta V_{\text{KA}}}{\Delta I_{\text{KA}}}$

When the device is operating with two external resistors (see Figure 3), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I} \approx |z_{\text{KA}}| \left(1 + \frac{R1}{R2} \right)$$

Figure 1. Calculating Deviation Parameters and Dynamic Impedance



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electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	TL431			UNIT
			MIN	TYP	MAX	
V_{ref} Reference voltage	2	$V_{\text{KA}} = V_{\text{ref}}$, $I_{\text{KA}} = 10 \text{ mA}$	2440	2495	2550	mV
$V_{\text{I(dev)}}$ Deviation of reference voltage over full temperature range (see Figure 1)	2	$V_{\text{KA}} = V_{\text{ref}}$, $I_{\text{KA}} = 10 \text{ mA}$, $T_A = \text{full range}^\dagger$		5	50	mV
$\frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}}$ Ratio of change in reference voltage to the change in cathode voltage	3	$I_{\text{KA}} = 10 \text{ mA}$	$\Delta V_{\text{KA}} = 10 \text{ V} - V_{\text{ref}}$	-1.4	-2.7	$\frac{\text{mV}}{\text{V}}$
			$\Delta V_{\text{KA}} = 36 \text{ V} - 10 \text{ V}$	-1	-2	
I_{ref} Reference current	3	$I_{\text{KA}} = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, $R_2 = \infty$		2	4	μA
$I_{\text{I(dev)}}$ Deviation of reference current over full temperature range (see Figure 1)	3	$I_{\text{KA}} = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, $R_2 = \infty$, $T_A = \text{full range}^\dagger$		0.8	2.5	μA
I_{min} Minimum cathode current for regulation	2	$V_{\text{KA}} = V_{\text{ref}}$		0.4	1	mA
I_{off} Off-state cathode current	4	$V_{\text{KA}} = 36 \text{ V}$, $V_{\text{ref}} = 0$		0.1	1	μA
$ z_{\text{KA}} $ Dynamic impedance (see Figure 1)	2	$I_{\text{KA}} = 1 \text{ mA}$ to 100 mA , $V_{\text{KA}} = V_{\text{ref}}$, $f \leq 1 \text{ kHz}$		0.2	0.5	Ω

† Full range is -40°C to 85°C for the TL431.

electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	TL431AC			UNIT
			MIN	TYP	MAX	
V_{ref} Reference voltage	2	$V_{\text{KA}} = V_{\text{ref}}$, $I_{\text{KA}} = 10 \text{ mA}$	2470	2495	2520	mV
$V_{\text{I(dev)}}$ Deviation of reference voltage over full temperature range (see Figure 1)	2	$V_{\text{KA}} = V_{\text{ref}}$, $I_{\text{KA}} = 10 \text{ mA}$, $T_A = \text{full range}^\ddagger$		4	25	mV
$\frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}}$ Ratio of change in reference voltage to the change in cathode voltage	3	$I_{\text{KA}} = 10 \text{ mA}$	$\Delta V_{\text{KA}} = 10 \text{ V} - V_{\text{ref}}$	-1.4	-2.7	$\frac{\text{mV}}{\text{V}}$
			$\Delta V_{\text{KA}} = 36 \text{ V} - 10 \text{ V}$	-1	-2	
I_{ref} Reference current	3	$I_{\text{KA}} = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, $R_2 = \infty$		2	4	μA
$I_{\text{I(dev)}}$ Deviation of reference current over full temperature range (see Figure 1)	3	$I_{\text{KA}} = 10 \text{ mA}$, $R_1 = 10 \text{ k}\Omega$, $R_2 = \infty$, $T_A = \text{full range}^\ddagger$		0.8	1.2	μA
I_{min} Minimum cathode current for regulation	2	$V_{\text{KA}} = V_{\text{ref}}$		0.4	0.6	mA
I_{off} Off-state cathode current	4	$V_{\text{KA}} = 36 \text{ V}$, $V_{\text{ref}} = 0$		0.1	0.5	μA
$ z_{\text{KA}} $ Dynamic impedance (see Figure 1)	1	$I_{\text{KA}} = 1 \text{ mA}$ to 100 mA , $V_{\text{KA}} = V_{\text{ref}}$, $f \leq 1 \text{ kHz}$		0.2	0.5	Ω

‡ Full range is 0°C to 70°C for the TL431AC.

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electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	TL431AI			UNIT
			MIN	TYP	MAX	
V_{ref} Reference voltage	2	$V_{\text{KA}} = V_{\text{ref}}, I_{\text{KA}} = 10 \text{ mA}$	2470	2495	2520	mV
$V_{\text{I(dev)}}$ Deviation of reference voltage over full temperature range (see Figure 1)	2	$V_{\text{KA}} = V_{\text{ref}}, I_{\text{KA}} = 10 \text{ mA}, T_A = \text{full range}^\dagger$		5	50	mV
$\frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}}$ Ratio of change in reference voltage to the change in cathode voltage	3	$I_{\text{KA}} = 10 \text{ mA}$		-1.4	-2.7	$\frac{\text{mV}}{\text{V}}$
		$\Delta V_{\text{KA}} = 10 \text{ V} - V_{\text{ref}}$				
		$\Delta V_{\text{KA}} = 36 \text{ V} - 10 \text{ V}$		-1	-2	$\frac{\text{mV}}{\text{V}}$
I_{ref} Reference current	3	$I_{\text{KA}} = 10 \text{ mA}, R_1 = 10 \text{ k}\Omega, R_2 = \infty$		2	4	μA
$I_{\text{I(dev)}}$ Deviation of reference current over full temperature range (see Figure 1)	3	$I_{\text{KA}} = 10 \text{ mA}, R_1 = 10 \text{ k}\Omega, R_2 = \infty, T_A = \text{full range}^\dagger$		0.8	2.5	μA
I_{min} Minimum cathode current for regulation	2	$V_{\text{KA}} = V_{\text{ref}}$		0.4	0.7	mA
I_{off} Off-state cathode current	4	$V_{\text{KA}} = 36 \text{ V}, V_{\text{ref}} = 0$		0.1	0.5	μA
$ z_{\text{KA}} $ Dynamic impedance (see Figure 1)	2	$I_{\text{KA}} = 1 \text{ mA to } 100 \text{ mA}, V_{\text{KA}} = V_{\text{ref}}, f \leq 1 \text{ kHz}$		0.2	0.5	Ω

† Full range is -40°C to 85°C for the TL431AI.

electrical characteristics over recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	TL431Y			UNIT
			MIN	TYP	MAX	
V_{ref} Reference voltage	2	$V_{\text{KA}} = V_{\text{ref}}, I_{\text{KA}} = 10 \text{ mA}$		2495		mV
$\frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}}$ Ratio of change in reference voltage to the change in cathode voltage	3	$I_{\text{KA}} = 10 \text{ mA}$		-1.4		$\frac{\text{mV}}{\text{V}}$
		$\Delta V_{\text{KA}} = 10 \text{ V} - V_{\text{ref}}$				
		$\Delta V_{\text{KA}} = 36 \text{ V} - 10 \text{ V}$		-1		$\frac{\text{mV}}{\text{V}}$
I_{ref} Reference input current	3	$I_{\text{KA}} = 10 \text{ mA}, R_1 = 10 \text{ k}\Omega, R_2 = \infty$		2		μA
I_{min} Minimum cathode current for regulation	2	$V_{\text{KA}} = V_{\text{ref}}$		0.4		mA
I_{off} Off-state cathode current	4	$V_{\text{KA}} = 36 \text{ V}, V_{\text{ref}} = 0$		0.1		μA
$ z_{\text{KA}} $ Dynamic impedance ‡	2	$I_{\text{KA}} = 1 \text{ mA to } 100 \text{ mA}, V_{\text{KA}} = V_{\text{ref}}, f \leq 1 \text{ kHz}$		0.2		Ω

‡ Calculating dynamic impedance:

The dynamic impedance is defined as: $|z_{\text{KA}}| = \frac{\Delta V_{\text{KA}}}{\Delta I_{\text{KA}}}$

When the device is operating with two external resistors (see Figure 3), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I} \approx |z_{\text{KA}}| \left(1 + \frac{R_1}{R_2} \right)$$



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PARAMETER MEASUREMENT INFORMATION

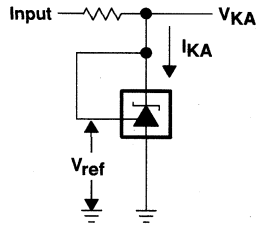


Figure 2. Test Circuit for $V_{KA} = V_{ref}$

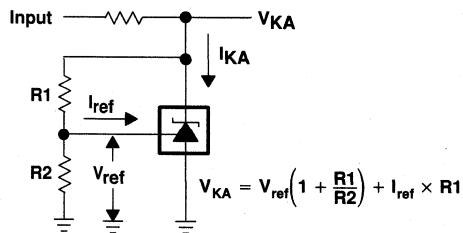


Figure 3. Test Circuit for $V_{KA} > V_{ref}$

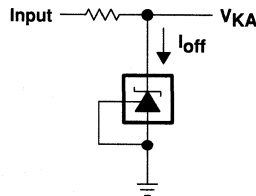


Figure 4. Test Circuit for I_{off}

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TYPICAL CHARACTERISTICS

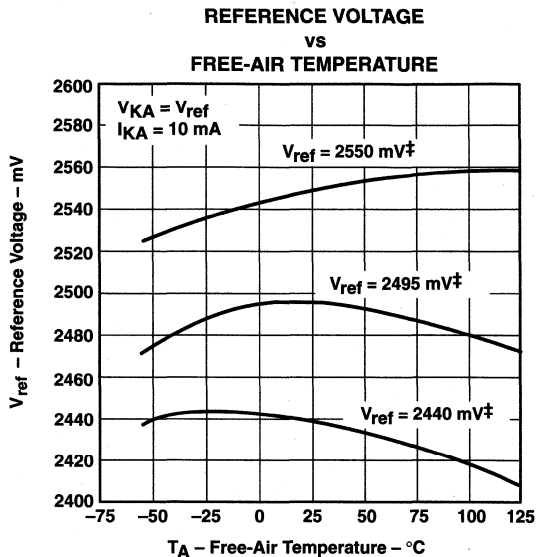
Table 1. Graphs

	FIGURE
Reference input voltage vs Free-air temperature	5
Reference input current vs Free-air temperature	6
Cathode current vs Cathode voltage	7, 8
Off-state cathode current vs Free-air temperature	9
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Equivalent input noise voltage vs Frequency	11
Equivalent input noise voltage over a 10-second period	12
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Table 2. Application Circuits

	FIGURE
Shunt regulator	17
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Precision 5-V 1.5-A regulator	23
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Voltage monitor	26
Delay timer	27
Precision current limiter	28
Precision constant-current sink	29

TYPICAL CHARACTERISTICS†



† Data is for devices having the indicated value of V_{ref} at $I_{KA} = 10 \text{ mA}$, $T_A = 25^\circ\text{C}$.

Figure 5

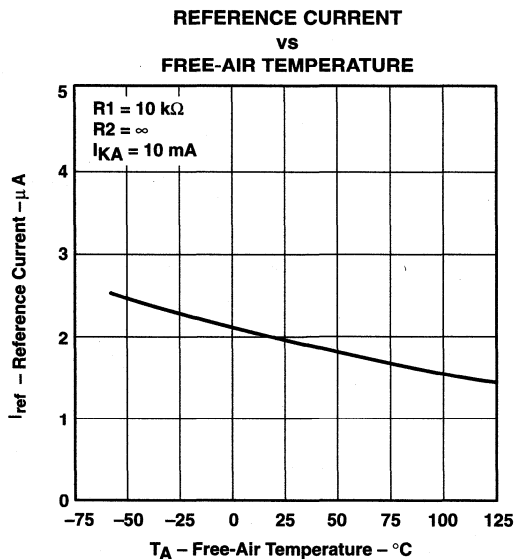


Figure 6

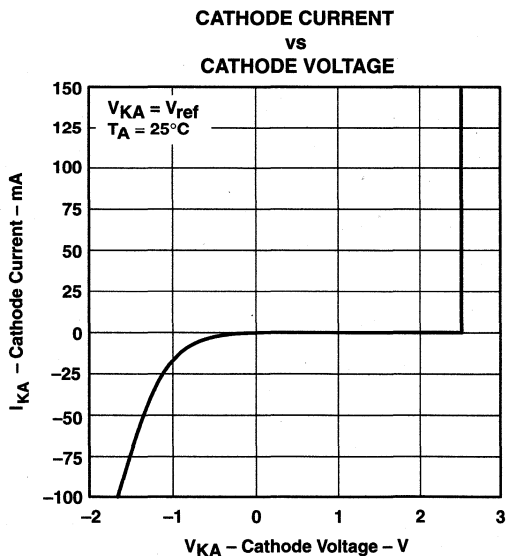


Figure 7

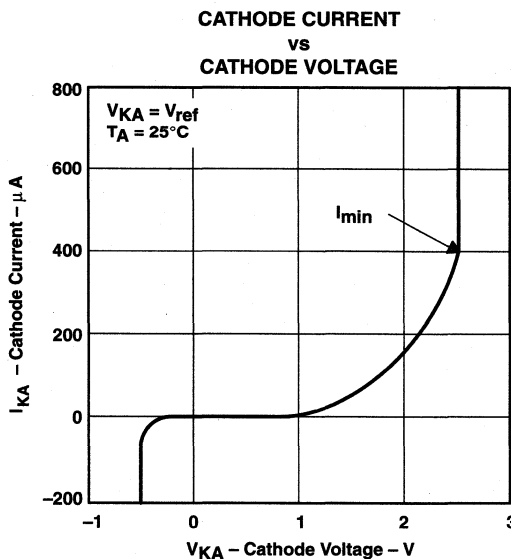


Figure 8

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

OFF-STATE CATHODE CURRENT
vs
FREE-AIR TEMPERATURE

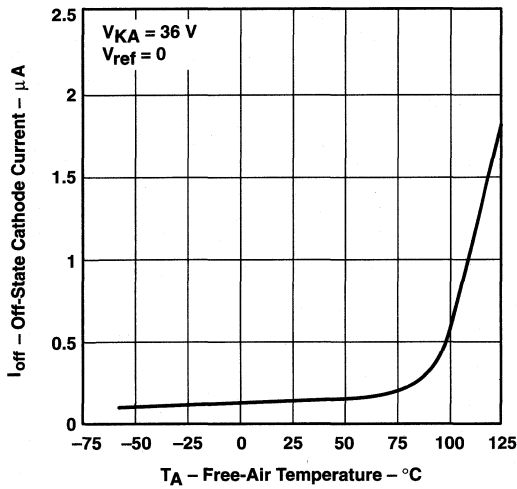


Figure 9

RATIO OF DELTA REFERENCE VOLTAGE TO
DELTA CATHODE VOLTAGE
vs
FREE-AIR TEMPERATURE

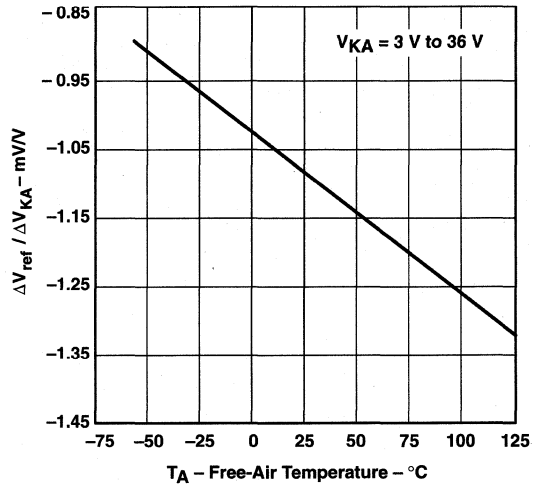


Figure 10

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

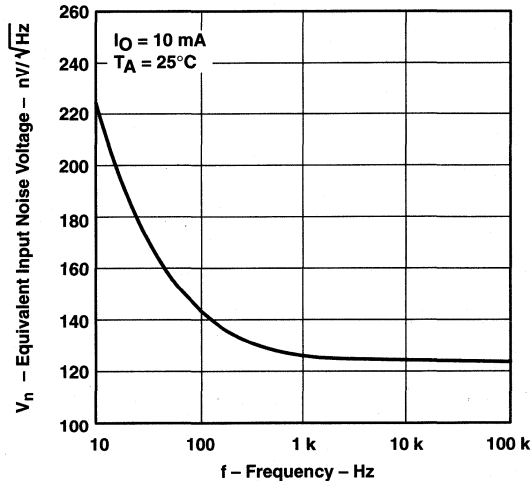


Figure 11

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
 OVER A 10-SECOND PERIOD

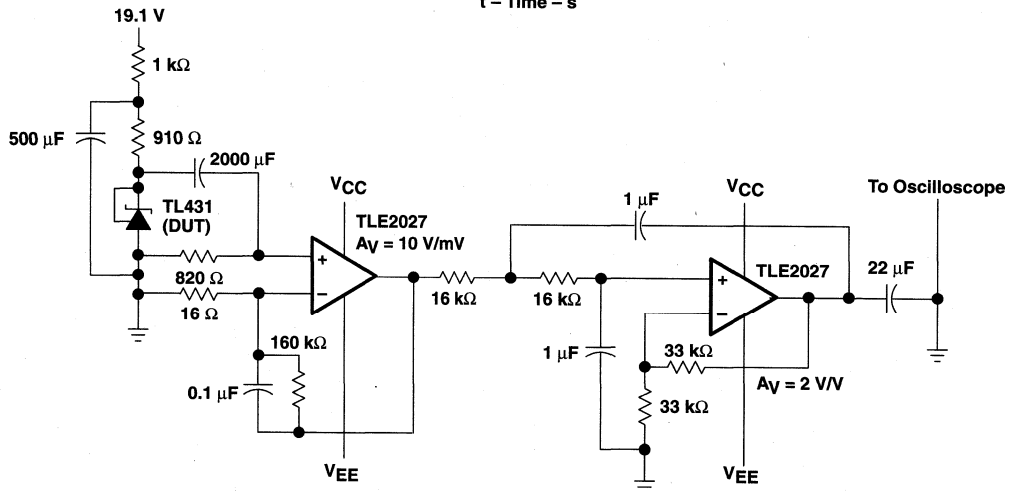
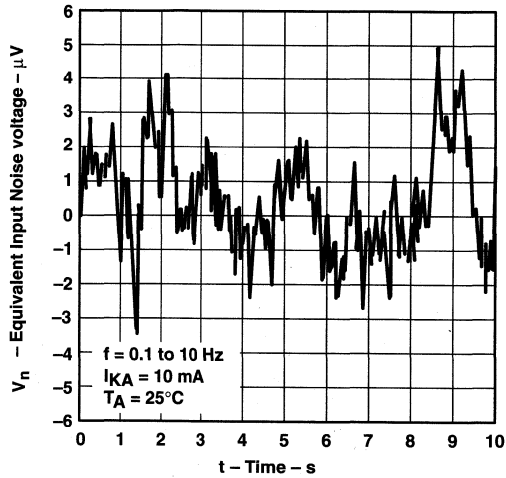
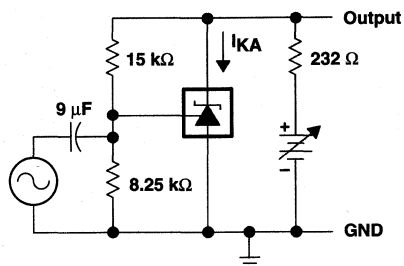
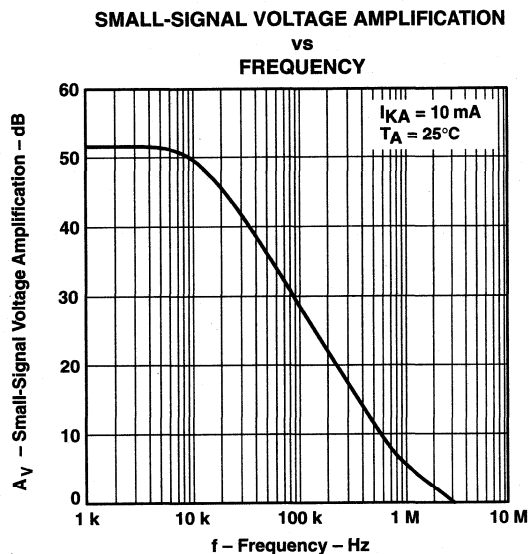


Figure 12. Test Circuit for Equivalent Input Noise Voltage

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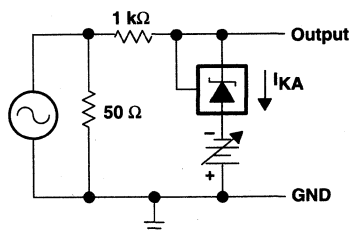
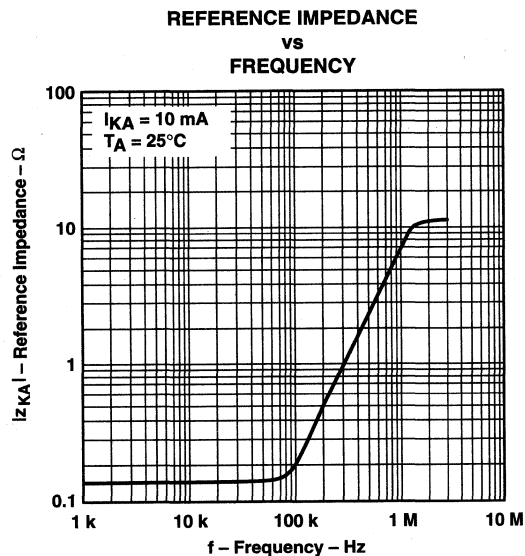
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TYPICAL CHARACTERISTICS



TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

Figure 13



TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 14

TYPICAL CHARACTERISTICS

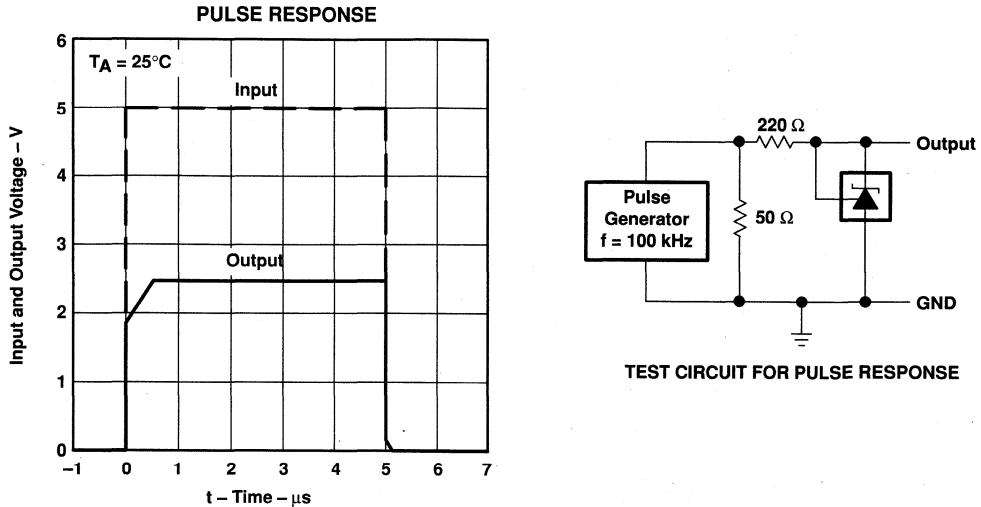


Figure 15

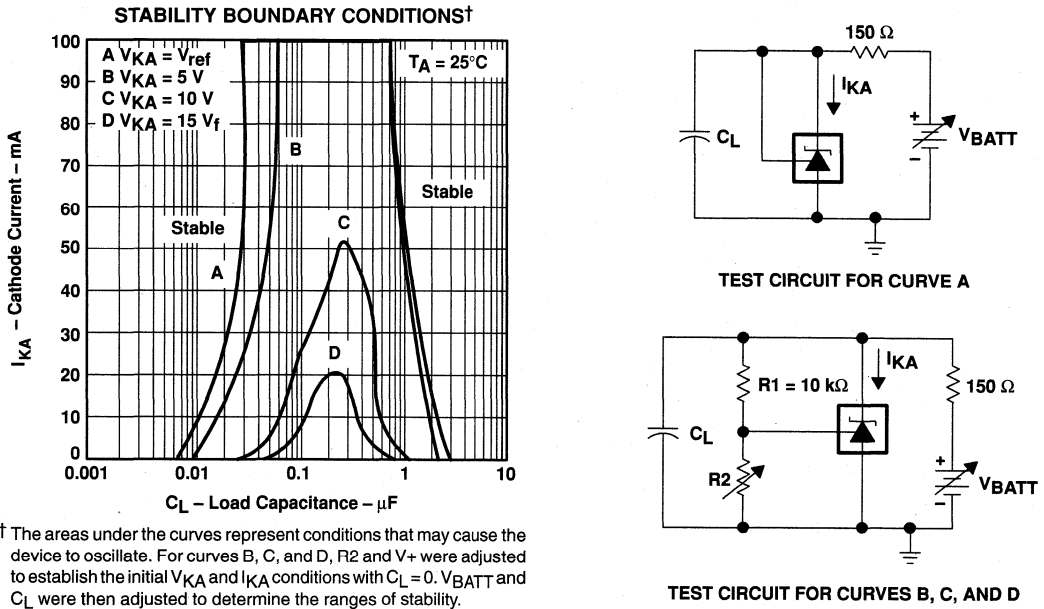
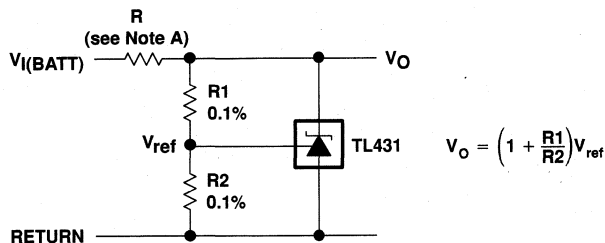


Figure 16

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APPLICATION INFORMATION



NOTE A. R should provide cathode current ≥ 1 mA to the TL431 at minimum $V_{I(BATT)}$.

Figure 17. Shunt Regulator

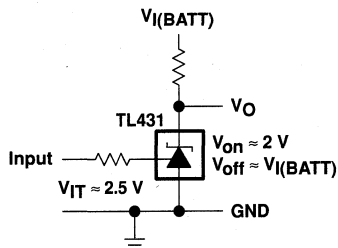
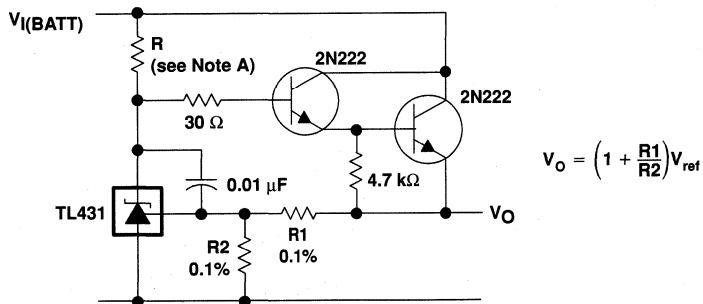


Figure 18. Single-Supply Comparator With Temperature-Compensated Threshold



NOTE A. R should provide cathode current ≥ 1 mA to the TL431 at minimum $V_{I(BATT)}$.

Figure 19. Precision High-Current Series Regulator

APPLICATION INFORMATION

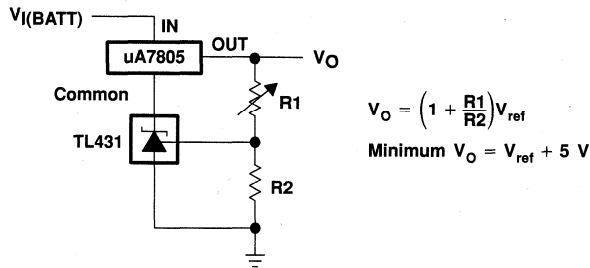


Figure 20. Output Control of a Three-Terminal Fixed Regulator

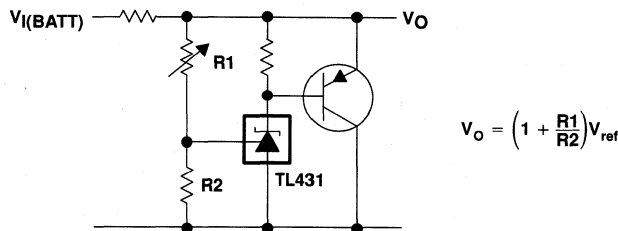
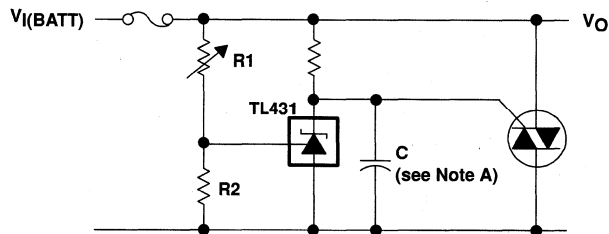


Figure 21. High-Current Shunt Regulator



NOTE A. Refer to the stability boundary conditions in Figure 16 to determine allowable values for C.

Figure 22. Crowbar Circuit

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APPLICATION INFORMATION

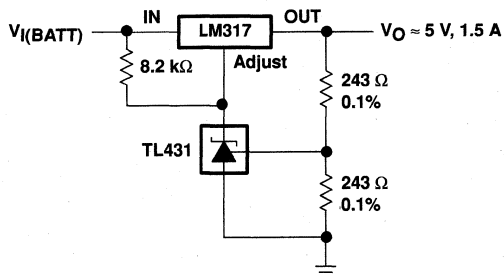
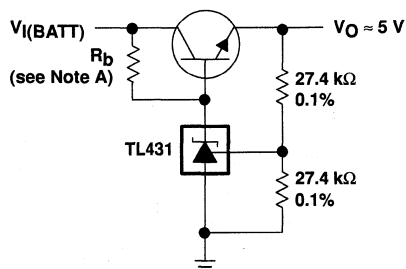


Figure 23. Precision 5-V 1.5-A Regulator



NOTE A. R_b should provide cathode current ≥ 1 -mA to the TL431.

Figure 24. Efficient 5-V Precision Regulator

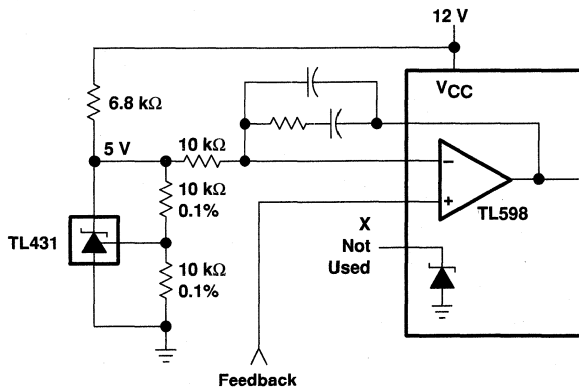
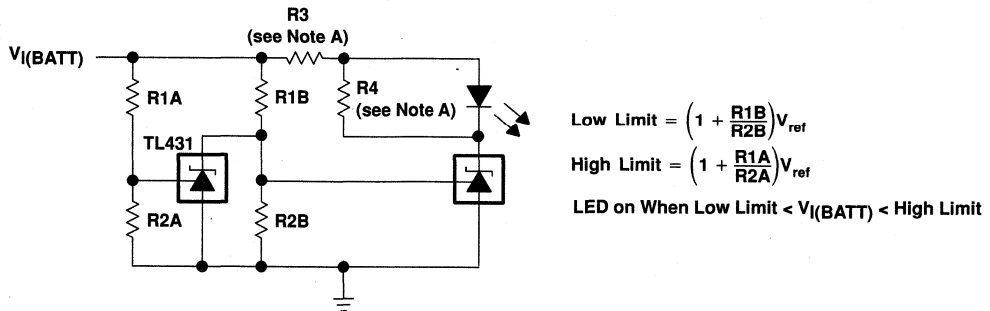


Figure 25. PWM Converter With Reference

APPLICATION INFORMATION



NOTE A. R3 and R4 are selected to provide the desired LED intensity and cathode current ≥ 1 mA to the TL431 at the available V_I(BATT).

Figure 26. Voltage Monitor

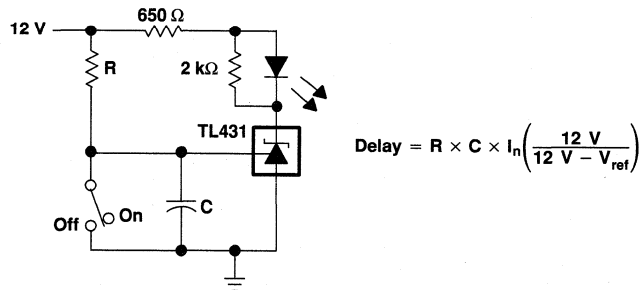


Figure 27. Delay Timer

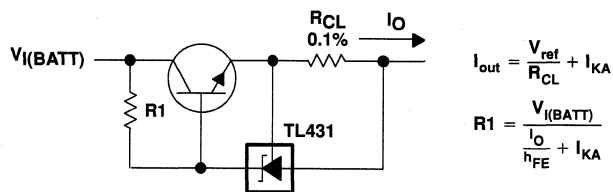


Figure 28. Precision Current Limiter

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APPLICATION INFORMATION

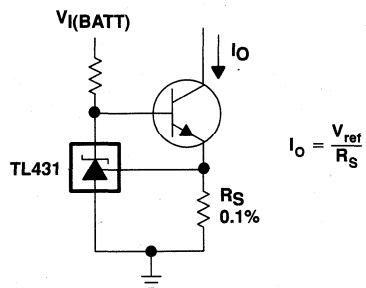


Figure 29. Precision Constant-Current Sink

TL1431 PRECISION PROGRAMMABLE REFERENCES

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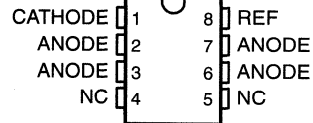
- 0.4% Initial Voltage Tolerance
- 0.2-Ω Typical Output Impedance
- Fast Turnon . . . 500 ns
- Sink Current Capability . . . 1 mA to 100 mA
- Low Reference Current (REF)
- Adjustable Output Voltage . . . $V_{I(ref)}$ to 36 V

description

The TL1431 is a precision programmable reference with specified thermal stability over applicable automotive and commercial temperature ranges. The output voltage can be set to any value between $V_{I(ref)}$ (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes and other types of references in applications such as on-board regulation, adjustable power supplies, and switching power supplies.

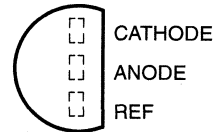
The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TL1431Q is characterized for operation over the automotive temperature range of -40°C to 125°C.

**D PACKAGE
(TOP VIEW)**

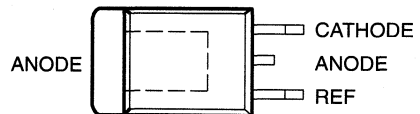


NC – No internal connection
ANODE terminals are connected internally.

**LP PACKAGE
(TOP VIEW)**



**KTP PACKAGE
(TOP VIEW)**



The ANODE terminal is in electrical contact with the mounting base.

AVAILABLE OPTIONS

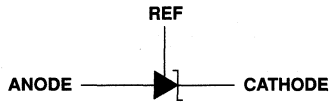
T _A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC FLANGE MOUNTED (KTP)	TO-226AA (LP)	
0°C to 70°C	TL1431CD	TL1431CKTPR	TL1431CLP	TL1431Y
-40°C to 125°C	TL1431QD	–	TL1431QLP	

The D and LP packages are available taped and reeled. The KTP package is only available tape and reeled. Add the suffix R to the device type (e.g., TL1431CDR). Chip forms are tested at 25°C.

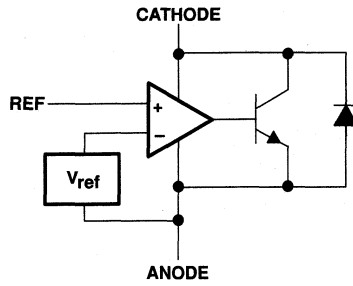
TL1431 PRECISION PROGRAMMABLE REFERENCES

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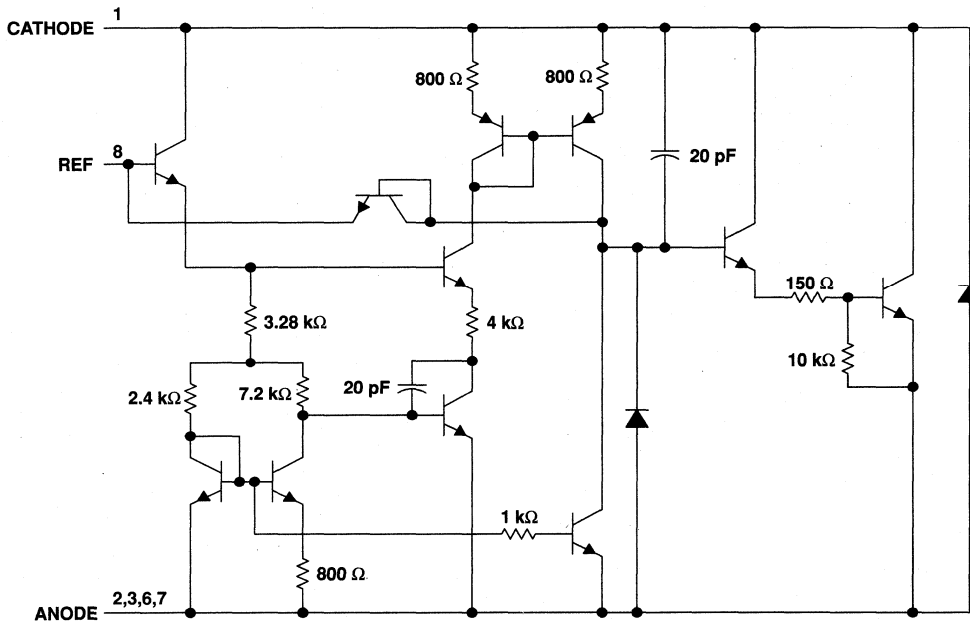
logic symbol



functional block diagram



equivalent schematic†



† All component values are nominal.
Pin numbers shown are for the D package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cathode voltage, V_{KA} (see Note 1)	37 V
Continuous cathode current range, I_{KA}	–100 mA to 150 mA
Reference input current range, $I_{I(ref)}$	–50 μ A to 10 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
KTP package	
LP package	
28°C/W	
156°C/W	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to ANODE unless otherwise noted.
 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Cathode voltage, V_{KA}		$V_{I(ref)}$	36	V
Cathode current, I_{KA}		1	100	mA
Operating free-air temperature, T_A	TL1431C	0	70	°C
	TL1431Q	–40	125	



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electrical characteristics at specified free-air temperature, $I_{KA} = 10 \text{ mA}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TEST CIRCUIT	TL1431C			TL1431Q			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(\text{ref})}$ Reference input voltage	$V_{KA} = V_{I(\text{ref})}$	25°C	1	2490	2500	2510	2490	2500	2510	mV
		Full range		2480		2520	2470		2530	
$V_{I(\text{dev})}$ Deviation of reference input voltage over full temperature range‡	$V_{KA} = V_{I(\text{ref})}$	Full range	1		4	20		17	55	mV
$\frac{\Delta V_{I(\text{ref})}}{\Delta V_{KA}}$ Ratio of change in reference input voltage to the change in cathode voltage	$\Delta V_{KA} = 3 \text{ V to } 36 \text{ V}$	Full range	2		-1.1	-2		-1.1	-2	mV/V
$I_{I(\text{ref})}$ Reference input current	$R1 = 10 \text{ k}\Omega, R2 = \infty$	25°C	2		1.5	2.5		1.5	2.5	μA
		Full range				3		3		
$I_{I(\text{dev})}$ Deviation of reference input current over full temperature range‡	$R1 = 10 \text{ k}\Omega, R2 = \infty$	Full range	2		0.2	1.2		0.5	1.2	μA
Minimum cathode current for regulation	$V_{KA} = V_{I(\text{ref})}$ to 36 V	25°C	1		0.45	1		0.45	1	mA
I_{off} Off-state cathode current	$V_{KA} = 36 \text{ V}, V_{I(\text{ref})} = 0$	25°C	3		0.18	0.5		0.18	0.5	μA
		Full range				2		2		
$ z_{KA} $ Output impedance§	$V_{KA} = V_{I(\text{ref})}, f \leq 1 \text{ kHz}, I_{KA} = 1 \text{ mA to } 100 \text{ mA}$	25°C	1		0.2	0.4		0.2	0.4	Ω

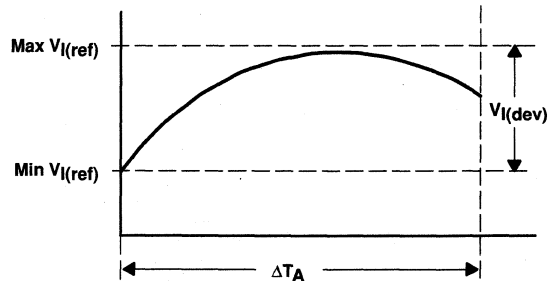
† Full range is 0°C to 70°C for C-suffix devices and -40°C to 125°C for Q-suffix devices.

‡ The deviation parameters $V_{I(\text{dev})}$ and $I_{I(\text{dev})}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{V_{I(\text{ref})}}$ is defined as:

$$\alpha_{V_{I(\text{ref})}} \left(\frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left(\frac{V_{I(\text{dev})}}{V_{I(\text{ref}) \text{ at } 25^\circ\text{C}}} \right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



$\alpha_{V_{I(\text{ref})}}$ is positive or negative depending on whether minimum $V_{I(\text{ref})}$ or maximum $V_{I(\text{ref})}$, respectively, occurs at the lower temperature.

§ The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}| \left(1 + \frac{R1}{R2} \right)$.

electrical characteristics at $I_{KA} = 10 \text{ mA}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TEST CIRCUIT	TL1431Y			UNIT
			MIN	TYP	MAX	
$V_{I(\text{ref})}$	Reference input voltage	$V_{KA} = V_{I(\text{ref})}$	2490	2500	2510	mV
$\frac{\Delta V_{I(\text{ref})}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	$\Delta V_{KA} = 3 \text{ V to } 36 \text{ V}$		-1.1	-2	mV/V
$I_{I(\text{ref})}$	Reference input current	$R1 = 10 \text{ k}\Omega$, $R2 = \infty$		1.44	2.5	μA
$I_{KA(\text{min})}$	Minimum cathode current for regulation	$V_{KA} = V_{I(\text{ref})}$ to 36 V		0.45	1	mA
I_{off}	Off-state cathode current	$V_{KA} = 36 \text{ V}$, $V_{\text{ref}} = 0$		0.18	0.5	μA
$ z_{KA} $	Output impedance†	$V_{KA} = V_{I(\text{ref})}$, $f \leq 1 \text{ kHz}$, $I_{KA} = 1 \text{ mA to } 100 \text{ mA}$		0.2	0.4	Ω

† The output impedance is defined as: $|z'| = \frac{\Delta V}{\Delta I}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$,

which is approximately equal to $|z_{KA}| \left(1 + \frac{R1}{R2}\right)$.

PARAMETER MEASUREMENT INFORMATION

$$\left| \alpha_{V_{I(\text{ref})}} \right| \left(\frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left(\frac{V_{I(\text{dev})}}{V_{I(\text{ref})} \text{ at } 25^\circ\text{C}} \right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.

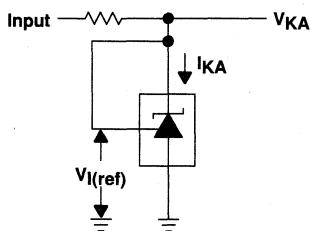
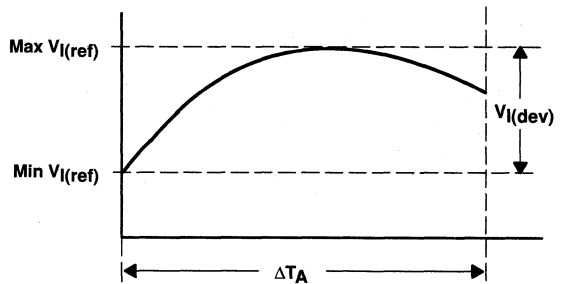


Figure 1. Test Circuit for $V_{(KA)} = V_{\text{ref}}$

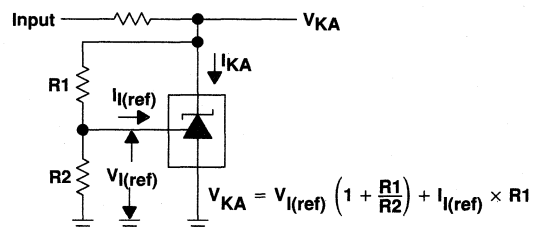


Figure 2. Test Circuit for $V_{(KA)} > V_{\text{ref}}$

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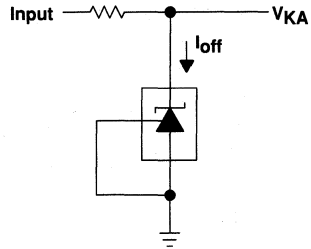


Figure 3. Test Circuit for I_{off}

TYPICAL CHARACTERISTICS

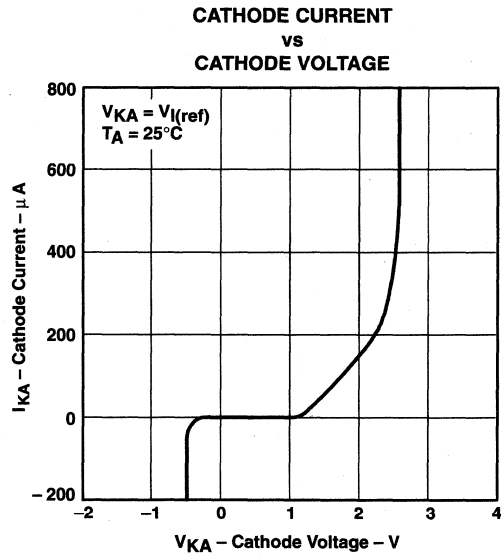
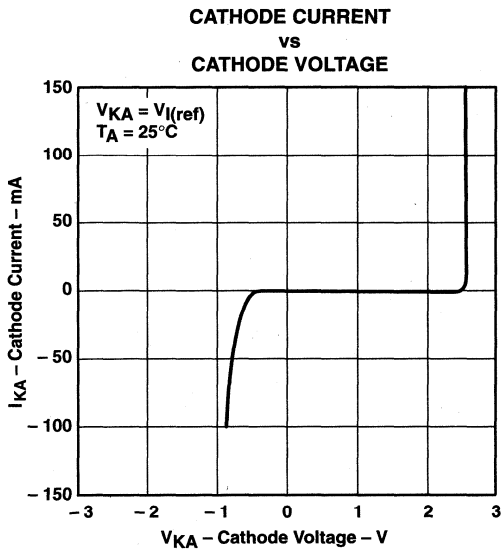
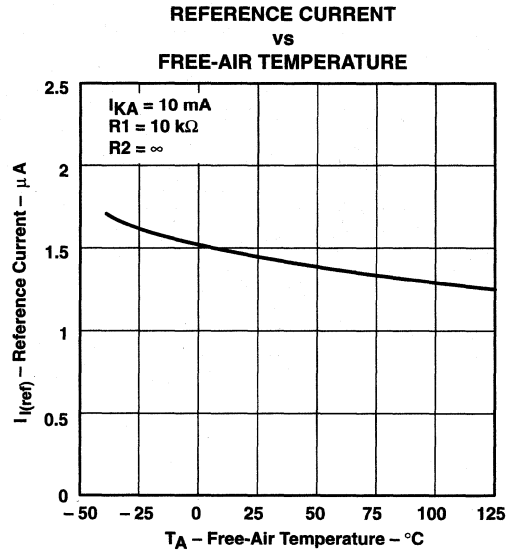
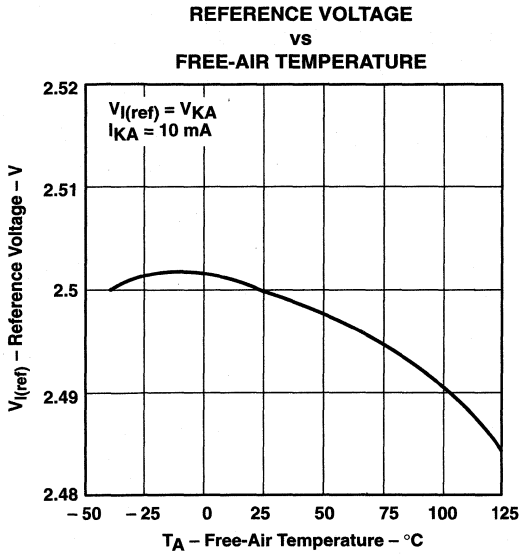
Table of Graphs

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Cathode current vs Cathode voltage	6, 7
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TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

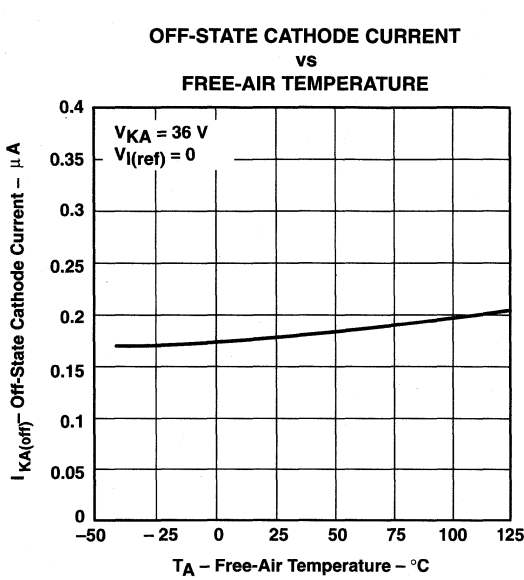


Figure 8

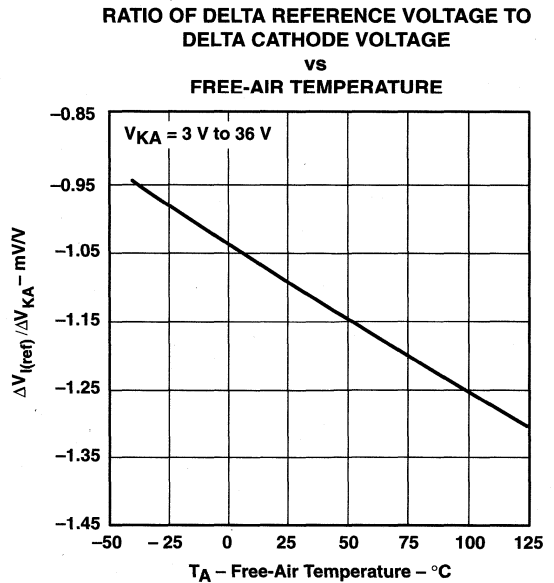


Figure 9

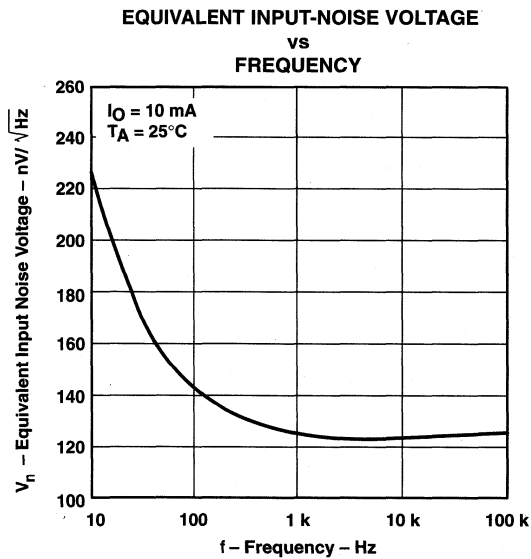


Figure 10

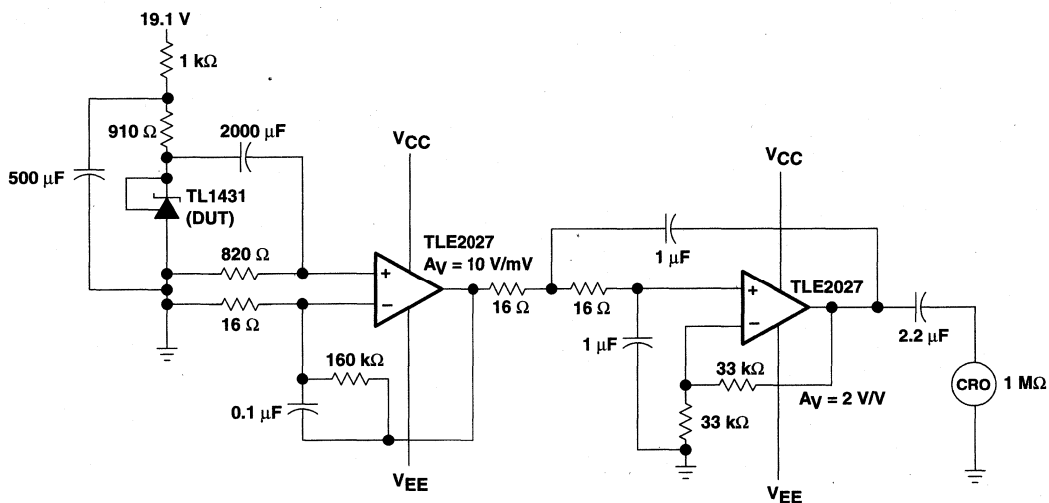
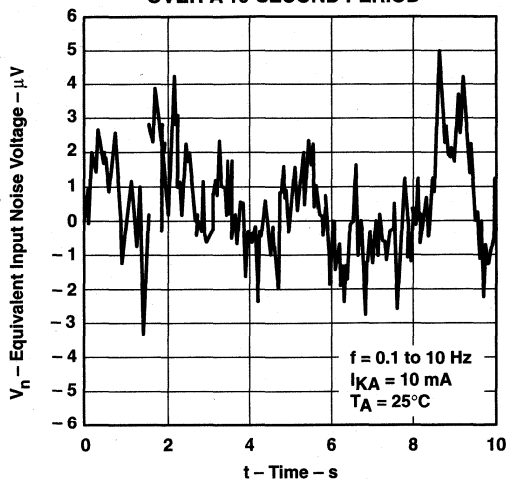
† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

EQUIVALENT INPUT-NOISE VOLTAGE OVER A 10-SECOND PERIOD



TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT INPUT-NOISE VOLTAGE

Figure 11

TYPICAL CHARACTERISTICS

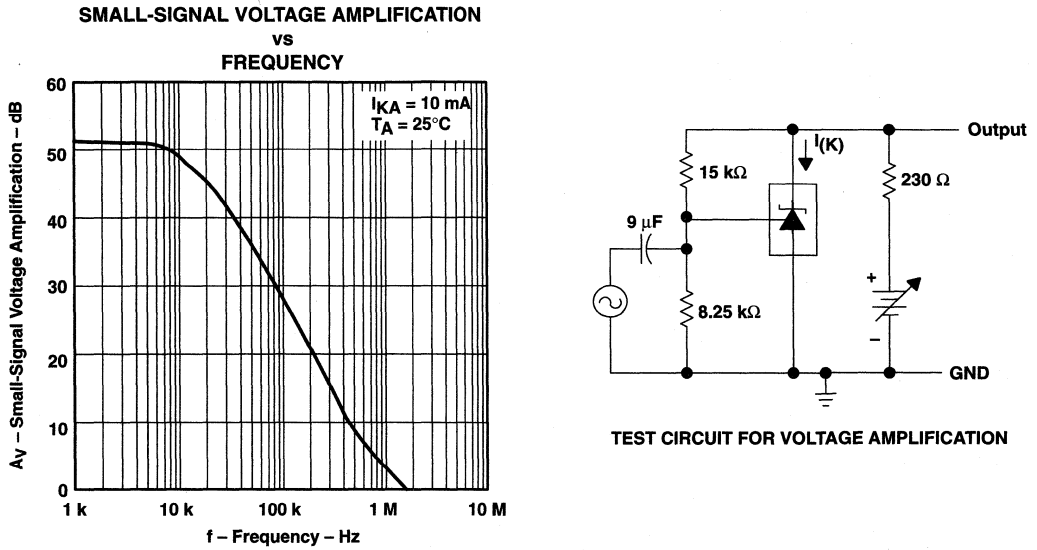


Figure 12

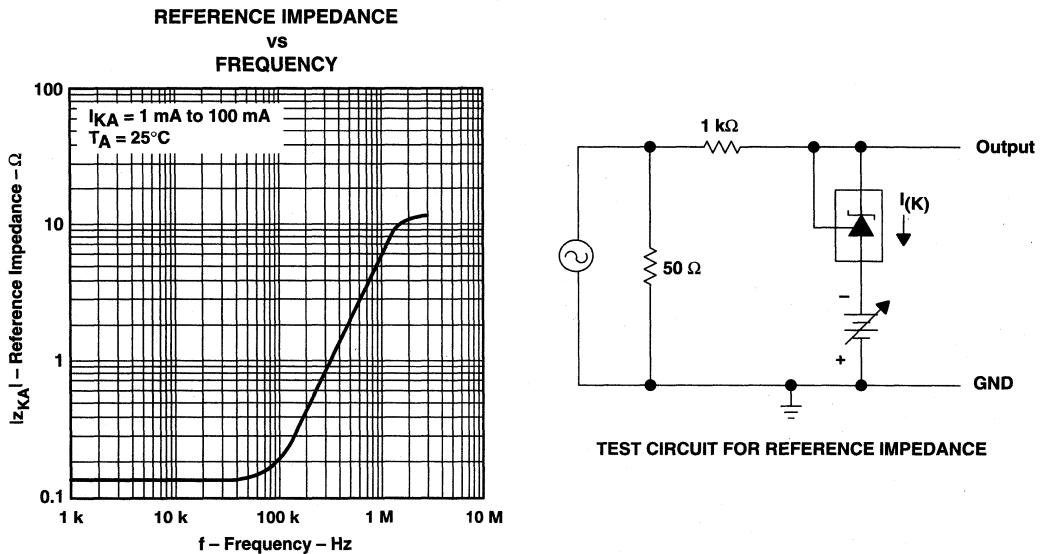


Figure 13

TYPICAL CHARACTERISTICS

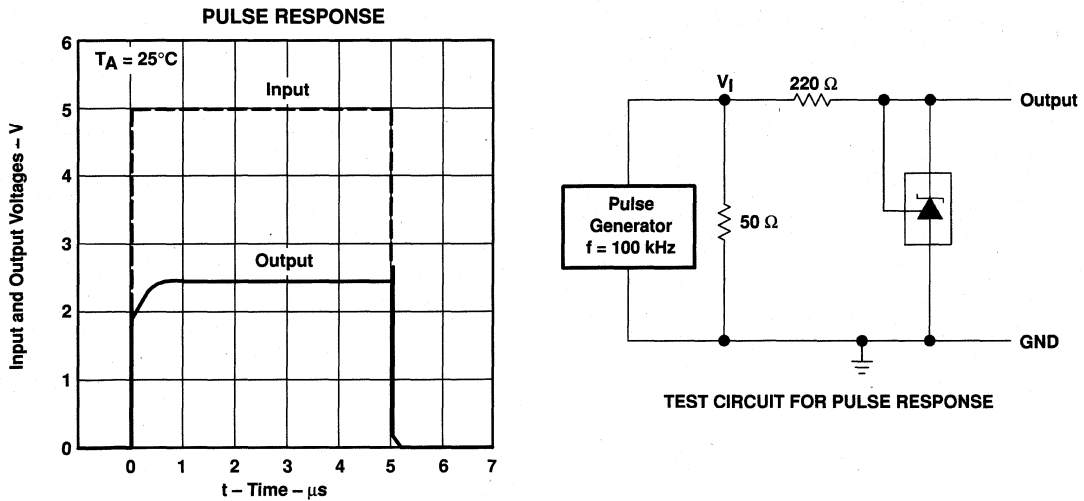


Figure 14

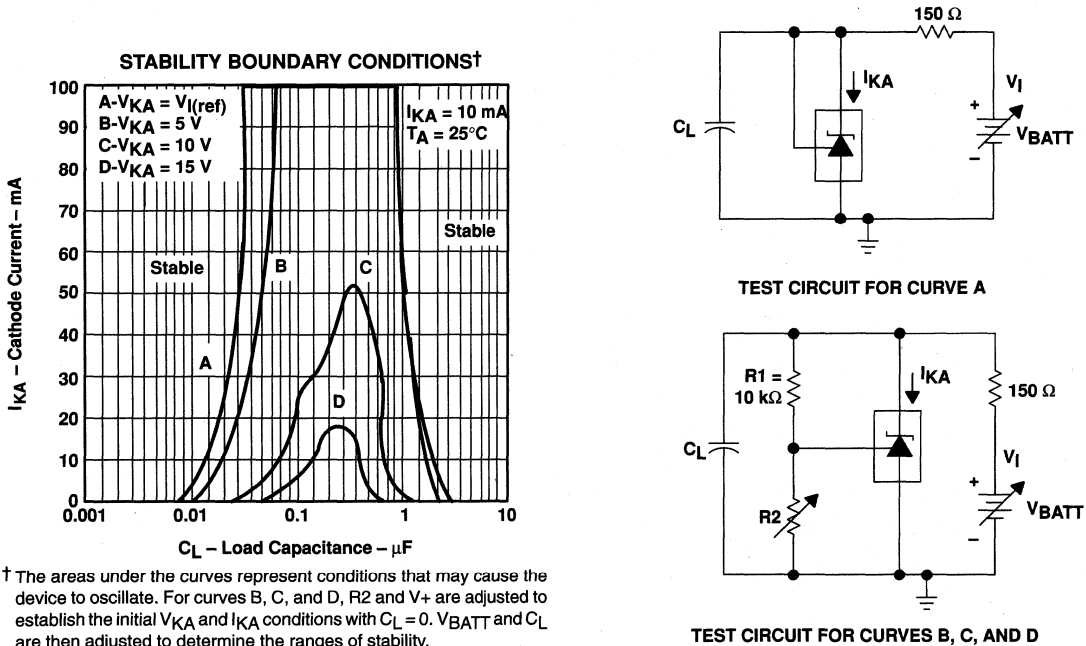
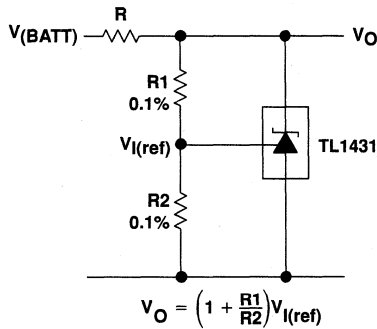


Figure 15

APPLICATION INFORMATION

Table of Application Circuits

APPLICATION	FIGURE
Shunt regulator	16
Single-supply comparator with temperature-compensated threshold	17
Precision high-current series regulator	18
Output control of a 3-terminal fixed regulator	19
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Crowbar	21
Precision 5-V, 1.5-A, 0.5% regulator	22
5-V precision regulator	23
PWM converter with 0.5% reference	24
Voltage monitor	25
Delay timer	26
Precision current limiter	27
Precision constant-current sink	28



NOTE A. R should provide cathode current ≥ 1 mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 16. Shunt Regulator

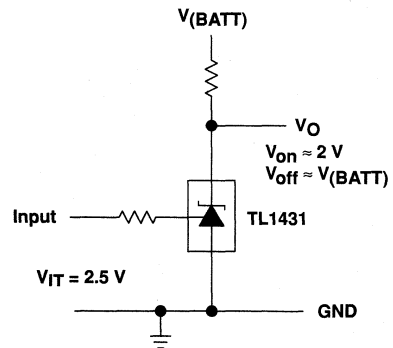
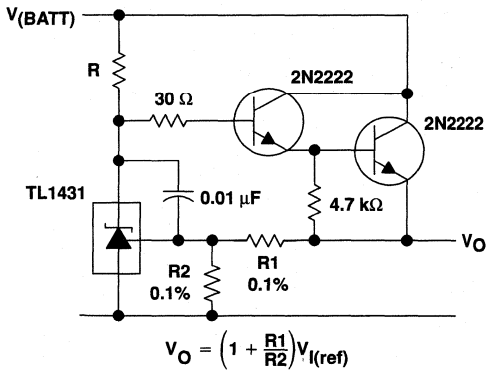


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold

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APPLICATION INFORMATION



NOTE A. R should provide cathode current ≥ 1 mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 18. Precision High-Current Series Regulator

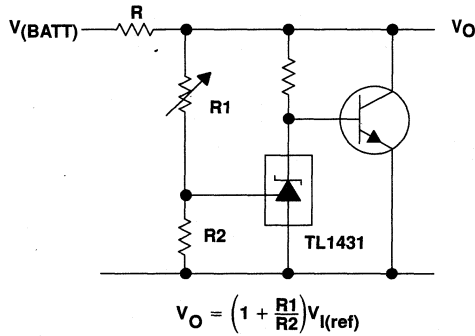


Figure 20. Higher-Current Shunt Regulator

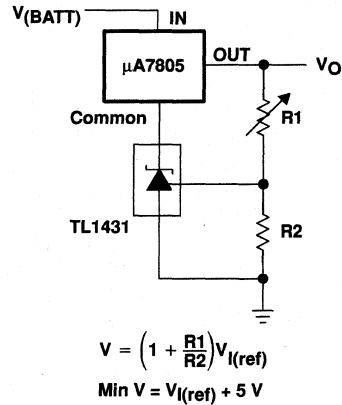
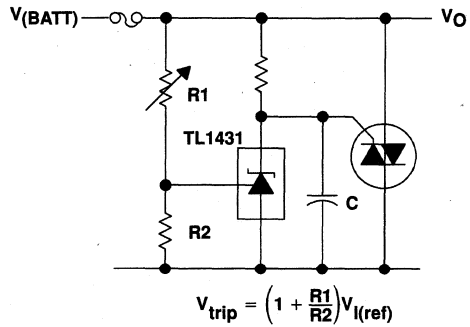


Figure 19. Output Control of a Three-Terminal Fixed Regulator



NOTE A. Refer to the stability boundary conditions in Figure 15 to determine allowable values for C.

Figure 21. Crowbar

APPLICATION INFORMATION

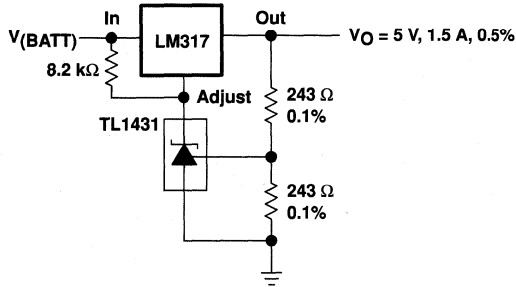
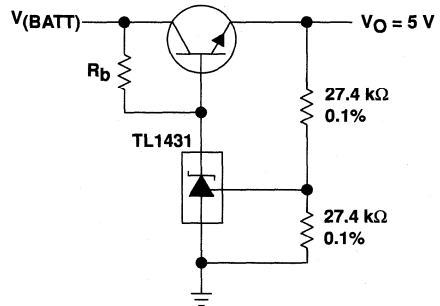


Figure 22. Precision 5-V, 1.5-A, 0.5% Regulator



NOTE A. R_b should provide cathode current ≥ 1 mA to the TL1431.

Figure 23. 5-V Precision Regulator

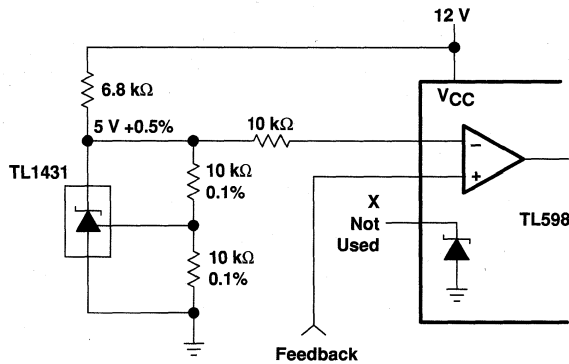
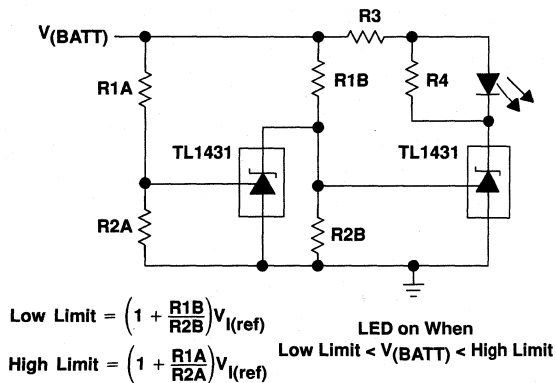


Figure 24. PWM Converter With 0.5% Reference

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APPLICATION INFORMATION



NOTE A. Select R3 and R4 to provide the desired LED intensity and cathode current ≥ 1 mA to the TL1431.

Figure 25. Voltage Monitor

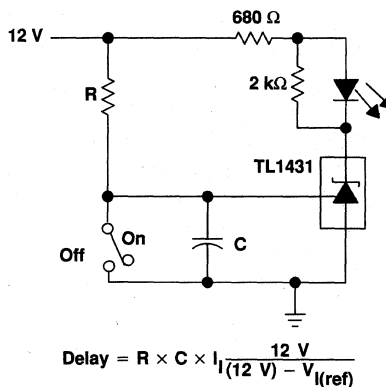


Figure 26. Delay Timer

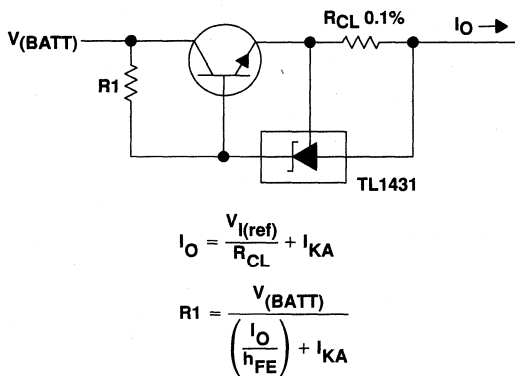


Figure 27. Precision Current Limiter

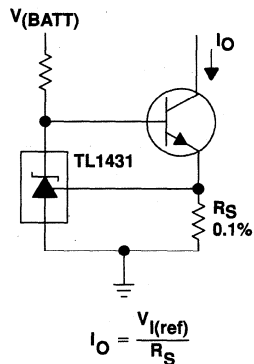


Figure 28. Precision Constant-Current Sink

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TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

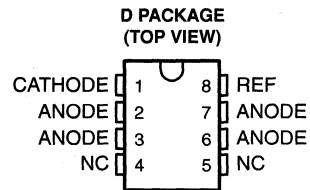
- Low-Voltage Operation . . . Down to 1.24 V
- 1% Reference-Voltage Tolerance (TLV431A)
- Adjustable Output Voltage, $V_O = V_{ref}$ to 6 V
- Low Operational Cathode Current . . . 80 μ A Typ
- 0.25- Ω Typical Output Impedance
- Package Options Include Plastic Small-Outline (D), SOT-23 (DBV), and Cylindrical (LP) Packages

description

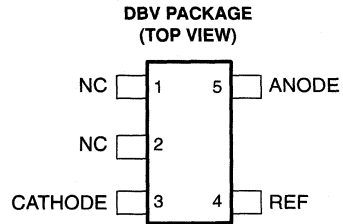
The TLV431 and TLV431A are low-voltage three-terminal adjustable voltage references with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{ref} (1.24 V) and 6 V with two external resistors (see Figure 2). The TLV431 and TLV431A operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

When used with an optocoupler, the TLV431 and TLV431A are ideal voltage references in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. These devices have a typical output impedance of 0.25 Ω . Active output circuitry provides a very sharp turn-on characteristic, making the TLV431 and TLV431A excellent replacements for low-voltage zener diodes in many applications, including onboard regulation and adjustable power supplies.

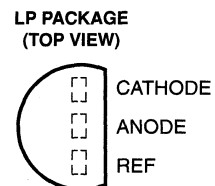
The TLV431C and TLV431AC devices are characterized for operation from 0°C to 70°C. The TLV431I and TLV431AI devices are characterized for operation from -40°C to 85°C.



NC – No internal connection



NC – No internal connection



AVAILABLE OPTIONS

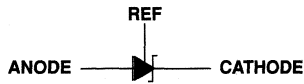
T _A	PACKAGED DEVICES			CHIP FORM (Y)
	TO-92 (LP)	SOIC (D)	SOT-23 (DBV)	
0°C to 70°C	TLV431CLP TLV431ACL	— —	TLV431CDBV TLV431ACDBV	TLV431Y
-40°C to 85°C	TLV431ILP TLV431AILP	TLV431IID TLV431AID	TLV431IDBV TLV431AIDBV	

The LP package is available taped and reeled. Add the suffix R to the device type (e.g., TLV431ACLPR). The D and DBV are available only taped and reeled (e.g., TLV431IOR). Chip forms are tested at 25°C.

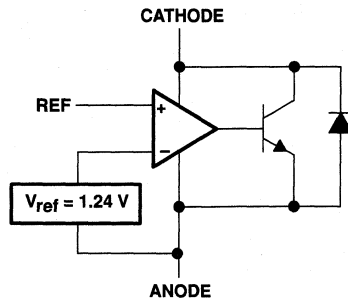
TLV431, TLV431A LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

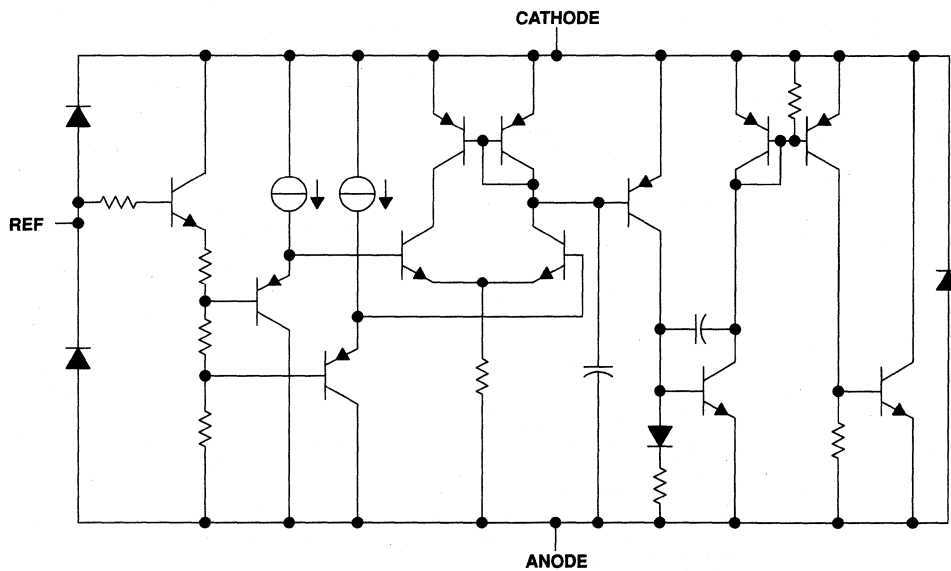
logic symbol



logic diagram (positive logic)



equivalent schematic



TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cathode voltage, V_{KA} (see Note 1)	7 V
Continuous cathode current range, I_K	–20 mA to 20 mA
Reference current range, I_{ref}	–0.05 mA to 3 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package	97°C/W
DBV package	347°C/W
LP package	156°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to the anode terminal unless otherwise noted.
 2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	6	V
Cathode current, I_K	0.1	15	mA
Operating free-air temperature range, T_A	TLV431C, TLV431AC	0	70
	TLV431I, TLV431AI	–40	85
			°C



TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV431C			TLV431I			UNIT					
		MIN	TYP	MAX	MIN	TYP	MAX						
V _{ref} Reference voltage	V _{KA} = V _{ref} , I _K = 10 mA	T _A = 25°C		1.222	1.24	1.258	1.222	1.24	1.258	V			
		T _A = full range (see Note 4 and Figure 1)		1.21		1.27		1.202			1.278		
V _{ref(dev)}	V _{ref} deviation over full temperature range (see Note 5)	V _{KA} = V _{ref} , I _K = 10 mA, (see Note 4 and Figure 1)			4		12		6		20		mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of V _{ref} change in cathode voltage change	I _K = 10 mA, V _{KA} = V _{ref} to 6 V, (see Figure 2)			-1.5		-2.7		-1.5		-2.7		mV/V
I _{ref}	Reference terminal current	I _K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 2)			0.15		0.5		0.15		0.5		μA
I _{ref(dev)}	I _{ref} deviation over full temperature range (see Note 5)	I _K = 10 mA, R1 = 10 kΩ, R2 = open (see Note 4 and Figure 2)			0.05		0.3		0.1		0.4		μA
I _{K(min)}	Minimum cathode current for regulation	V _{KA} = V _{ref} (see Figure 1)			55		80		55		80		μA
I _{K(off)}	Off-state cathode current	V _{KA} = 6 V, V _{ref} = 0 (see Figure 3)			0.001		0.1		0.001		0.1		μA
z _{KA}	Dynamic impedance (see Note 6)	V _{KA} = V _{ref} , f ≤ 1 kHz, I _K = 0.1 mA to 15 mA (see Figure 1)			0.25		0.4		0.25		0.4		Ω

NOTES: 4. Full range is -40°C to 85°C for the TLV431I, and 0°C to 70°C for the TLV431C.

5. The deviation parameters V_{ref(dev)} and I_{ref(dev)} are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, α_{V_{ref}}, is defined as:

$$|\alpha_{V_{ref}}| \left(\frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref \text{ at } 25^{\circ}\text{C}}} \right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.

α_{V_{ref}} can be positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

6. The dynamic impedance is defined as: $z_{KA} = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z_{KA}| = \frac{\Delta V}{\Delta I} \approx |z_{KA}| \times \left(1 + \frac{R1}{R2} \right)$$

TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV431AC			TLV431AI			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{ref} Reference voltage	V _K A = V _{ref} , I _K = 10 mA, T _A = 25°C T _A = full range, (see Note 4 and Figure 1)	1.228	1.24	1.252	1.228	1.24	1.252	V
		1.221		1.259	1.215		1.265	
V _{ref(dev)} V _{ref} deviation over full temperature range (see Note 5)	V _K A = V _{ref} , I _K = 10 mA (see Note 4 and Figure 1)		4	12		6	20	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$ Ratio of V _{ref} change in cathode voltage change	I _K = 10 mA, V _K A = V _{ref} to 6 V (see Figure 2)		-1.5	-2.7		-1.5	-2.7	mV/V
I _{ref} Reference terminal current	I _K = 10 mA, (see Figure 2) R1 = 10 kΩ		0.15	0.5		0.15	0.5	μA
I _{ref(dev)} I _{ref} deviation over full temperature range (see Note 5)	I _K = 10 mA, R1 = 10 kΩ, R2 = open (see Note 4 and Figure 2)		0.05	0.3		0.1	0.4	μA
I _{K(min)} Minimum cathode current for regulation	V _K A = V _{ref} (see Figure 1)		55	80		55	80	μA
I _{K(off)} Off-state cathode current	V _K A = 6 V, V _{ref} = 0, (see Figure 3)		0.001	0.1		0.001	0.1	μA
z _{KA} Dynamic impedance (see Note 6)	V _K A = V _{ref} , f ≤ 1 kHz, I _K = 0.1 mA to 15 mA (see Figure 1)		0.25	0.4		0.25	0.4	Ω

- NOTES: 4. Full range is -40°C to 85°C for the TLV431I, and 0°C to 70°C for the TLV431C.
 5. The deviation parameters V_{ref(dev)} and I_{ref(dev)} are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, α_{V_{ref}}, is defined as:

$$|\alpha_{V_{ref}}| \left(\frac{\text{ppm}}{^{\circ}\text{C}} \right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref \text{ at } 25^{\circ}\text{C}}} \right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.

α_{V_{ref}} can be positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

6. The dynamic impedance is defined as: |z_{KA}| = $\frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z_{KA}| = \frac{\Delta V}{\Delta I} \approx |z_{KA}| \times \left(1 + \frac{R1}{R2} \right)$$

TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TLV431Y			UNIT
		MIN	TYP	MAX	
V_{ref}	Reference voltage $V_{KA} = V_{ref}, I_K = 10 \text{ mA}$ (see Figure 1) $T_A = 25^\circ\text{C}$	1.24			V
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of V_{ref} change in cathode voltage change $I_K = 10 \text{ mA}, \Delta V_{KA} = V_{ref}$ to 6 V (see Figure 2)	-1.5			mV/V
I_{ref}	Reference terminal current $I_K = 10 \text{ mA}, R1 = 10 \text{ k}\Omega, R2 = \text{open}$ (see Figure 2)	0.15			μA
$I_{K(\text{min})}$	Minimum cathode current for regulation $V_{KA} = V_{ref}$ (see Figure 1)	55			μA
I_{off}	Off-state cathode current $V_{KA} = 6 \text{ V}, V_{ref} = 0$ (see Figure 3)	0.001			μA
$ z_{KA} $	Dynamic impedance (see Note 6) $V_{KA} = V_{ref}, f \leq 1 \text{ kHz}, I_K = 0.1 \text{ mA}$ to 15 mA (see Figure 1)	0.25			Ω

NOTE 6: The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z_{KA}| = \frac{\Delta V}{\Delta I} \approx |z_{KA}| \times \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

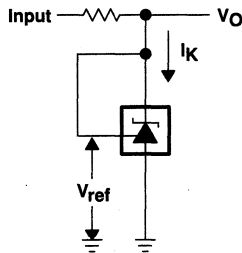


Figure 1. Test Circuit for $V_{KA} = V_{ref}$,
 $V_O = V_{KA} = V_{ref}$

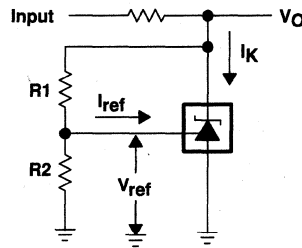


Figure 2. Test Circuit for $V_{KA} > V_{ref}$,
 $V_O = V_{KA} = V_{ref} \times (1 + R1/R2) + I_{ref} \times R1$

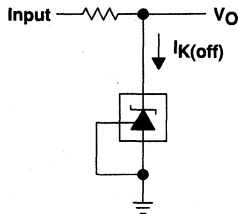


Figure 3. Test Circuit for $I_{K(\text{off})}$

TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION†

**REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE**

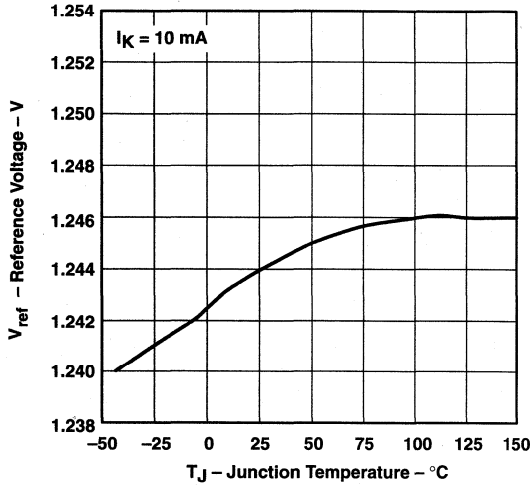


Figure 4

**REFERENCE INPUT CURRENT
vs
JUNCTION TEMPERATURE**

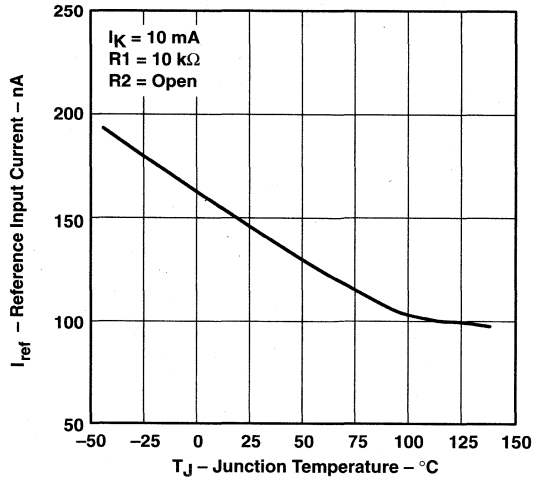


Figure 5

**CATHODE CURRENT
vs
CATHODE VOLTAGE**

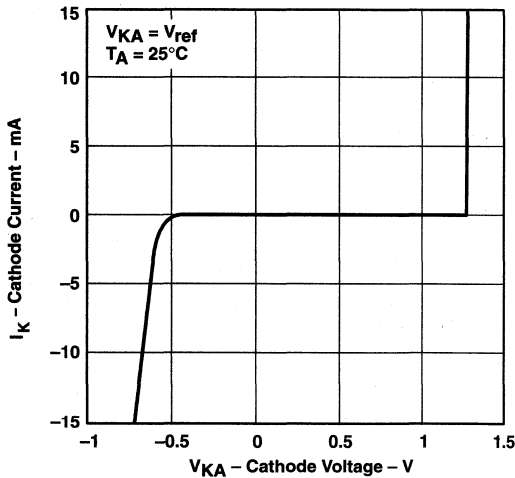


Figure 6

**CATHODE CURRENT
vs
CATHODE VOLTAGE**

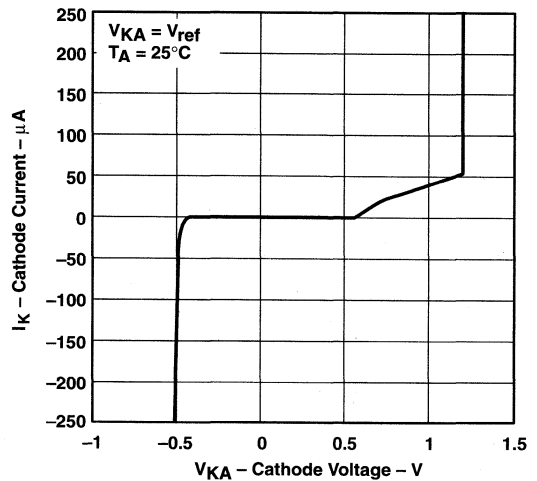


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TLV431, TLV431A LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION†

OFF-STATE CATHODE CURRENT
vs
JUNCTION TEMPERATURE

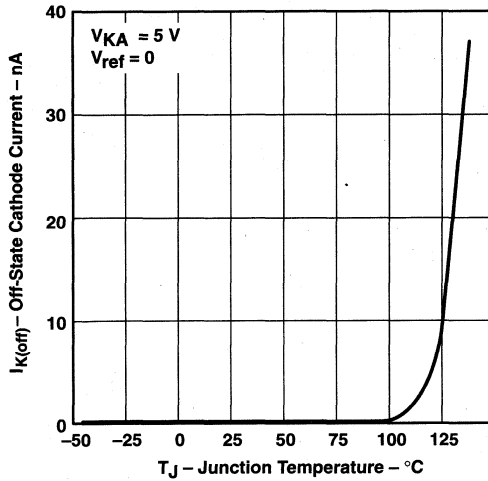


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE
TO DELTA CATHODE VOLTAGE
vs
JUNCTION TEMPERATURE

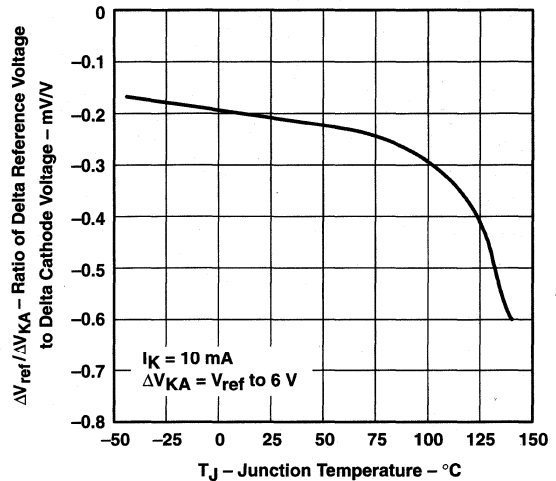


Figure 9

PERCENTAGE CHANGE IN V_{ref}
vs
OPERATING LIFE AT 55°C

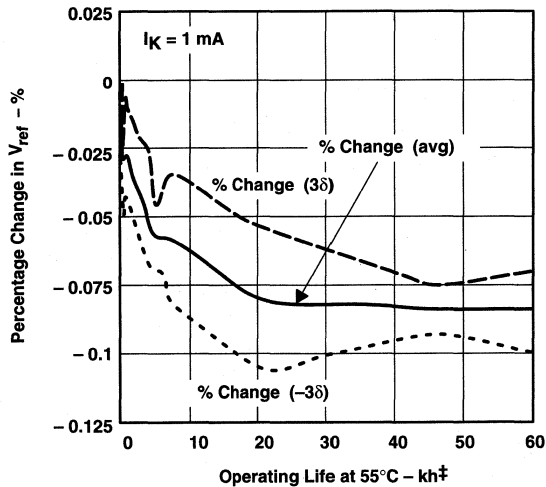


Figure 10

‡ Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7 eV.

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.



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TLV431, TLV431A LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

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PARAMETER MEASUREMENT INFORMATION

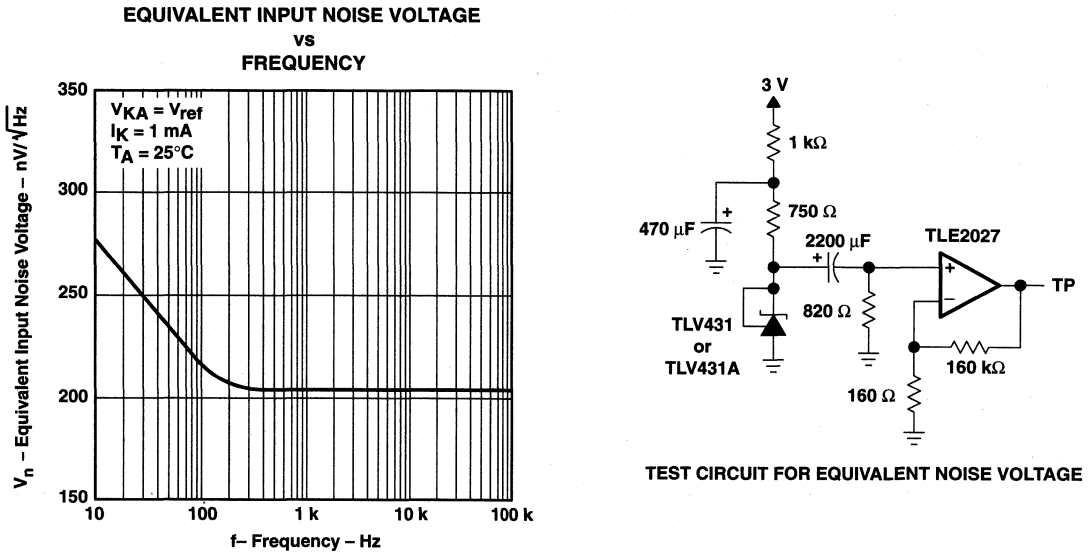


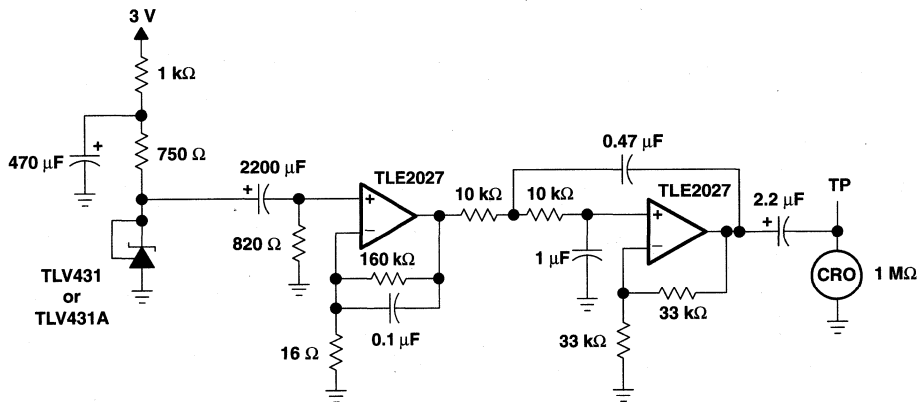
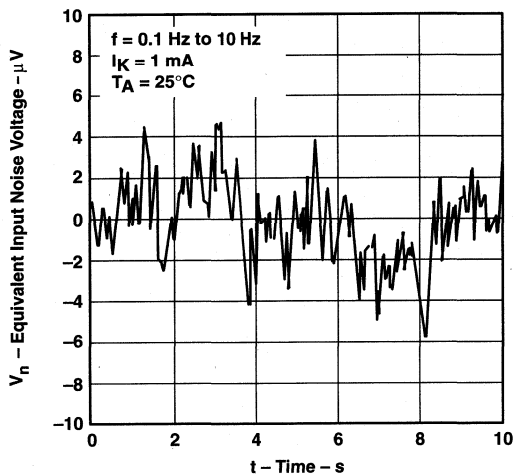
Figure 11

TLV431, TLV431A LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

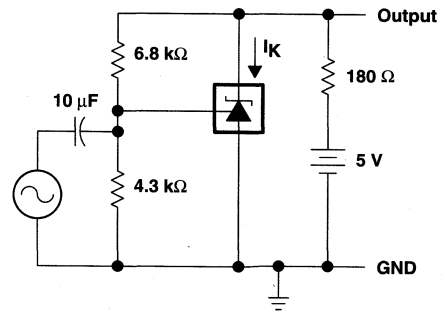
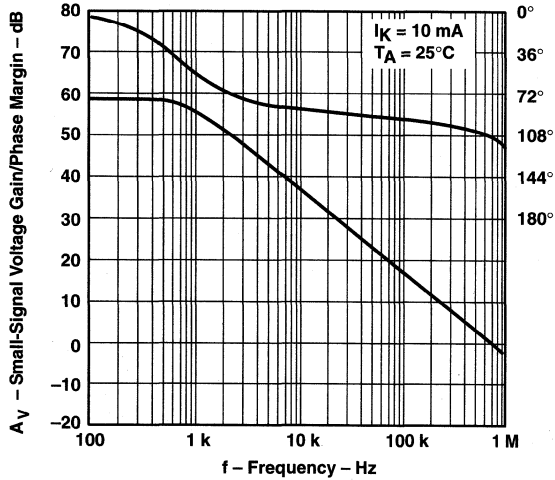


TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

Figure 12

PARAMETER MEASUREMENT INFORMATION

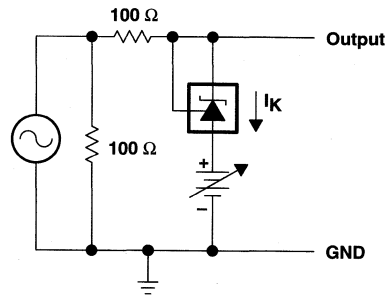
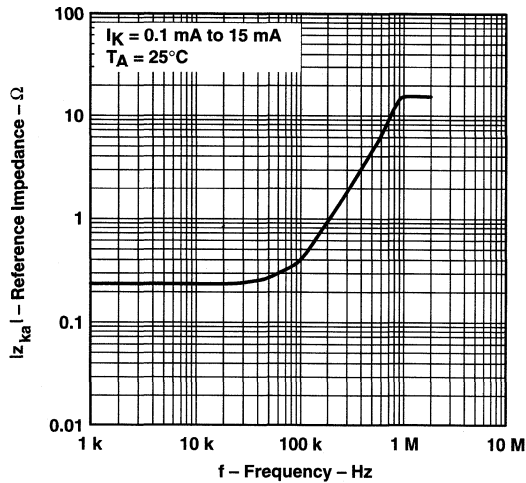
SMALL-SIGNAL VOLTAGE GAIN
 /PHASE MARGIN
 vs
 FREQUENCY



TEST CIRCUIT FOR VOLTAGE GAIN AND PHASE MARGIN

Figure 13

REFERENCE IMPEDANCE
 vs
 FREQUENCY



TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 14

TLV431, TLV431A LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION

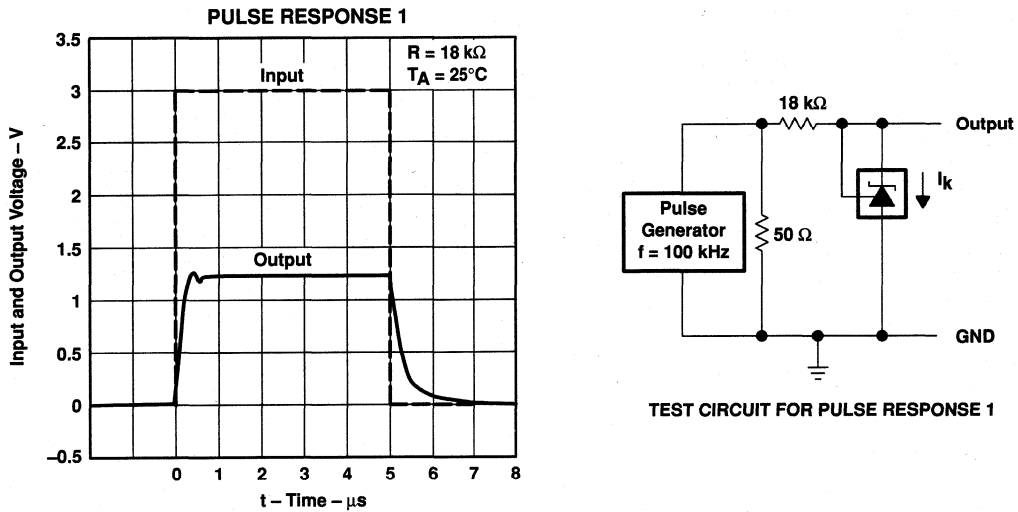


Figure 15

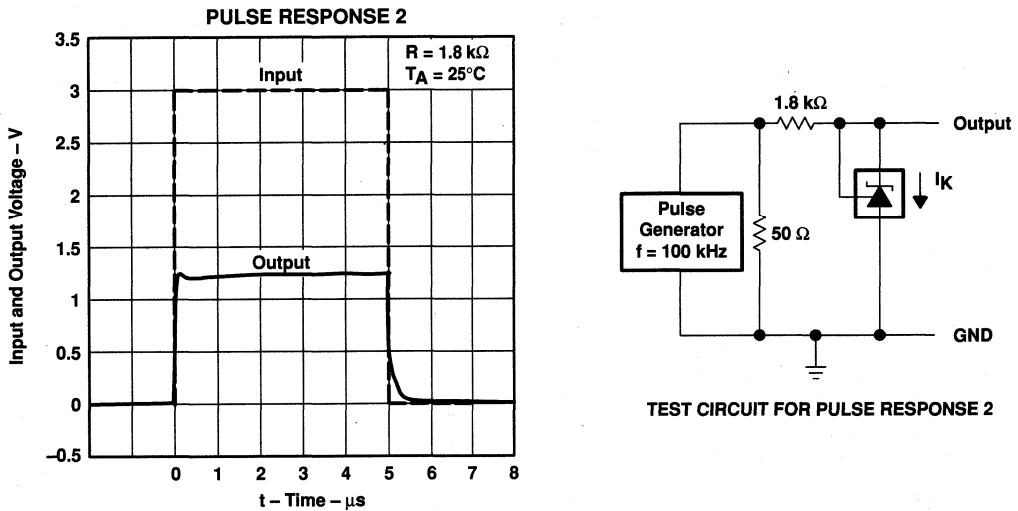


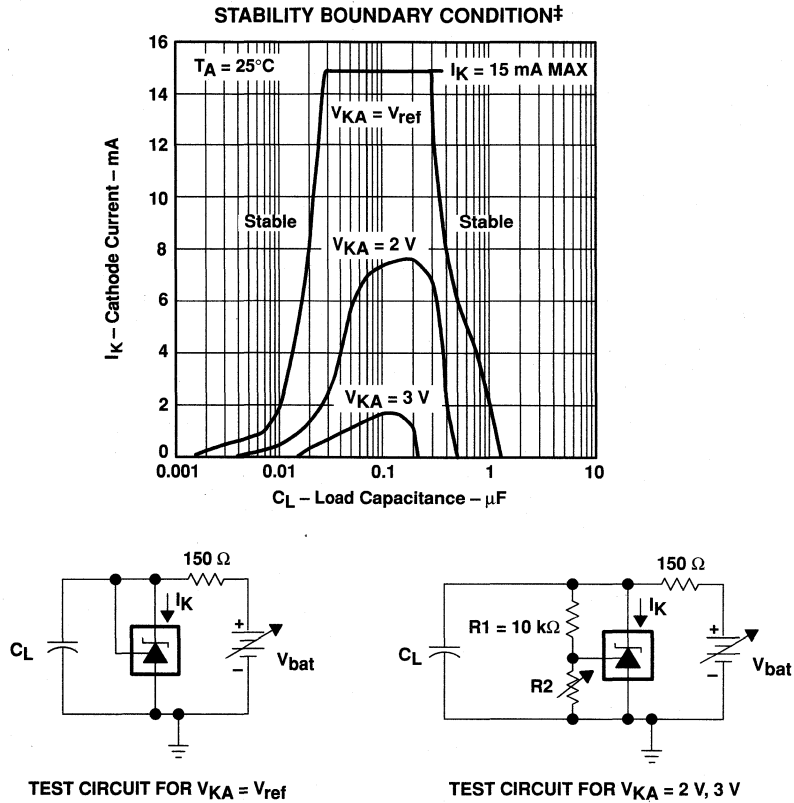
Figure 16

TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

SLVS139C – JULY 1996 – REVISED JULY 1999

PARAMETER MEASUREMENT INFORMATION†



‡ The areas under the curves represent conditions that may cause the device to oscillate. For $V_{KA} = 2\text{-V}$ and 3-V curves, R_2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with $C_L = 0$. V_{bat} and C_L then were adjusted to determine the ranges of stability.

Figure 17

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TLV431, TLV431A

LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

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APPLICATION INFORMATION

Figure 18 shows the TLV431 or TLV431A used in a 3.3-V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{ref} ($1.24\text{ V} \pm 1\%$). The output of the regulator, plus the forward voltage drop of the optocoupler LED ($1.24 + 1.4 = 2.64\text{ V}$), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible using the circuit in Figure 18.

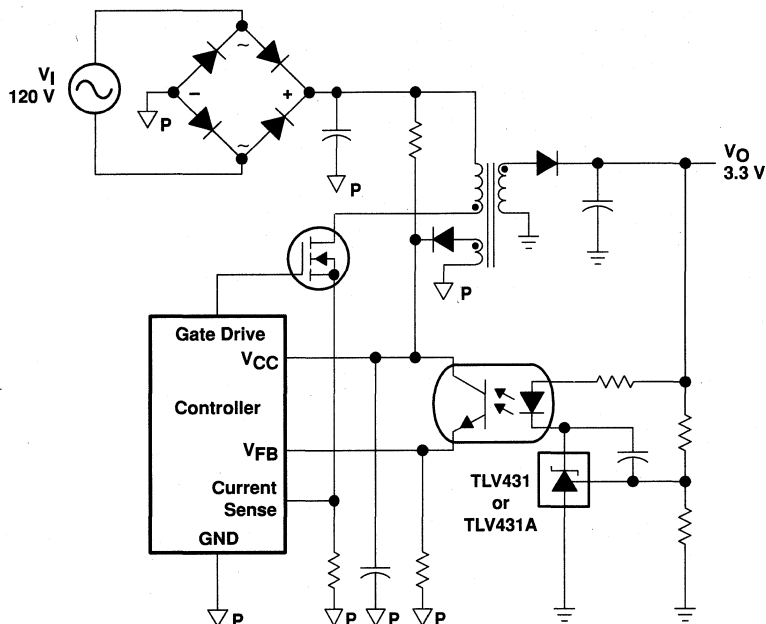


Figure 18. Flyback With Isolation Using TLV431 or TLV431A as Voltage Reference and Error Amplifier

General Information (Vol. 1)	1
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4 Precision Virtual Grounds

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C – MARCH 1991 – REVISED MAY 1998

- 2.5-V Virtual Ground for 5-V/GND Analog Systems
- Self-Contained in Small-Outline, Dual-In-Line or 3-Terminal TO-226AA Packages
- High Output-Current Capability Sink or Source . . . 20 mA Typ
- Micropower Operation . . . 170 μ A Typ
- Excellent Regulation Characteristics
 - Output Regulation
 - 45 μ V Typ at $I_O = 0$ to –10 mA
 - +15 μ V Typ at $I_O = 0$ to +10 mA
 - Input Regulation = 1.5 μ V/V Typ
- Low-Impedance Output . . . 0.0075 Ω Typ
- Macromodel Included

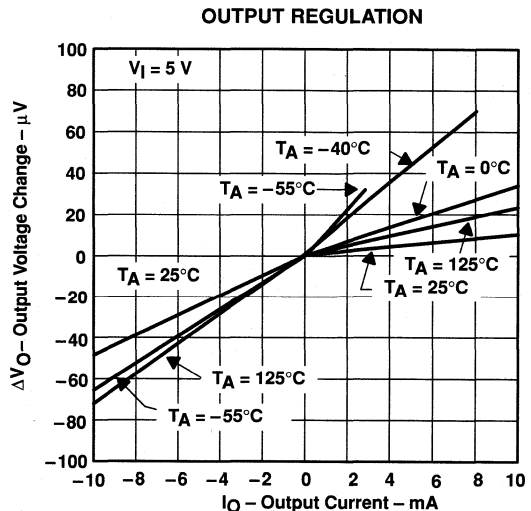
description

In signal-conditioning applications using a single power source, a reference voltage is required for termination of all signal grounds. To accomplish this, engineers have typically used solutions consisting of resistors, capacitors, operational amplifiers, and voltage references. Texas Instruments has eliminated all of those components with one easy-to-use 3-terminal device. That device is the TLE2425 precision virtual ground.

Use of the TLE2425 over other typical circuit solutions gives the designer increased dynamic signal range, improved signal-to-noise ratio, lower distortion, improved signal accuracy, and easier interfacing to ADCs and DACs. These benefits are the result of combining a precision micropower voltage reference and a high-performance precision operational amplifier in a single silicon chip. It is the precision and performance of these two circuit functions together that yield such dramatic system-level performance.

The TLE2425 improves input regulation as well as output regulation and, in addition, reduces output impedance and power dissipation in a majority of virtual-ground-generation circuits. Both input regulation and load regulation exceed 12 bits of accuracy on a single 5-V system. Signal-conditioning front ends of data acquisition systems that push 12 bits and beyond can use the TLE2425 to eliminate a major source of system error.

The TLE2425C is characterized for operation from 0°C to 70°C. The TLE2425I is characterized for operation from –40°C to 85°C. The TLE2425M is characterized for operation over the full military temperature range of –55°C to 125°C.



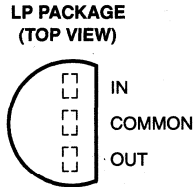
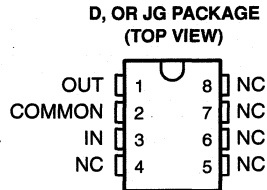
AVAILABLE OPTIONS

T _A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC TO-226AA (LP)	
0°C to 70°C	TLE2425CD	—	TLE2425CD	TLE2425Y
–40°C to 85°C	TLE2425ID	—	TLE2425ID	—
–55°C to 125°C	TLE2425MD	TLE2425MD	TLE2425MD	—

† The D and LP packages are available taped and reeled in the commercial temperature range only. Add R suffix to the device type (e.g., TLE2425CDR). The chip form is tested at 25°C.

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

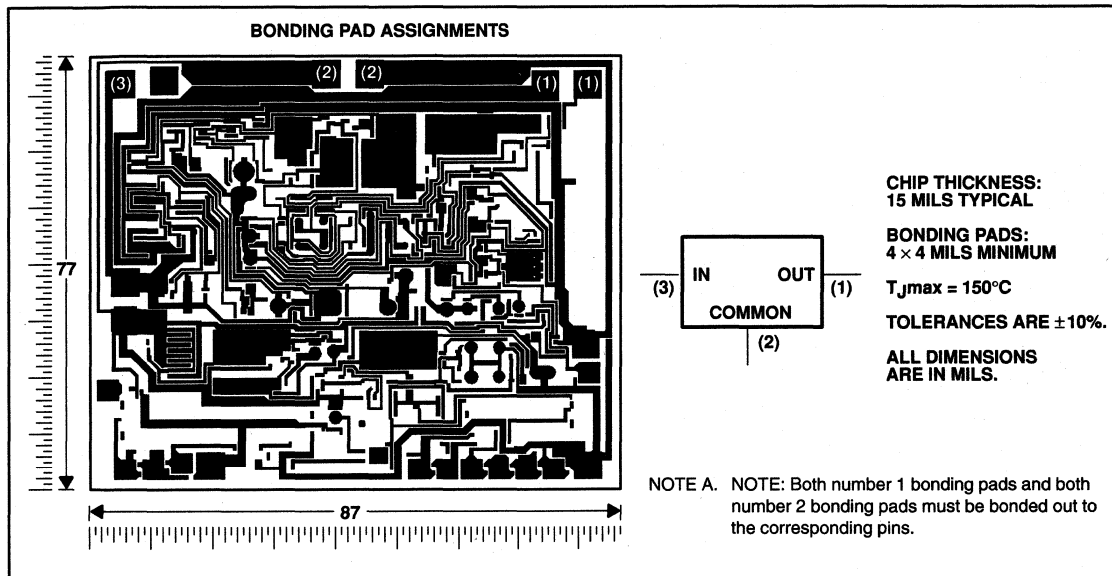
SLOS065C – MARCH 1991 – REVISED MAY 1998



NC – No internal connection

TLE2425Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2425C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Continuous input voltage, V_I	40 V
Output current, I_O	± 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C-suffix	0°C to 70°C
I-suffix	-40°C to 85°C
M-suffix	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	155 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	-40	85	-55	125	°C

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C – MARCH 1991 – REVISED MAY 1998

electrical characteristics at specified free-air temperature, $V_I = 5\text{ V}$, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLE2425C			UNIT
			MIN	TYP	MAX	
Output voltage		25°C	2.48	2.5	2.52	V
		Full range	2.47		2.53	
Temperature coefficient of output voltage		25°C	20			ppm/°C
Bias current	$I_O = 0$	25°C	170			μA
		Full range	250			
Input voltage regulation	$V_I = 4.5\text{ V to }5.5\text{ V}$	25°C	1.5			μV
		Full range	25			
	$V_I = 4\text{ V to }40\text{ V}$	25°C	1.5			μV/V
		Full range	25			
Ripple rejection	$f = 120\text{ Hz}$, $\Delta V_I(\text{PP}) = 1\text{ V}$	25°C	80			dB
Output voltage regulation (source current)‡	$I_O = 0\text{ to }-10\text{ mA}$	25°C	-160	-45	160	μV
		Full range	-250		250	
	$I_O = 0\text{ to }-20\text{ mA}$	25°C	-450	-150	450	
Output voltage regulation (sink current)‡	$I_O = 0\text{ to }10\text{ mA}$	25°C	-160	15	160	μV
		Full range	-250		250	
	$I_O = 0\text{ to }20\text{ mA}$	25°C	-235	65	235	
Long-term drift of output voltage	$\Delta t = 1000\text{ h}$, Noncumulative	25°C	15			ppm
Output impedance		25°C	7.5 22.5			mΩ
Short-circuit output current (sink current)	$V_O = 5\text{ V}$	25°C	30	55		mA
Short-circuit output current (source current)	$V_O = 0$		-30	-50		
Output noise voltage, rms	$f = 10\text{ Hz to }10\text{ kHz}$	25°C	100			μV
Output voltage response to output current step	$V_O\text{ to }0.1\%$, $I_O = \pm 10\text{ mA}$	25°C	$C_L = 0$	110		μs
			$C_L = 100\text{ pF}$	115		
	$V_O\text{ to }0.01\%$, $I_O = \pm 10\text{ mA}$	$C_L = 0$	180			
		$C_L = 100\text{ pF}$	180			
Output voltage response to input voltage step	$V_I = 4.5\text{ to }5.5\text{ V}$, $V_O\text{ to }0.1\%$	25°C	12			μs
	$V_I = 4.5\text{ to }5.5\text{ V}$, $V_O\text{ to }0.01\%$		30			
Output voltage turn-on response	$V_I = 0\text{ to }5\text{ V}$, $V_O\text{ to }0.1\%$	25°C	125			μs
	$V_I = 0\text{ to }5\text{ V}$, $V_O\text{ to }0.01\%$		210			

† Full range is 0°C to 70°C.

‡ The listed values are not production tested.



TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C – MARCH 1991 – REVISED MAY 1998

electrical characteristics at specified free-air temperature, $V_I = 5\text{ V}$, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A †	TLE2425I			UNIT
			MIN	TYP	MAX	
Output voltage		25°C	2.48	2.5	2.52	V
		Full range	2.47		2.53	
Temperature coefficient of output voltage		25°C	20			ppm/°C
Bias current	I _O = 0	25°C	170		250	μA
		Full range			250	
Input voltage regulation	V _I = 4.5 V to 5.5 V	25°C	1.5		20	μV
		Full range			75	
	V _I = 4 V to 40 V	25°C	1.5		20	μV/V
		Full range			75	
Ripple rejection	f = 120 Hz, ΔV _I (PP) = 1 V	25°C	80			dB
Output voltage regulation (source current)‡	I _O = 0 to -10 mA	25°C	-160	-45	160	μV
		Full range			250	
	I _O = 0 to -20 mA	25°C	-450	-150	450	
Output voltage regulation (sink current)‡	I _O = 0 to 8 mA	25°C	-160	15	160	μV
		Full range			250	
	I _O = 0 to 20 mA	25°C	-235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative	25°C	15			ppm
Output impedance		25°C	7.5		22.5	mΩ
Short-circuit output current (sink current)	V _O = 5 V	25°C	30		55	mA
Short-circuit output current (source current)	V _O = 0		-30		-50	
Output noise voltage, rms	f = 10 Hz to 10 kHz	25°C	100			μV
Output voltage response to output current step	V _O to 0.1%, I _O = ±10 mA	25°C	C _L = 0		110	μs
			C _L = 100 pF		115	
	V _O to 0.01%, I _O = ±10 mA		C _L = 0		180	
			C _L = 100 pF		180	
Output voltage response to input voltage step	V _I = 4.5 to 5.5 V, V _O to 0.1%	25°C	12			μs
	V _I = 4.5 to 5.5 V, V _O to 0.01%		30			
Output voltage turn-on response	V _I = 0 to 5 V, V _O to 0.1%	25°C	125			μs
	V _I = 0 to 5 V, V _O to 0.01%		210			

† Full range is -40°C to 85°C.

‡ The listed values are not production tested.

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C – MARCH 1991 – REVISED MAY 1998

electrical characteristics at specified free-air temperature, $V_I = 5\text{ V}$, $I_O = 0$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLE2425M			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	2.48	2.5	2.52	V
		Full range	2.47		2.53	
Temperature coefficient of output voltage		25°C		20		ppm/°C
Bias current	$I_O = 0$	25°C		170	250	µA
		Full range			250	
Input voltage regulation	$V_I = 4.5\text{ V to }5.5\text{ V}$	25°C		1.5	20	µV
		Full range			100	
	$V_I = 4.5\text{ V to }40\text{ V}$	25°C		1.5	20	µV/V
		Full range			100	
Ripple rejection	$f = 120\text{ Hz}$, $\Delta V_I(\text{PP}) = 1\text{ V}$	25°C		80		dB
Output voltage regulation (source current)‡	$I_O = 0\text{ to }-10\text{ mA}$	25°C	-160	-45	160	µV
	Full range		-250		250	
Output voltage regulation (sink current)‡	$I_O = 0\text{ to }3\text{ mA}$	25°C	-450	-150	450	µV
		Full range				
	$I_O = 0\text{ to }20\text{ mA}$	25°C	-160	15	160	
		Full range				
Long-term drift of output voltage	$\Delta t = 1000\text{ h}$, Noncumulative	25°C		15		ppm
Output impedance		25°C		7.5	22.5	mΩ
Short-circuit output current (sink current)	$V_O = 5\text{ V}$	25°C	30	55		mA
Short-circuit output current (source current)	$V_O = 0$		-30	-50		
Output noise voltage, rms	$f = 10\text{ Hz to }10\text{ kHz}$	25°C		100		µV
Output voltage response to output current step	$V_O\text{ to }0.1\%$, $I_O = \pm 10\text{ mA}$	25°C	$C_L = 0$		110	µs
			$C_L = 100\text{ pF}$		115	
	$V_O\text{ to }0.01\%$, $I_O = \pm 10\text{ mA}$	$C_L = 0$		180		
		$C_L = 100\text{ pF}$		180		
Output voltage response to input voltage step	$V_I = 4.5\text{ to }5.5\text{ V}$, $V_O\text{ to }0.1\%$	25°C		12	µs	
	$V_I = 4.5\text{ to }5.5\text{ V}$, $V_O\text{ to }0.01\%$			30		
Output voltage turn-on response	$V_I = 0\text{ to }5\text{ V}$, $V_O\text{ to }0.1\%$	25°C		125	µs	
	$V_I = 0\text{ to }5\text{ V}$, $V_O\text{ to }0.01\%$			210		

† Full range is -55°C to 125°C.

‡ The listed values are not production tested.



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TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C – MARCH 1991 – REVISED MAY 1998

electrical characteristics $V_I = 5\text{ V}$, $I_O = 0$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2425Y			UNIT
		MIN	TYP	MAX	
Output voltage			2.5		V
Temperature coefficient of output voltage			20		ppm/°C
Bias current	$I_O = 0$		170		μA
Input voltage regulation	$V_I = 4.5\text{ V to } 5.5\text{ V}$		1.5		μV
	$V_I = 4\text{ V to } 40\text{ V}$		1.5		$\mu\text{V/V}$
Ripple rejection	$f = 120\text{ Hz}$, $\Delta V_I(\text{PP}) = 1\text{ V}$		80		dB
Output voltage regulation (source current)†	$I_O = 0\text{ to } -10\text{ mA}$		-45		μV
	$I_O = 0\text{ to } -20\text{ mA}$		-150		
Output voltage regulation (sink current)†	$I_O = 0\text{ to } 10\text{ mA}$		15		μV
	$I_O = 0\text{ to } 20\text{ mA}$		65		
Output impedance			7.5		$\text{m}\Omega$
Short-circuit output current (sink current)	$V_O = 5\text{ V}$		55		mA
Short-circuit output current (source current)	$V_O = 0$		-50		
Output noise voltage, rms	$f = 10\text{ Hz to } 10\text{ kHz}$		100		μV
Output voltage response to output current step	$V_O\text{ to } 0.1\%$, $I_O = \pm 10\text{ mA}$	$C_L = 0$	110		μs
		$C_L = 100\text{ pF}$	115		
	$V_O\text{ to } 0.01\%$, $I_O = \pm 10\text{ mA}$	$C_L = 0$	180		
		$C_L = 100\text{ pF}$	180		
Output voltage response to input voltage step	$V_I = 4.5\text{ to } 5.5\text{ V}$, $V_O\text{ to } 0.1\%$		12		μs
	$V_I = 4.5\text{ to } 5.5\text{ V}$, $V_O\text{ to } 0.01\%$		30		
Output voltage turn-on response	$V_I = 0\text{ to } 5\text{ V}$, $V_O\text{ to } 0.1\%$		125		μs
	$V_I = 0\text{ to } 5\text{ V}$, $V_O\text{ to } 0.01\%$		210		

† The listed values are not production tested.

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

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TYPICAL CHARACTERISTICS

Table Of Graphs

		FIGURE
Output voltage	Distribution	1
	vs Free-air temperature	2
Output voltage hysteresis	vs Free-air temperature	3
Input bias current	vs Input voltage	4
	vs Free-air temperature	5
Input voltage regulation		6
Ripple rejection	vs Frequency	7
Output voltage regulation		8
Output impedance	vs Frequency	9
Short-circuit output current	vs Free-air temperature	10
Spectral noise voltage density	vs Frequency	11
Wide-band noise voltage	vs Frequency	12
Output voltage change with current step	vs Time	13
Output voltage change with voltage step	vs Time	14
Output voltage power-up response	vs Time	15
Output current	vs Load capacitance	16



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TYPICAL CHARACTERISTICS†

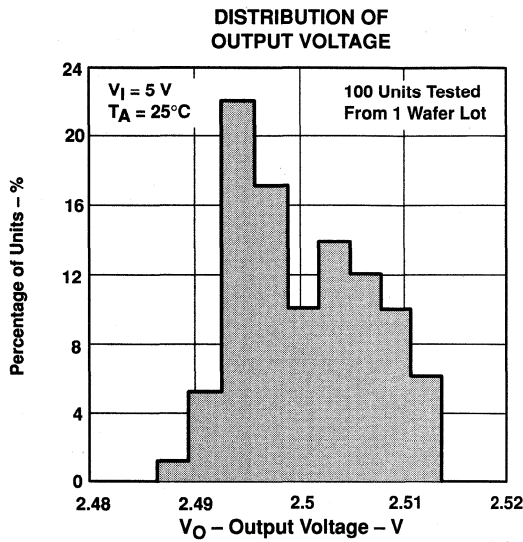


Figure 1

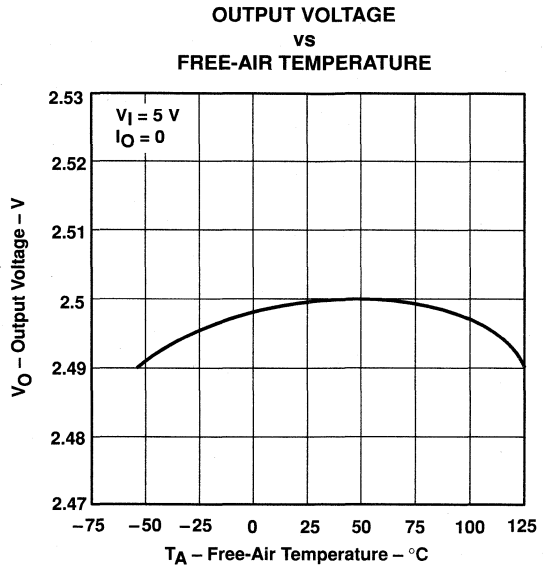


Figure 2

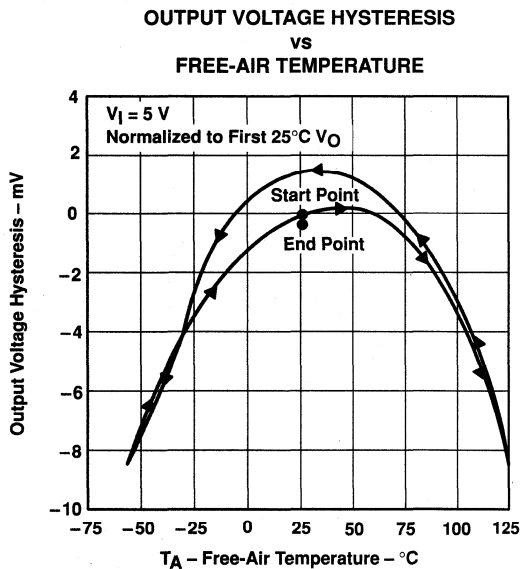


Figure 3

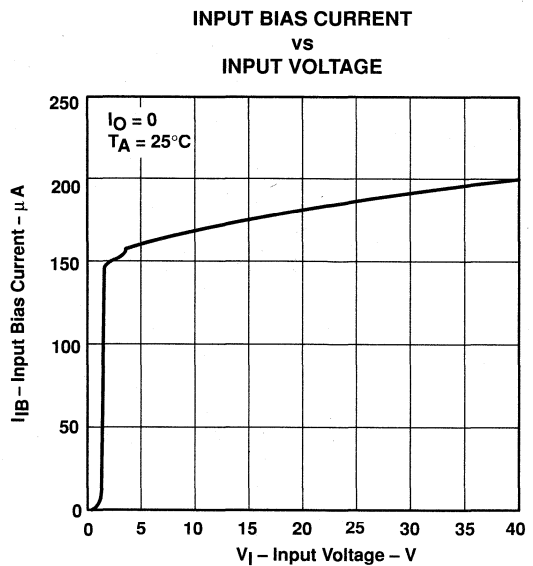


Figure 4

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

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TYPICAL CHARACTERISTICS†

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**

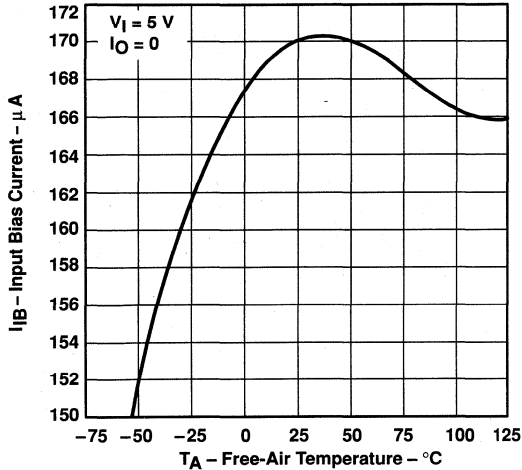


Figure 5

INPUT VOLTAGE REGULATION

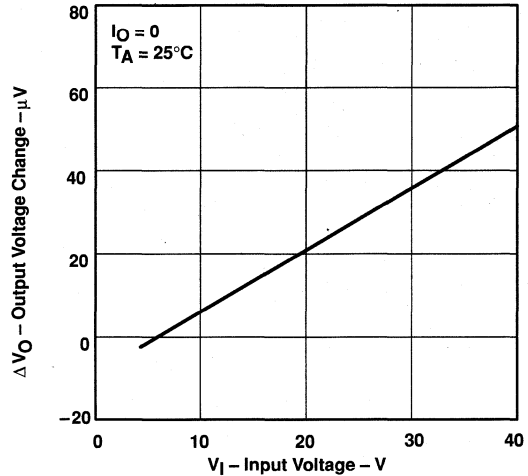


Figure 6

**RIPPLE REJECTION
vs
FREQUENCY**

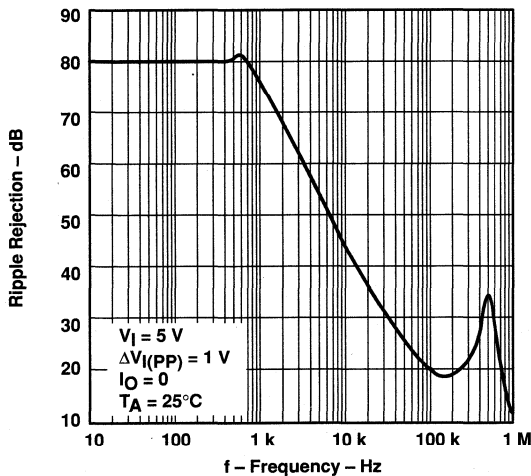


Figure 7

OUTPUT VOLTAGE REGULATION

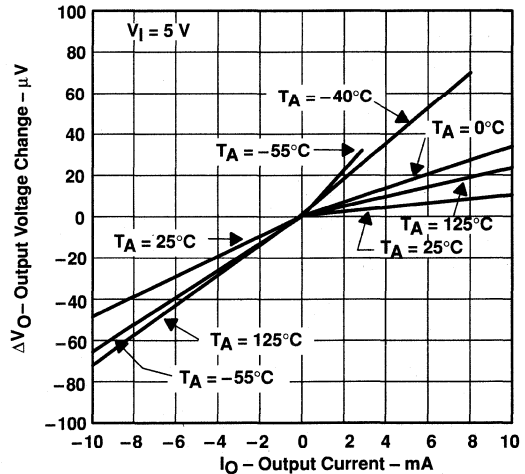


Figure 8

† Data at high and low temperatures are applicable within rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

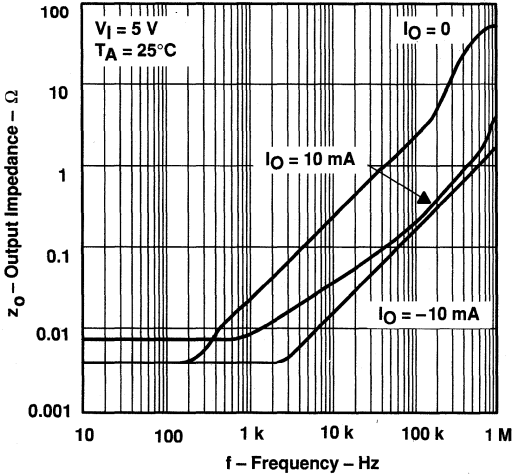


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

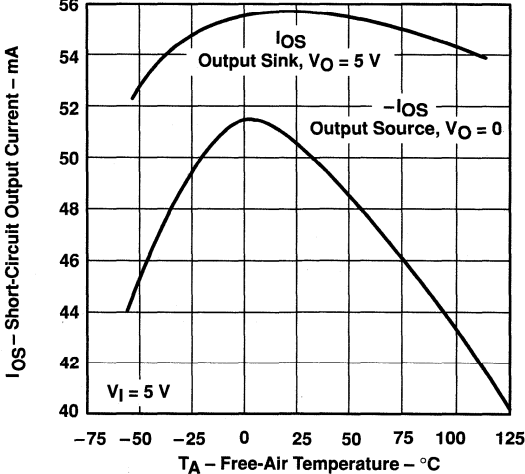


Figure 10

SPECTRAL NOISE VOLTAGE DENSITY
vs
FREQUENCY

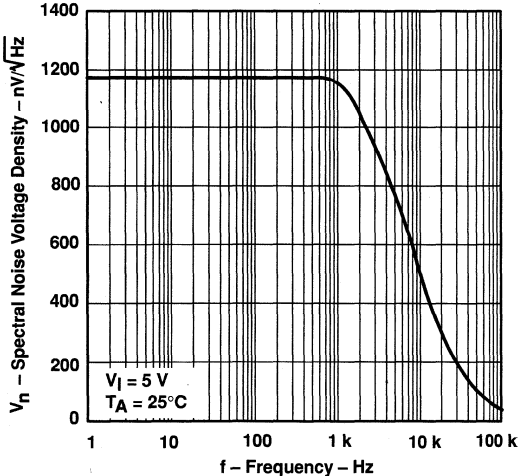


Figure 11

WIDE-BAND NOISE VOLTAGE
vs
FREQUENCY

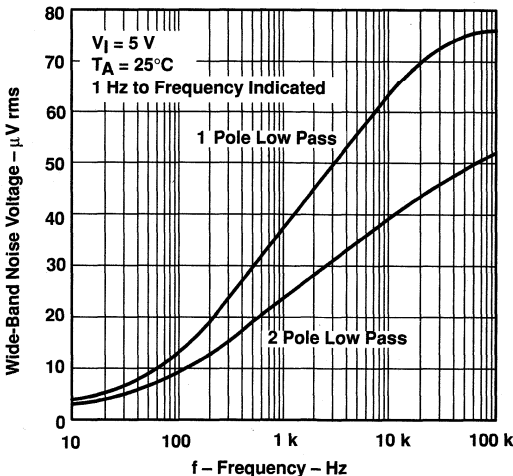


Figure 12

TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE
TO OUTPUT CURRENT STEP
vs
TIME

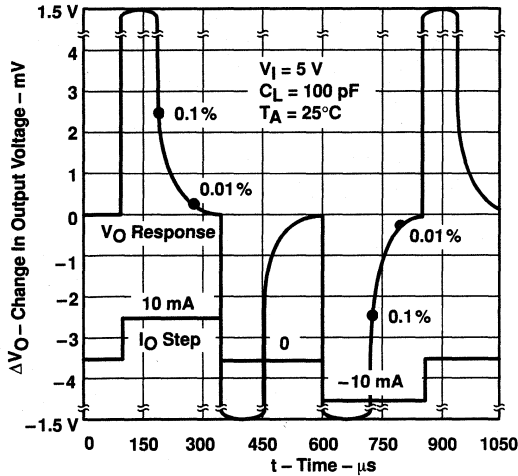


Figure 13

OUTPUT VOLTAGE RESPONSE
TO INPUT VOLTAGE STEP
vs
TIME

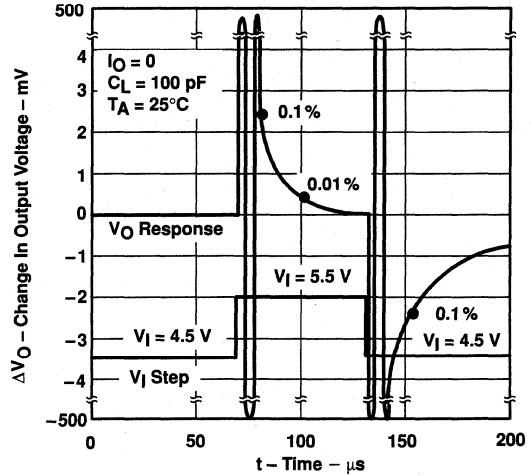


Figure 14

OUTPUT VOLTAGE POWER-UP RESPONSE
vs
TIME

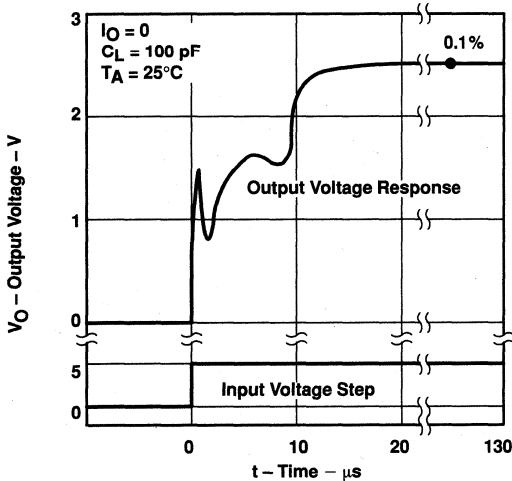


Figure 15

STABILITY RANGE
OUTPUT CURRENT
vs
LOAD CAPACITANCE

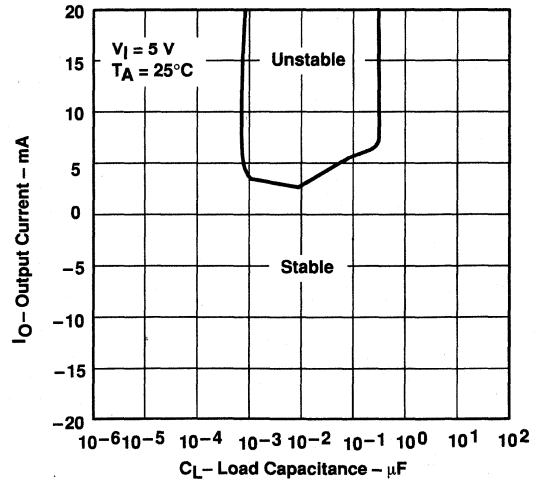


Figure 16

macromodel information

```
* TLE2425 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
* REV (N/A) SUPPLY VOLTAGE: 5 V
* CONNECTIONS: INPUT
*           | COMMON
*           | | OUTPUT
*           | | |
.SUBCKT TLE2425 3 4 5
*
```

```
* OPAMP SECTION
C1 11 12 21.66E-12
C2 6 7 30.00E-12
C3 87 0 10.64E-9
CPSR 85 86 15.9E-9
DCM+ 81 82 DX
DCM- 83 81 DX
DC 5 53 DX
DE 54 5 DX
DLN 92 90 DX
DLP 90 91 DX
DP 4 3 DX
ECMR 84 99 (2,99) 1
EGND 99 0 POLY(2) (3,0) (4,0) 0 .5 .5
EPSR 85 0 POLY(1) (3,4) -16.22E-6 3.24E-6
ENSE 89 2 POLY(1) (88,0) 120E-6 1
FB 7 99 POLY(6) VB VC VE VLPV LNVPSR O 74.8E6 -10E6 10E6 10E6
+ -10E6 74E6
GA 6 0 11 12 320.4E-6
GCM 0 6 10 99 1.013E-9
GPSR 85 86 (85,86) 100E-6
GRC1 4 11 (4,11) 3.204E-4
GRC2 4 12 (4,12) 3.204E-4
GRE1 13 10 (13,10) 1.038E-3
GRE2 14 10 (14,10) 1.038E-3
HLIM 90 0 VLIM 1K
HCMR 80 1 POLY(2) VCM+ VCM- 0 1E2 1E2
IRP 3 4 146E-6
IEE 3 10 DC 24.05E-6
IIO 2 0 .2E-9
I1 88 0 1E-21
Q1 11 89 13 QX
Q2 12 80 14 QX
R2 6 9 100.0E3
RCM 84 81 1K
REE 10 99 8.316E6
RN1 87 0 2.55E8
RN2 87 88 11.67E3
```

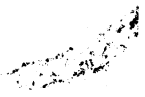
TLE2425, TLE2425Y PRECISION VIRTUAL GROUND

SLOS065C - MARCH 1991 - REVISED MAY 1998

macromodel information (continued)

```
RO1      8  5  63
RO2      7  99 62
VCM+    82 99 1.0
VCM-    83 99 -2.3
VB       9  0  DC 0
VC       3  53 DC 1.400
VE      54  4  DC 1.400
VLIM     7  8  DC 0
VLP     91  0  DC 30
VLN      0  92 DC 30
VPSR     0  86 DC 0
RFB      5  2  1K
RIN     30  1  1K
RCOM    34  4  .1
*REGULATOR SECTION
RG1     30  0  20MEG
RG2     30  31 .2
RG3     31  35 400K
RG4     35  34 411K
RG5     31  36 25MEG
HREG    31  32 POLY(2)  VPSET VNSET 0 1E21E2
VREG    32  33 DC 0V
EREG    33  34 POLY(1)  (36,34) 1.23 1
VADJ    36  34 1.27V
HPSET   37  0  VREG 1.030E3
VPSET   38  0  DC 20V
HNSET   39  0  VREG 6.11E5
VNSET   40  0  DC -20V
DSUB    4  34 DX
DPOS    37  38 DX
DNNEG   40  39 DX
.MODEL DX D(IS=800.0E-18)
.MODEL QX PNP(IS=800.0E-18 BF=480)
.ENDS
```

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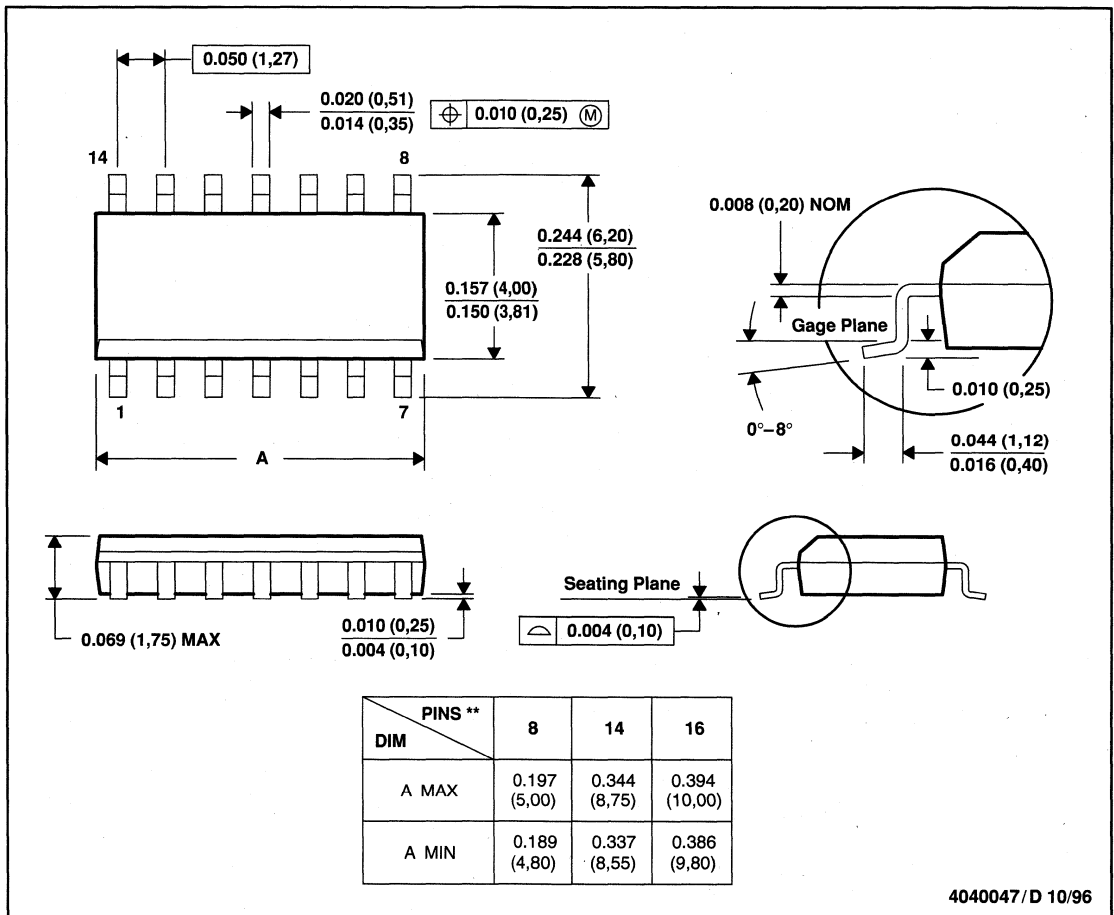
5

Mechanical Data

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



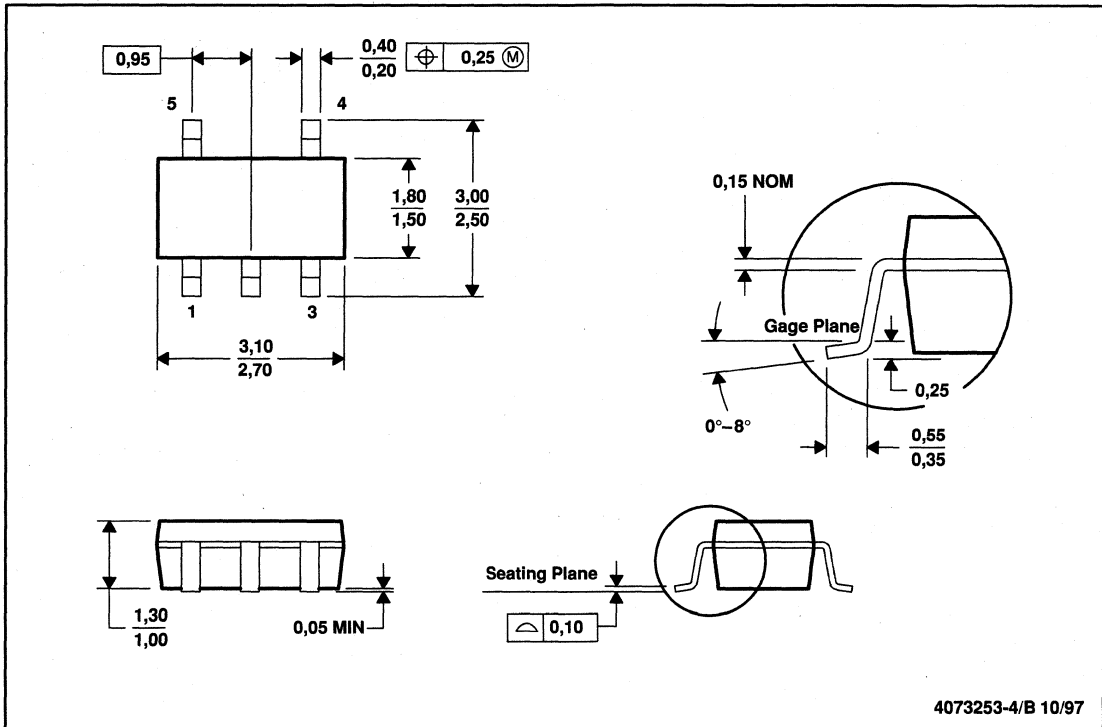
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

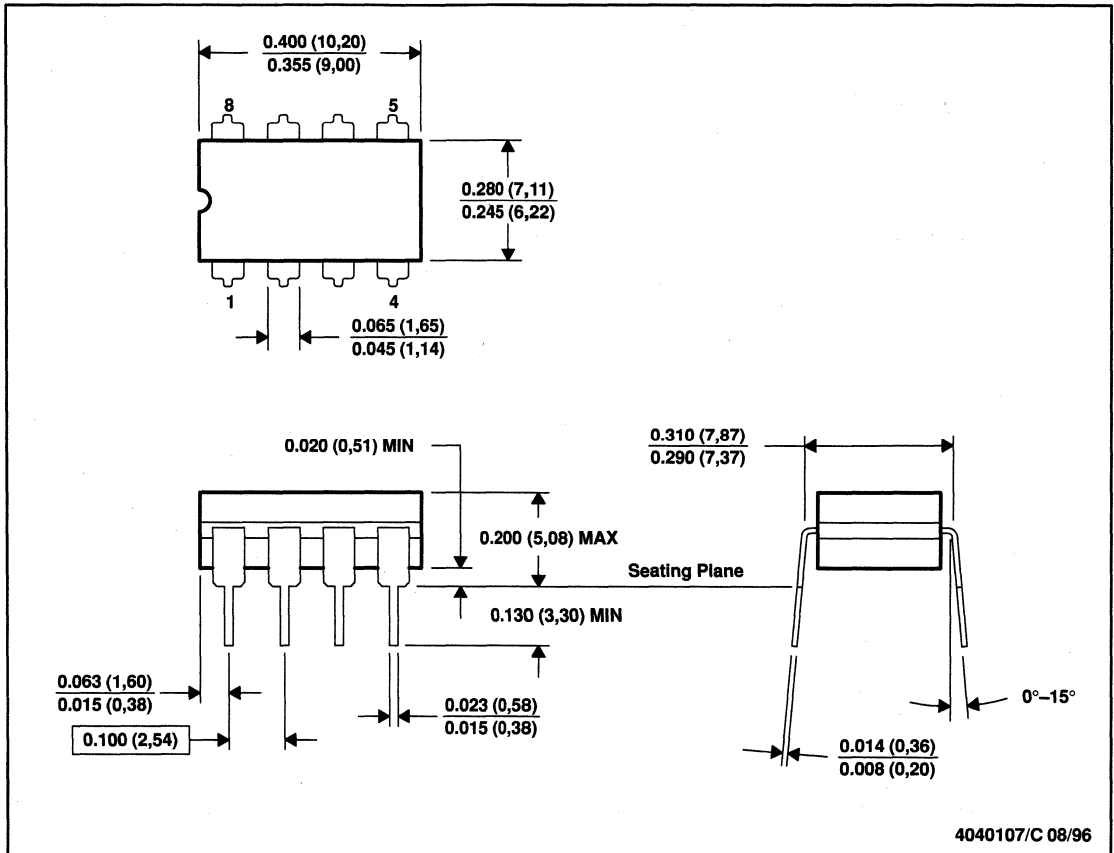


- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



4040107/C 08/96

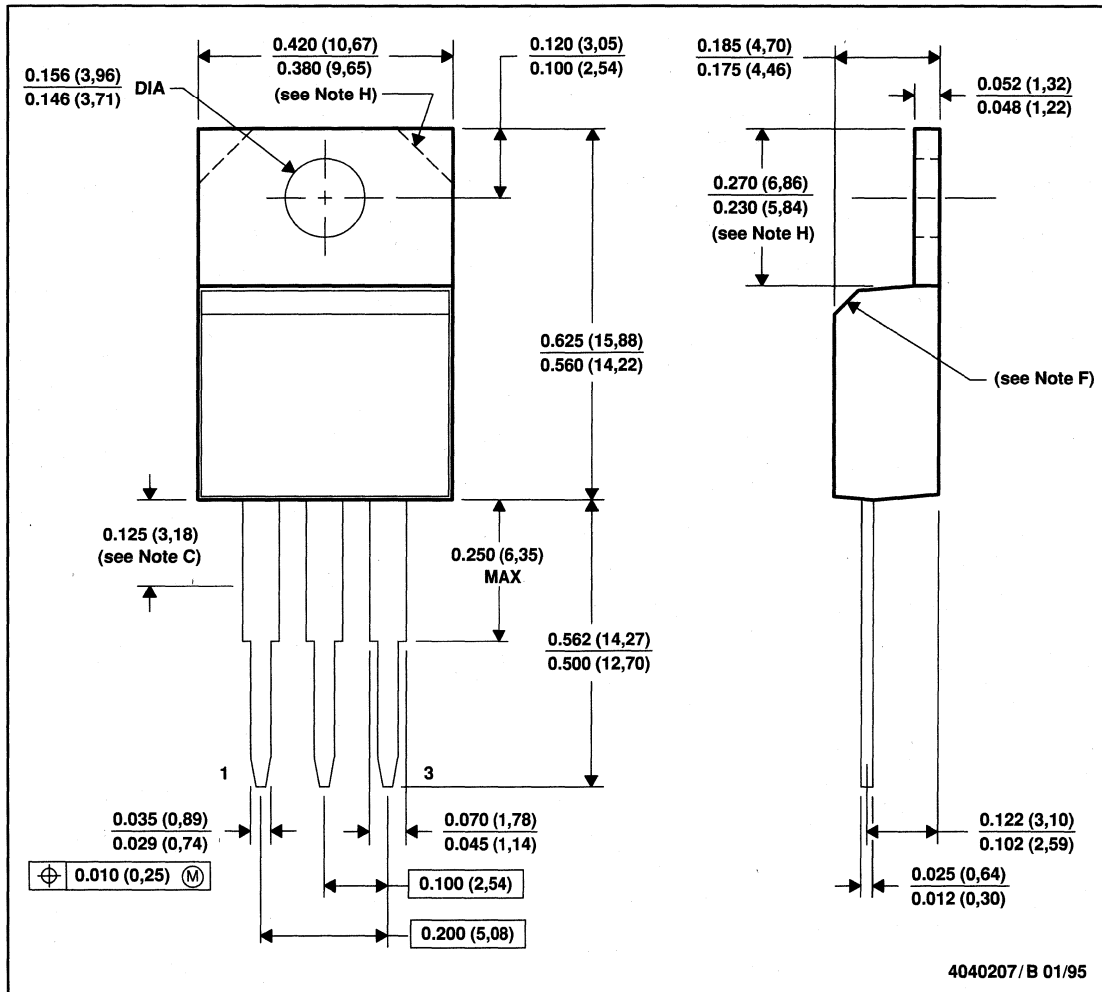
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL DATA

MECHANICAL INFORMATION

KC (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE

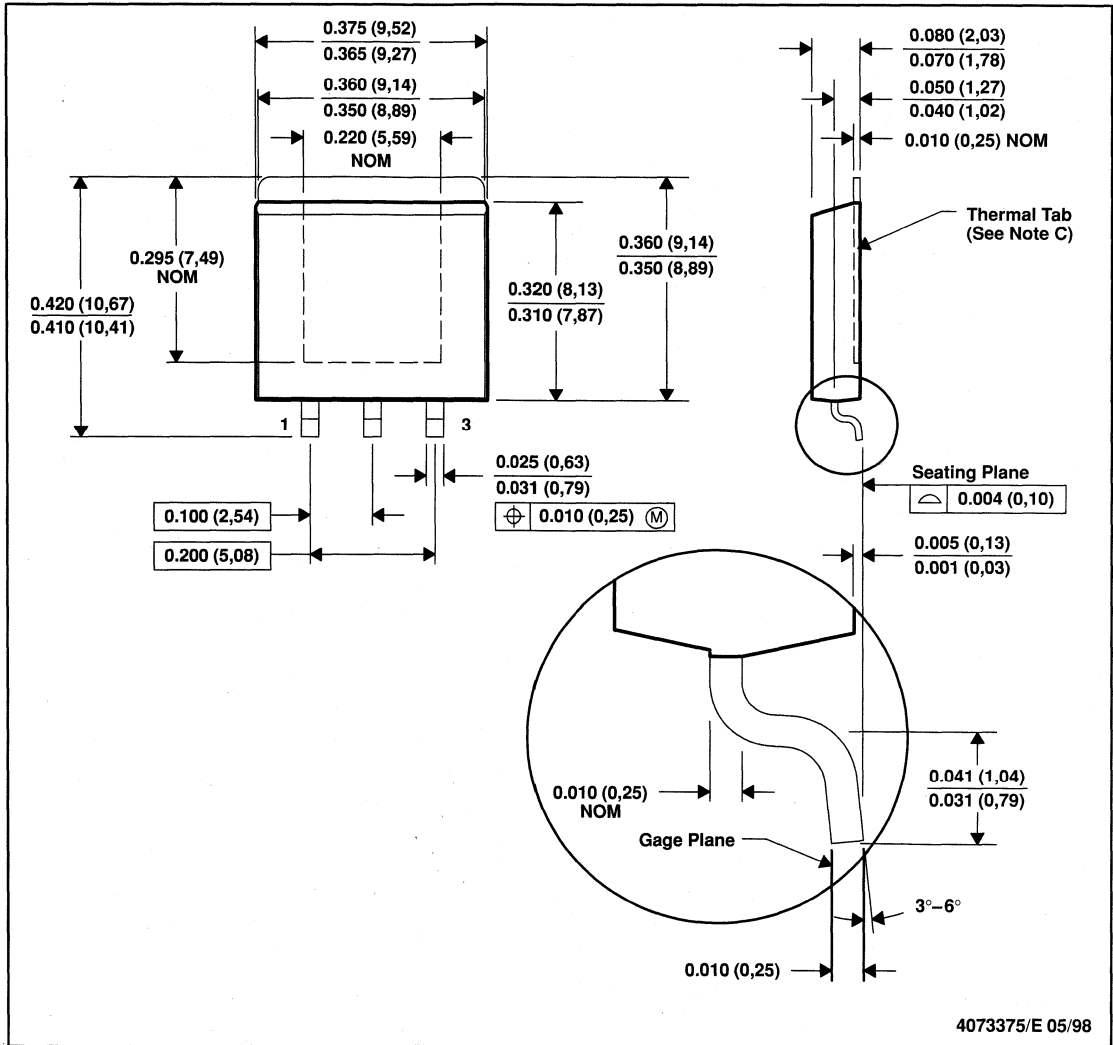


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Lead dimensions are not controlled within this area.
 - All lead dimensions apply before solder dip.
 - The center lead is in electrical contact with the mounting tab.
 - The chamfer is optional.
 - Falls within JEDEC TO-220AB
 - Tab contour optional within these dimensions

MECHANICAL INFORMATION

KTE (R-PSFM-G3)

PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. The center lead is in electrical contact with the thermal tab.
 D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

PowerFLEX is a trademark of Texas Instruments Incorporated.



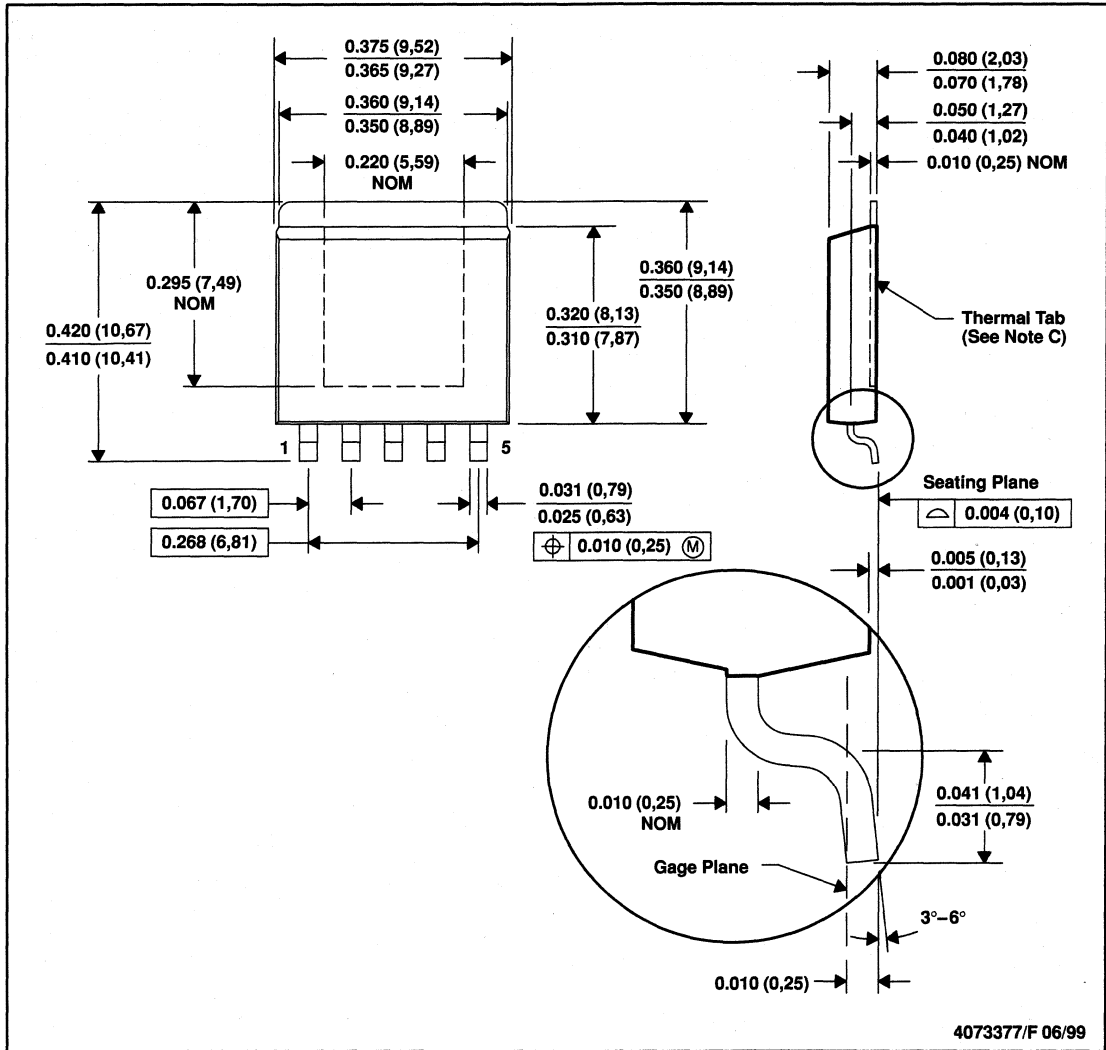
MECHANICAL DATA

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MECHANICAL INFORMATION

KTG (R-PSFM-G5)

PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - The center lead is in electrical contact with the thermal tab.
 - Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

PowerFLEX is a trademark of Texas Instruments Incorporated.

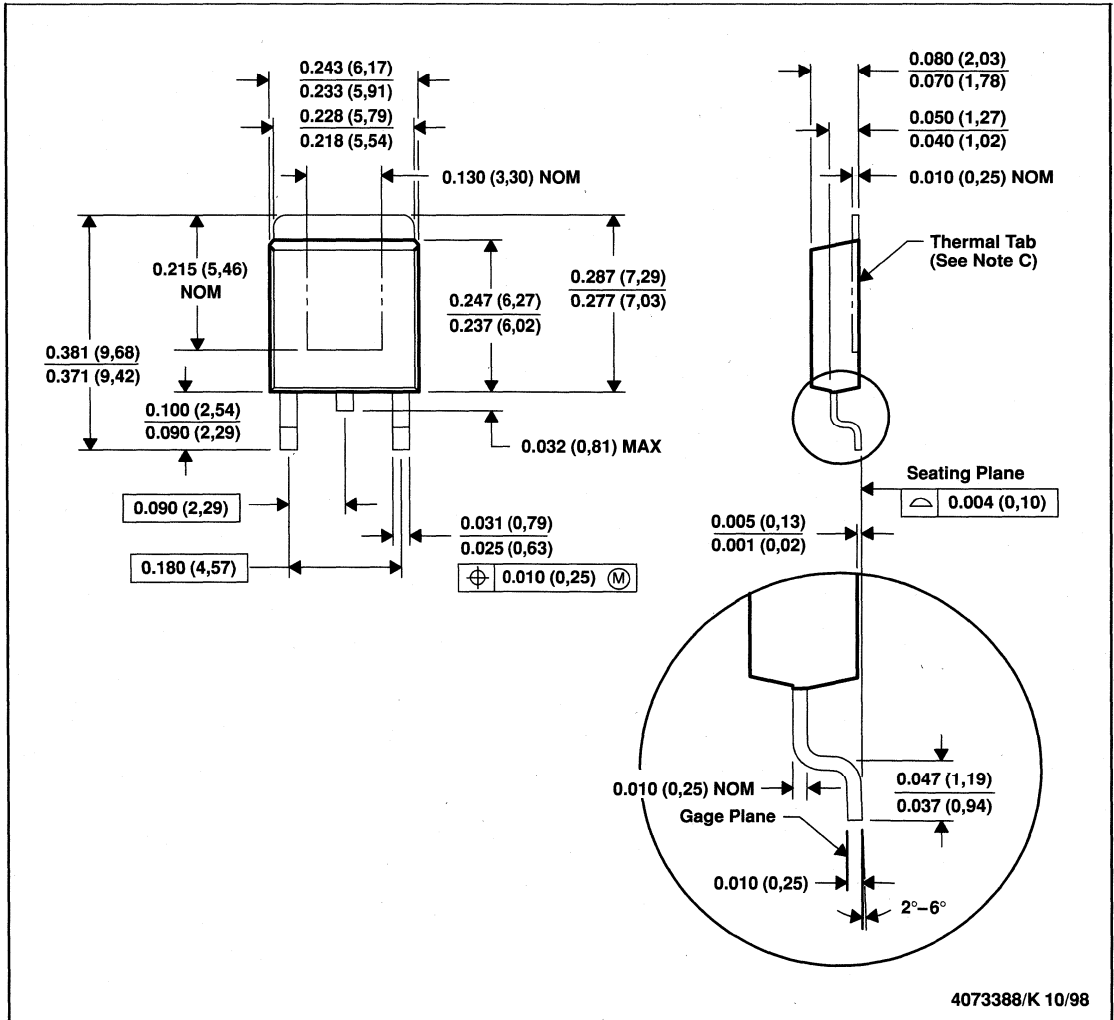
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MECHANICAL INFORMATION

KTP (R-PSFM-G2)

PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. The center lead is in electrical contact with the thermal tab.
 D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

PowerFLEX is a trademark of Texas Instruments Incorporated.



MECHANICAL DATA

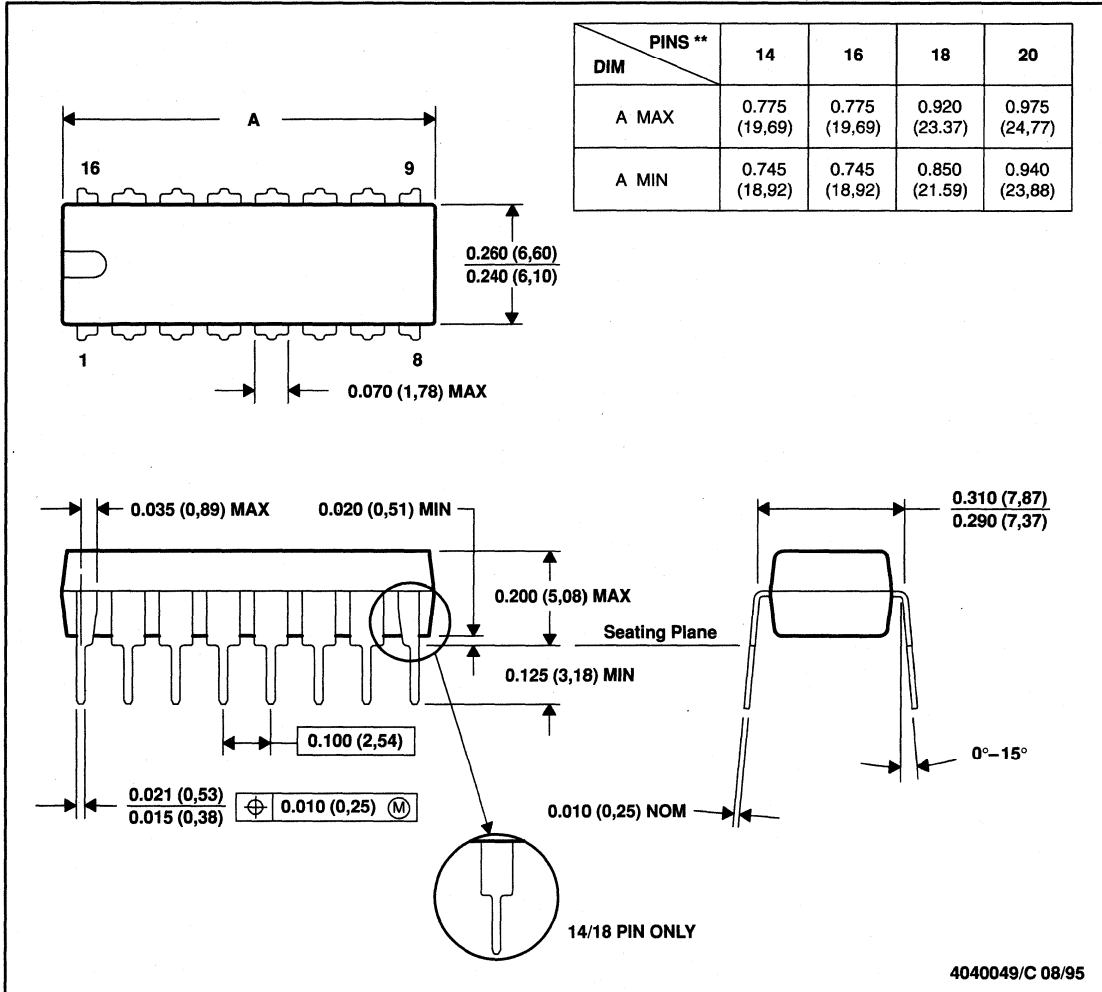
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MECHANICAL INFORMATION

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN

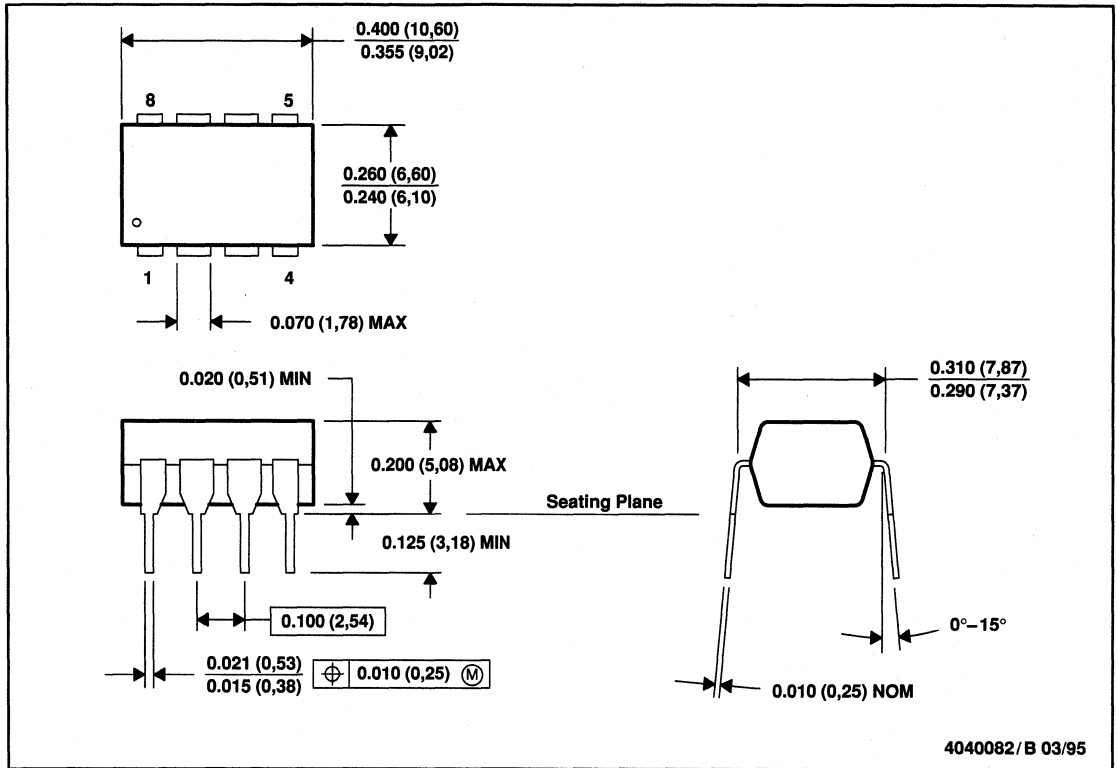


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

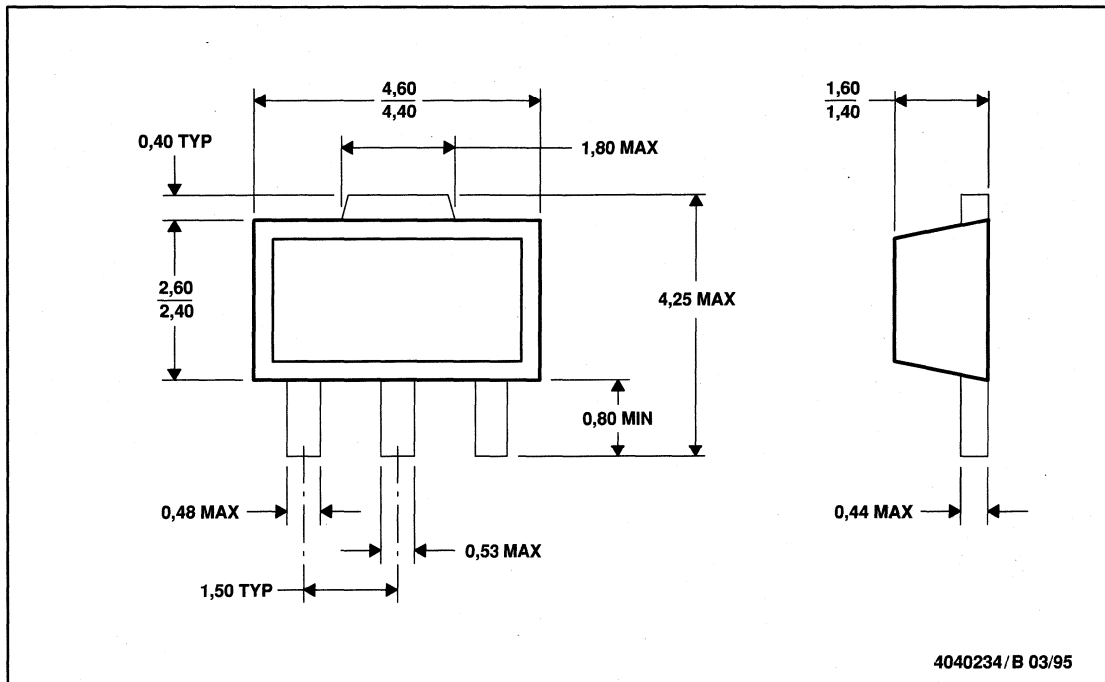
MECHANICAL DATA

MPFM003E - OCTOBER 1994 - REVISED JUNE 1999

MECHANICAL INFORMATION

PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



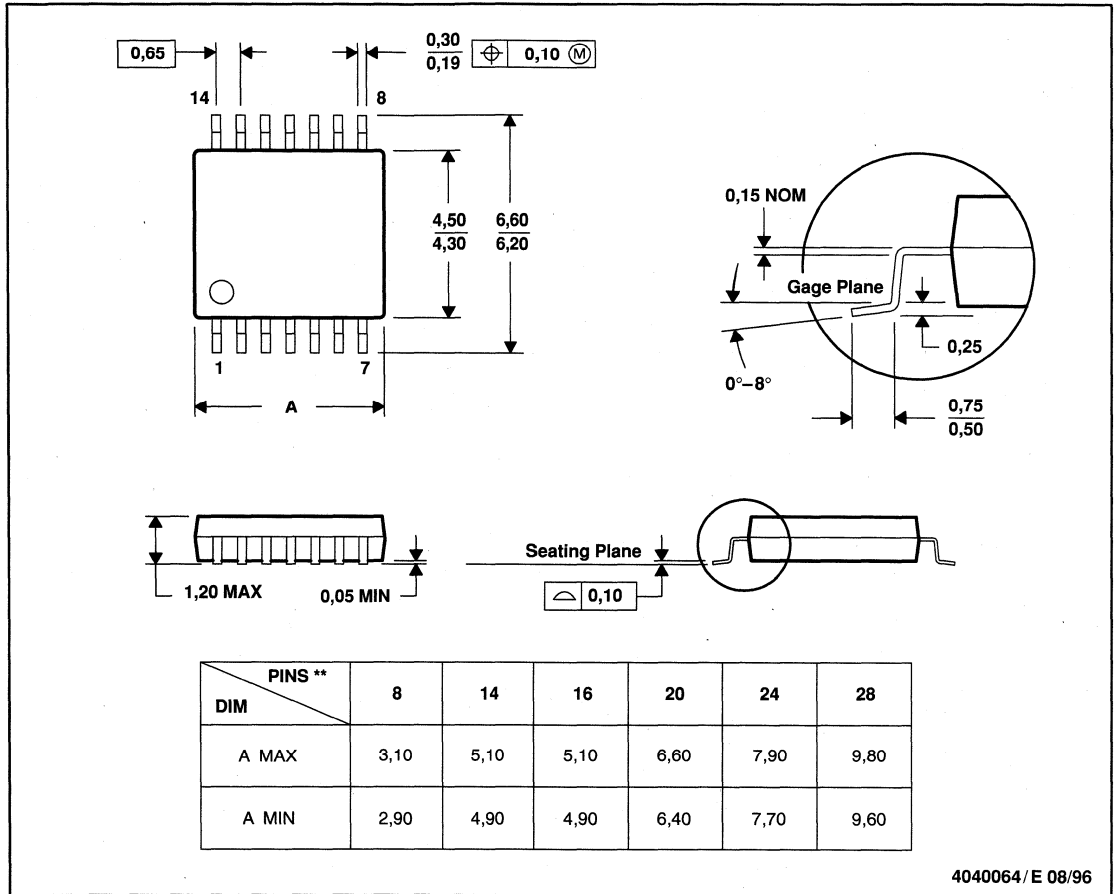
- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/ E 08/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

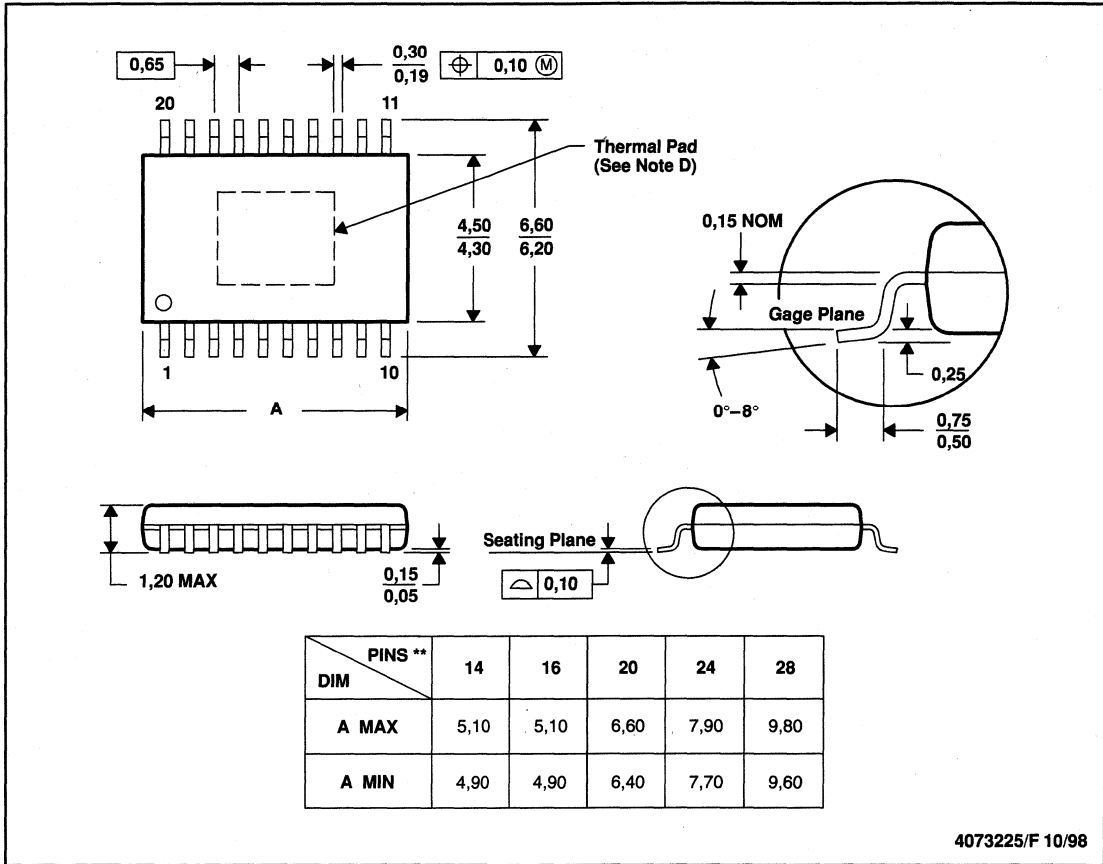
MHTS001D – JANUARY 1995 – REVISED MAY 1999

MECHANICAL INFORMATION

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusions.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.



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NOTES

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A050200